

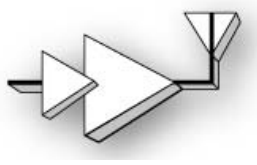


Millimeter Wave CMOS Power Amplifiers

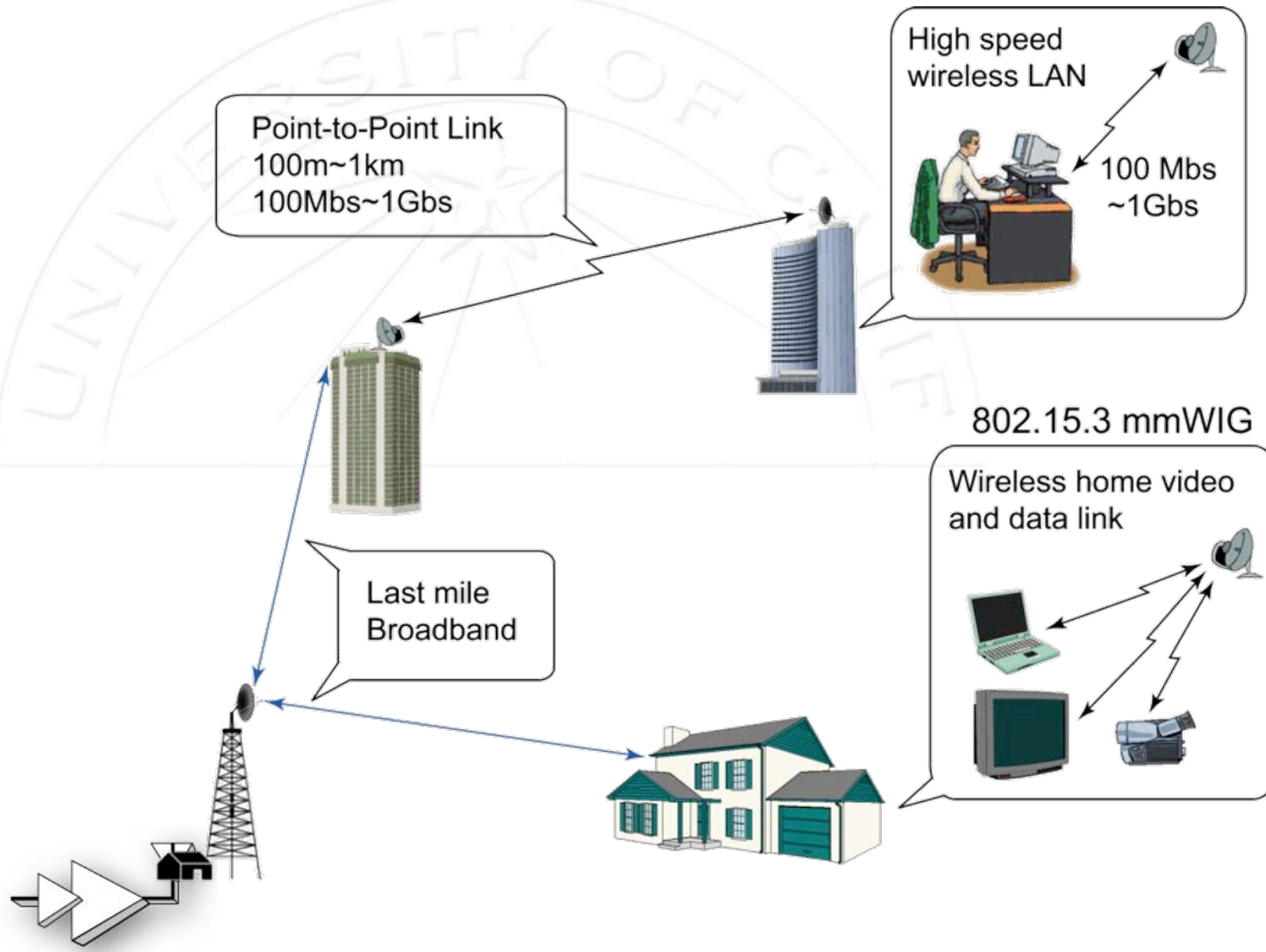
Professor Ali M. Niknejad
Berkeley Wireless Research Center
University of California, Berkeley

Outline

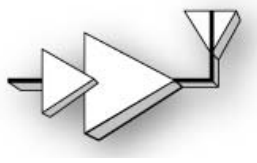
- Applications / Performance Requirements
- PA Amplifier Design Examples
- Complete “Digital” CMOS PA Transmitter



The “Last Inch”

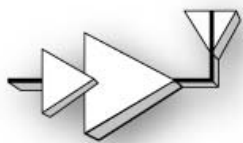
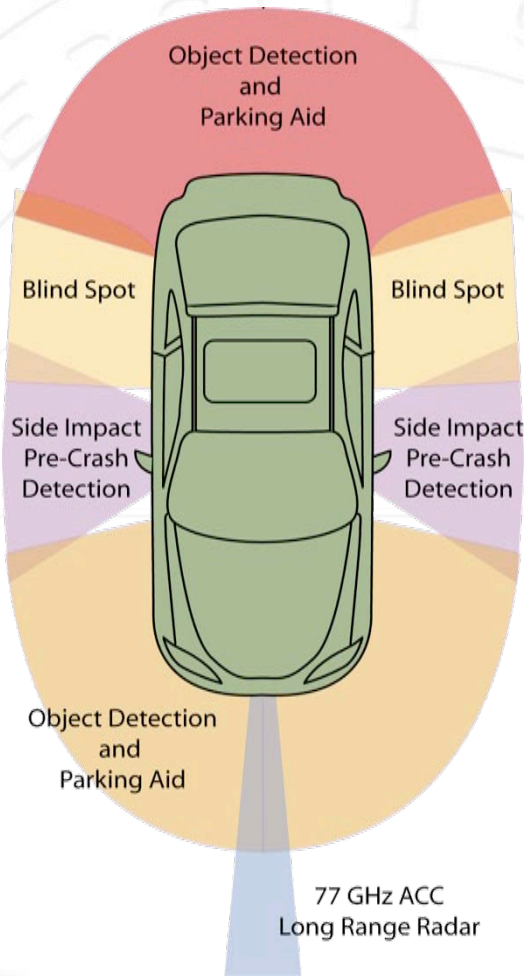


Universal Mobility

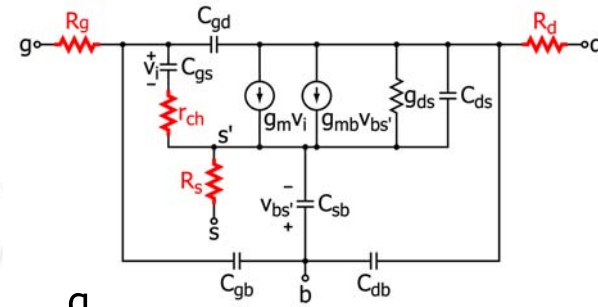
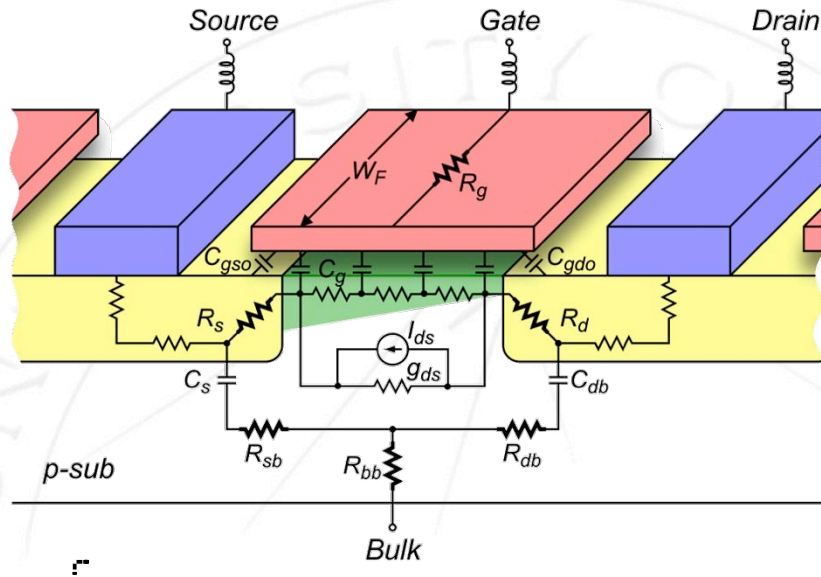


Automotive Radar

- Short range radar for parking assist, object detection
- Long range radars for automatic cruise control, low visibility (fog) object detection, impact warning
- Long range vision: automatic driver



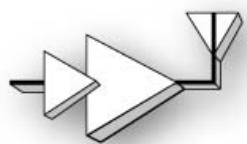
CMOS Technology Trends



$$f_t \approx \frac{g_m}{2\pi C_{gg}}$$

$$f_{max} \approx \frac{f_t}{2\sqrt{R_g(g_m C_{gd}/C_{gg}) + (R_g + r_{ch} + R_s)g_{ds}}}$$

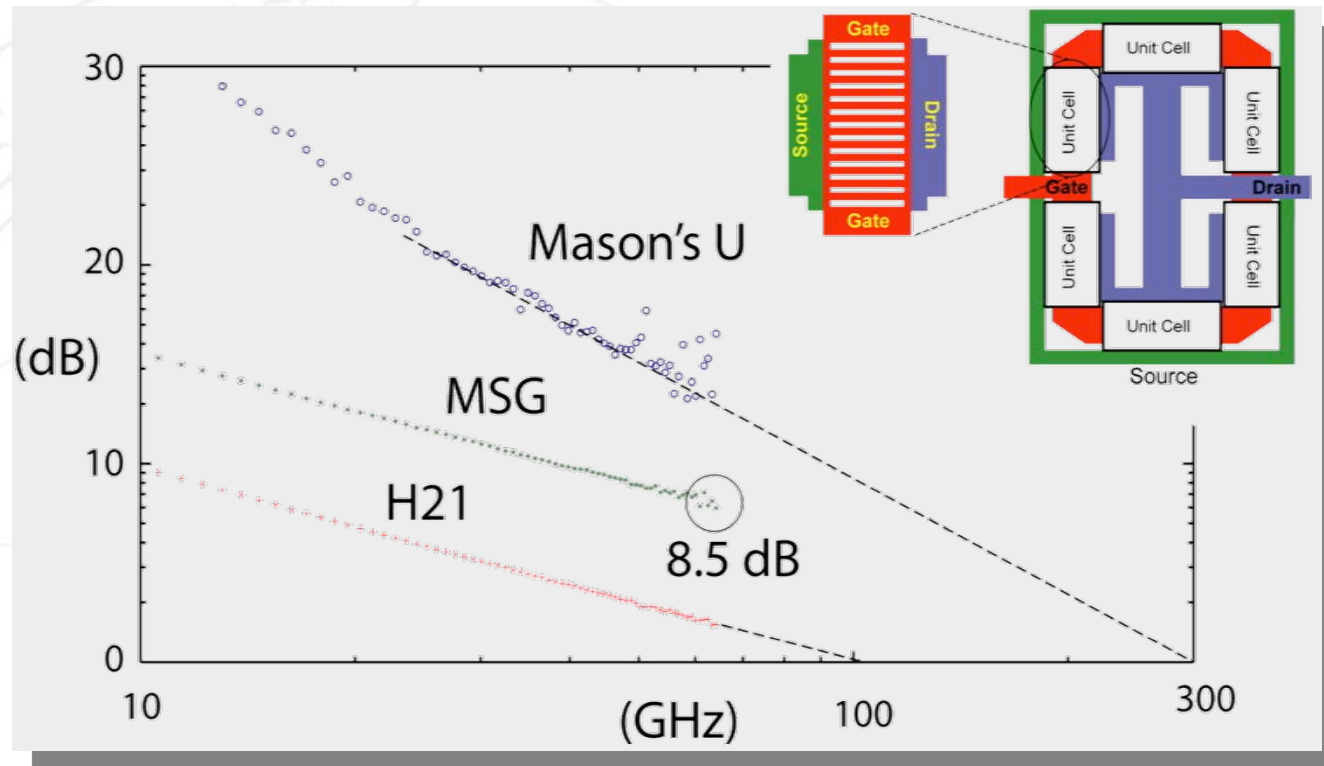
	130nm	90 nm	65nm	45nm
F_t	70 GHz	100 GHz	150 GHz	280 GHz
F_{max}	135 GHz	200-300 GHz	300 GHz	560 GHz
NF_{min} (60 GHz)	4-5 dB	3-4 dB	3 dB	2.3 dB



Measured

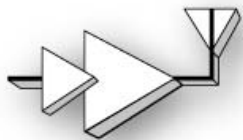
ITRS+projection

Layout Optimization (90nm)



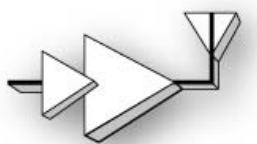
Presented at ISSCC 2007

- MSG 60GHz = 8.5 dB, NFmin ~ 3-4 dB
- $f_{\max} = 300$ GHz (*extrapolated*), $f_T = 100$ GHz
- Highest reported $f_{\max}/f_T = 3$ ratio for CMOS!



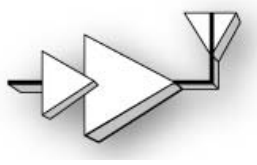
60 GHz Link Budget

Component	Contribution	Comment
Background Noise	-174 dBm/Hz	kT at room temp.
Noise BW	93 dB	2 GHz
Noise Figure	10 dB	RX noise figure
SNR at input	10 dB	Typ. Digital Mod.
Noise at input	-61 dBm	$(-174 + 93 + 10 + 10)$
Antenna Gain	-67 dBm	6 dBi
Path Loss	74 dB	2-m LOS
Other Loss	10 dB	Reflection from wall
Tx Power	17 dBm	$-67 \text{ dBm} + 84 \text{ dB}$
PA output power	11 dBm	6 dBi gain in antenna

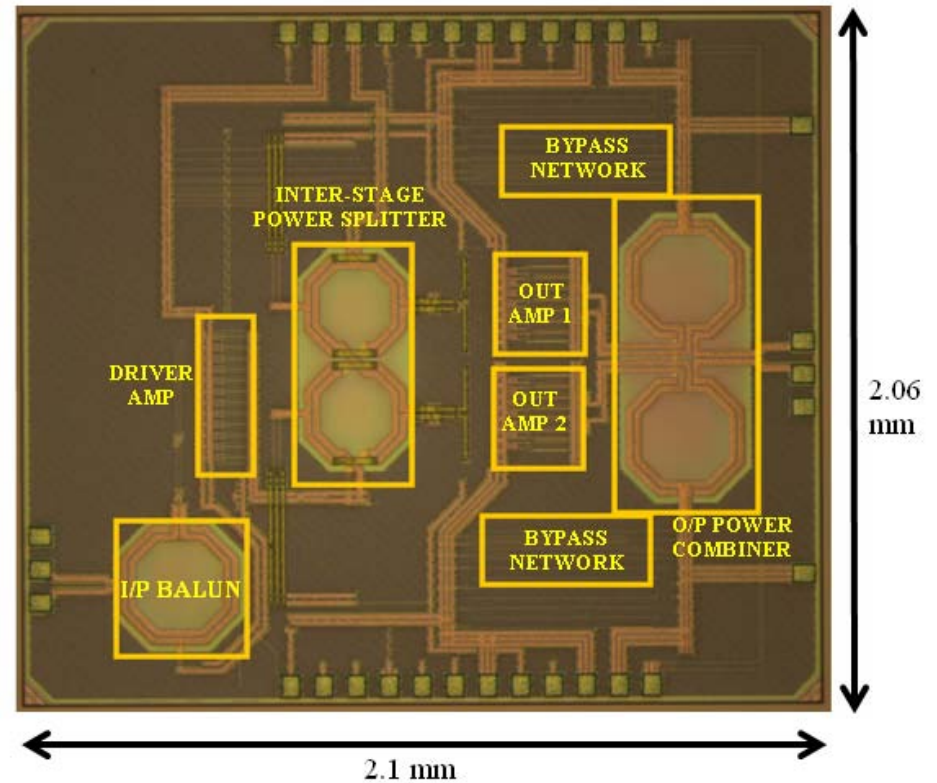
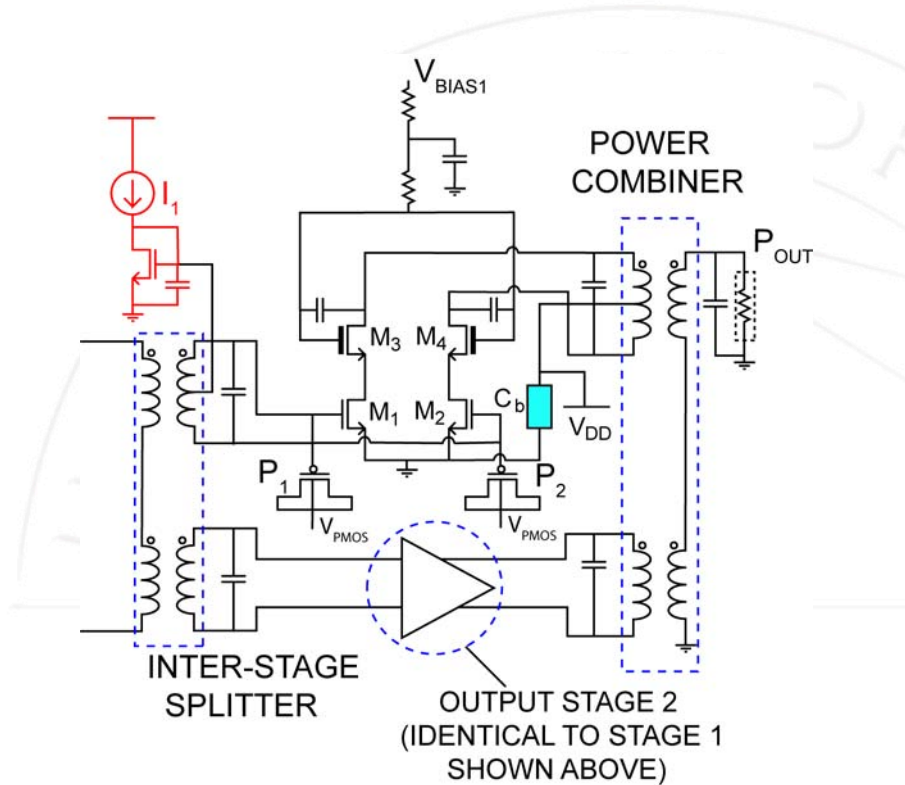




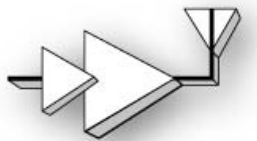
60 GHZ PA DESIGNS



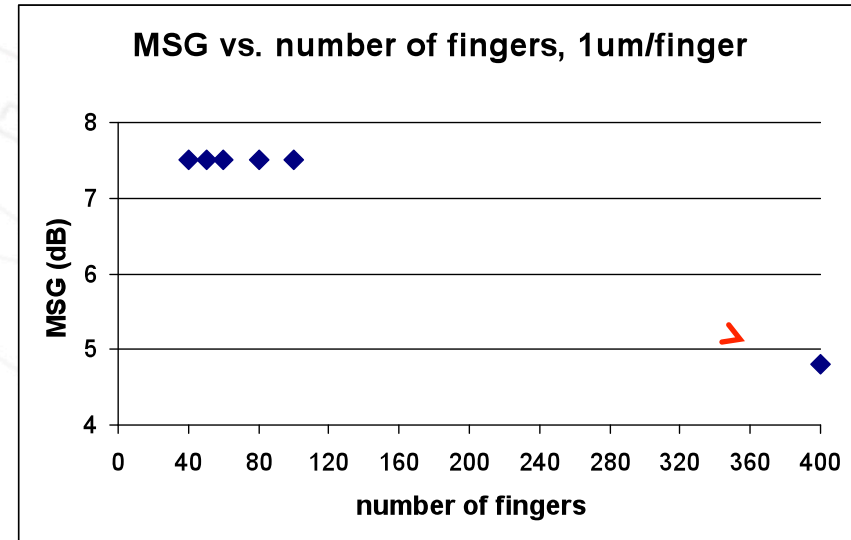
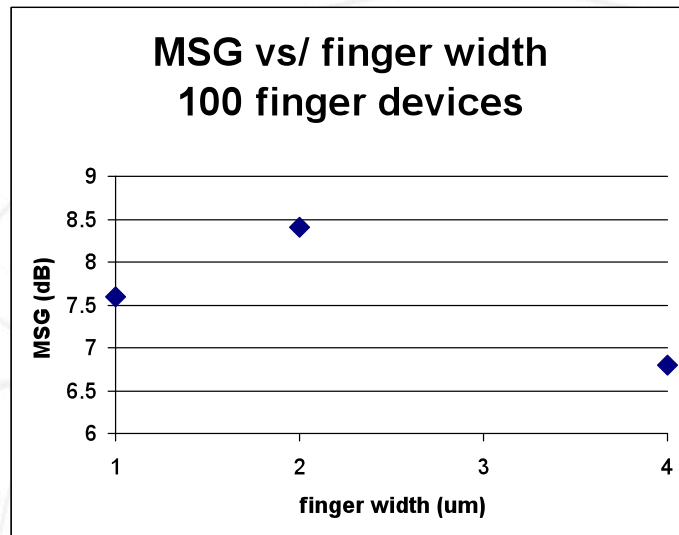
24. GHz WiMAX CMOS PA's



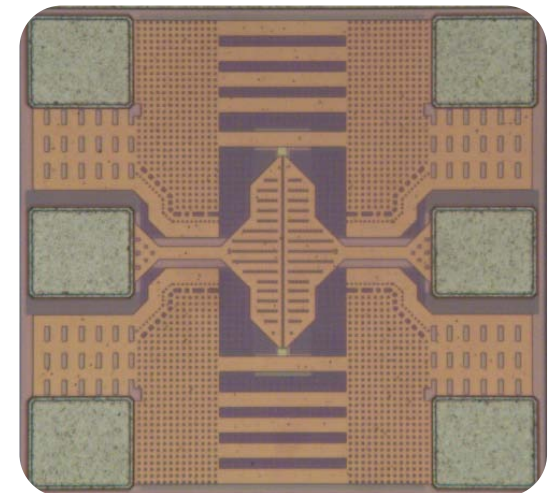
- $P_{sat} > 30$ dBm, $P-1$ dB > 27.7 dBm, PAE = 33%
- OFDM output EVM < -26 dB with 22.7 dBm output power
- Fully FCC compliant, no external components



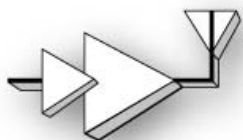
PA Device Selection



- Need a large device for high power → large parasitics → lower gain. Optimum finger size for stable gain.
- Using too many parallel devices leads to low gain

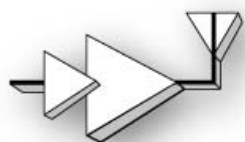
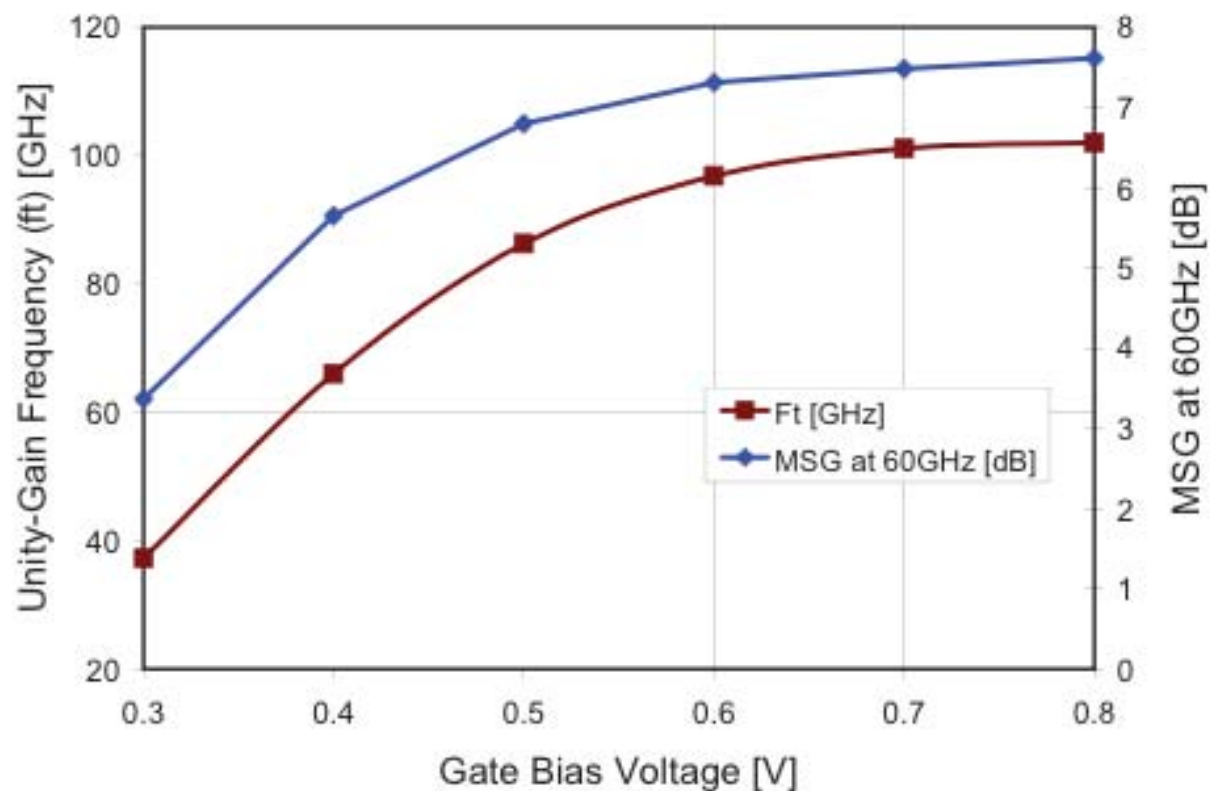


400u x 1u device

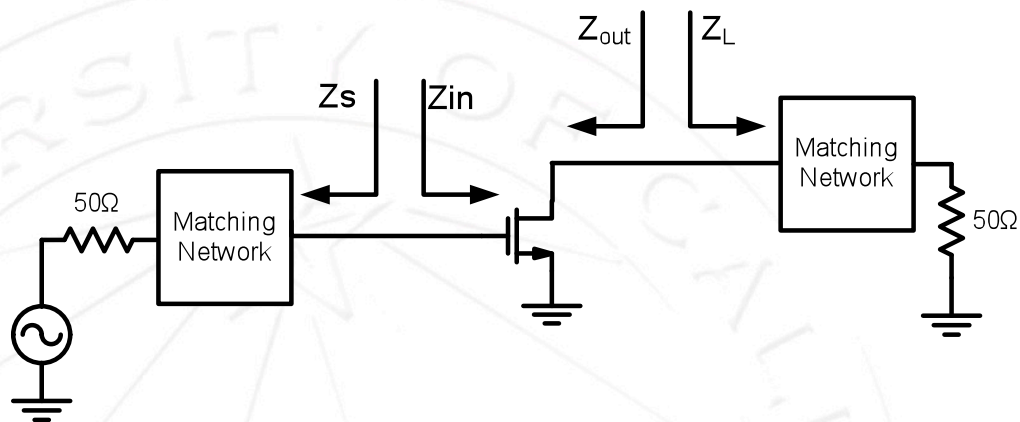


PA Bias / Class of Operation

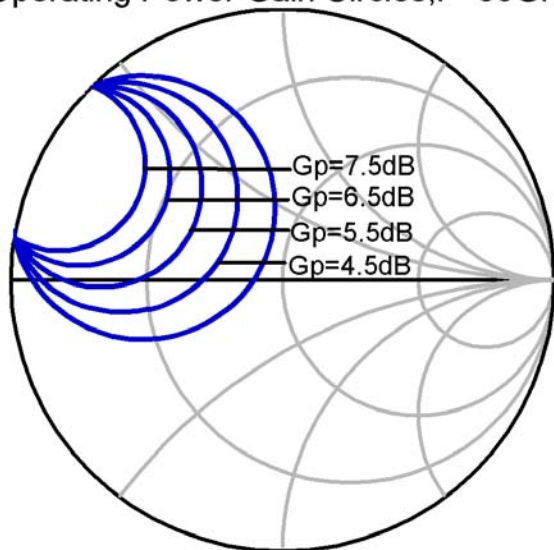
- Gain of device drops quickly requiring operating in the strong inversion regime
- Class AB biasing does not provide sufficient gain (PAE too low)



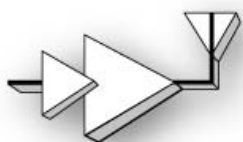
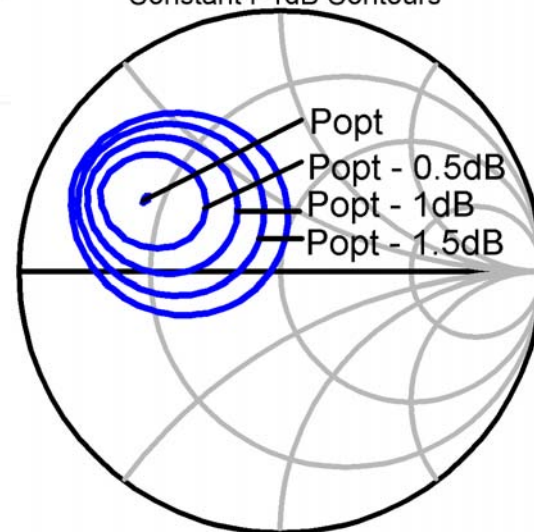
Gain vs. Output Power Tradeoff



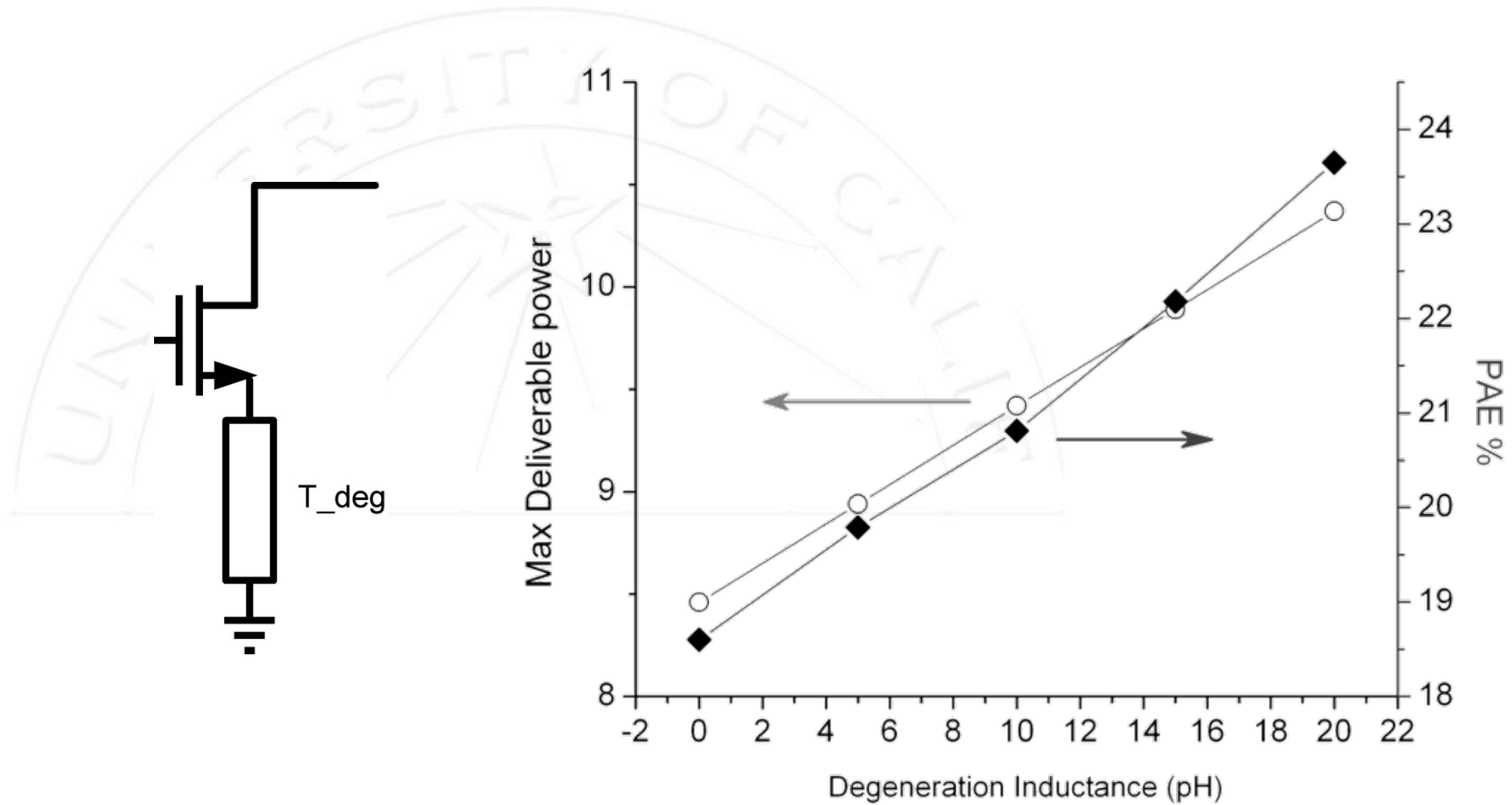
Operating Power Gain Circles, $F=60\text{GHz}$



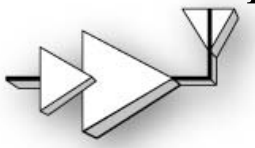
Constant $P_{1\text{dB}}$ Contours



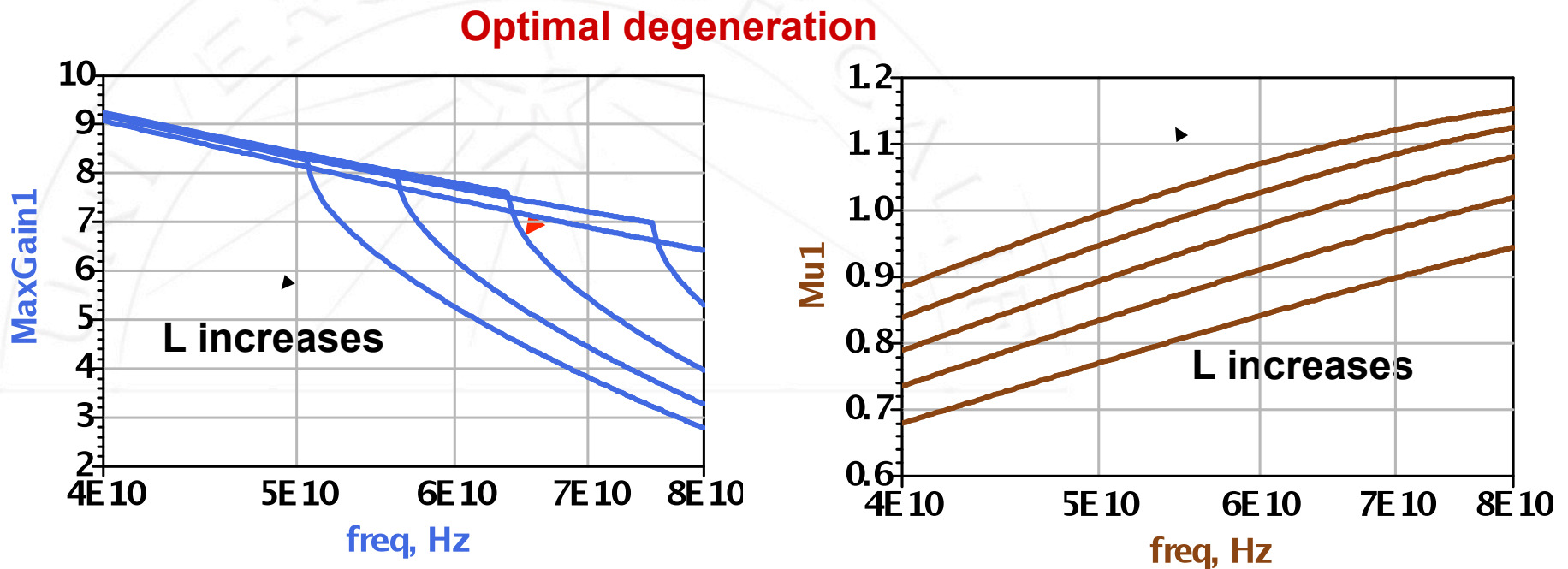
Output Stage Degeneration (I)



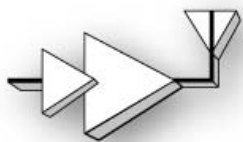
- Output power and PAE increase with small source inductive degeneration



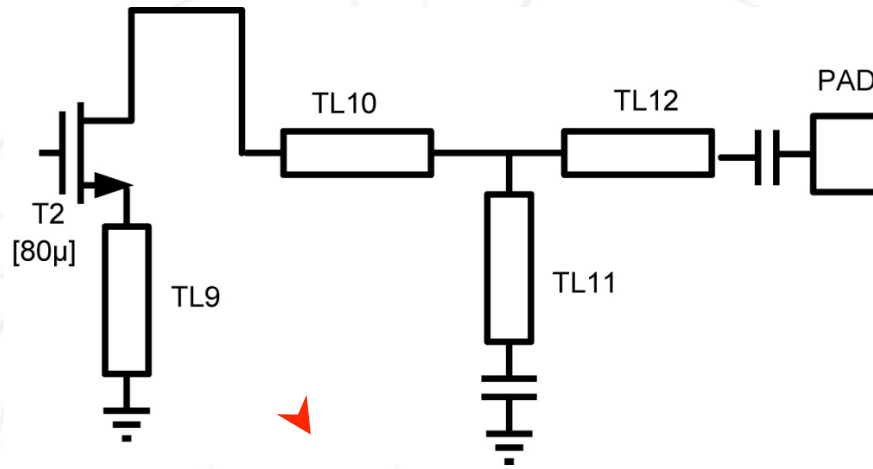
Output Stage Degeneration (II)



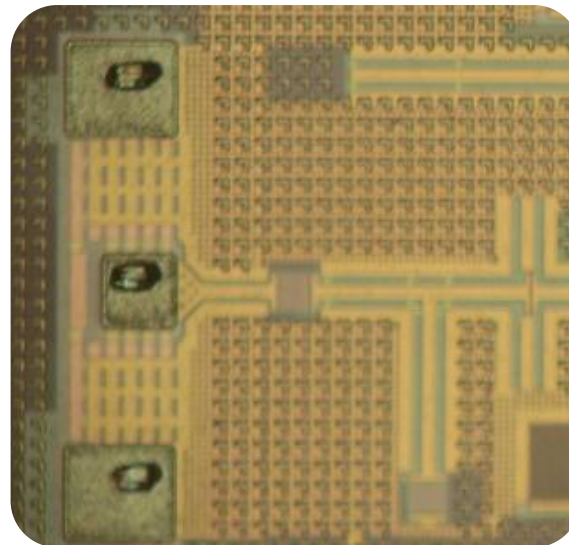
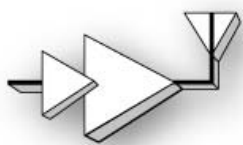
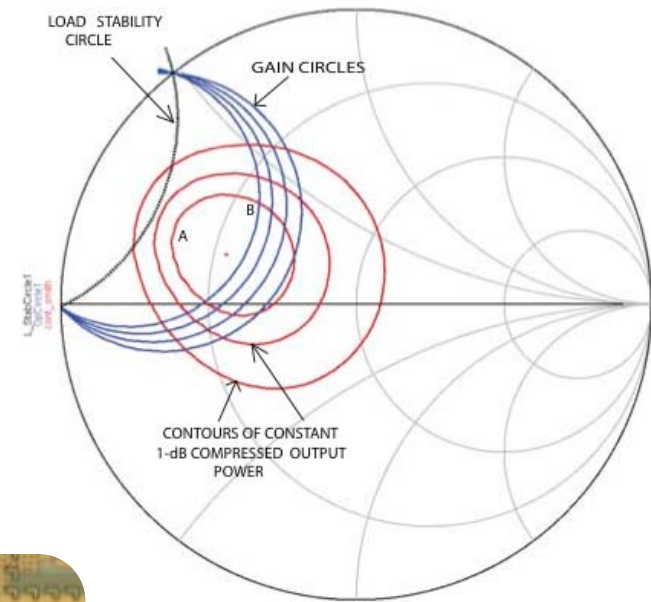
- Degeneration also increases stability, but could reduce the gain significantly!



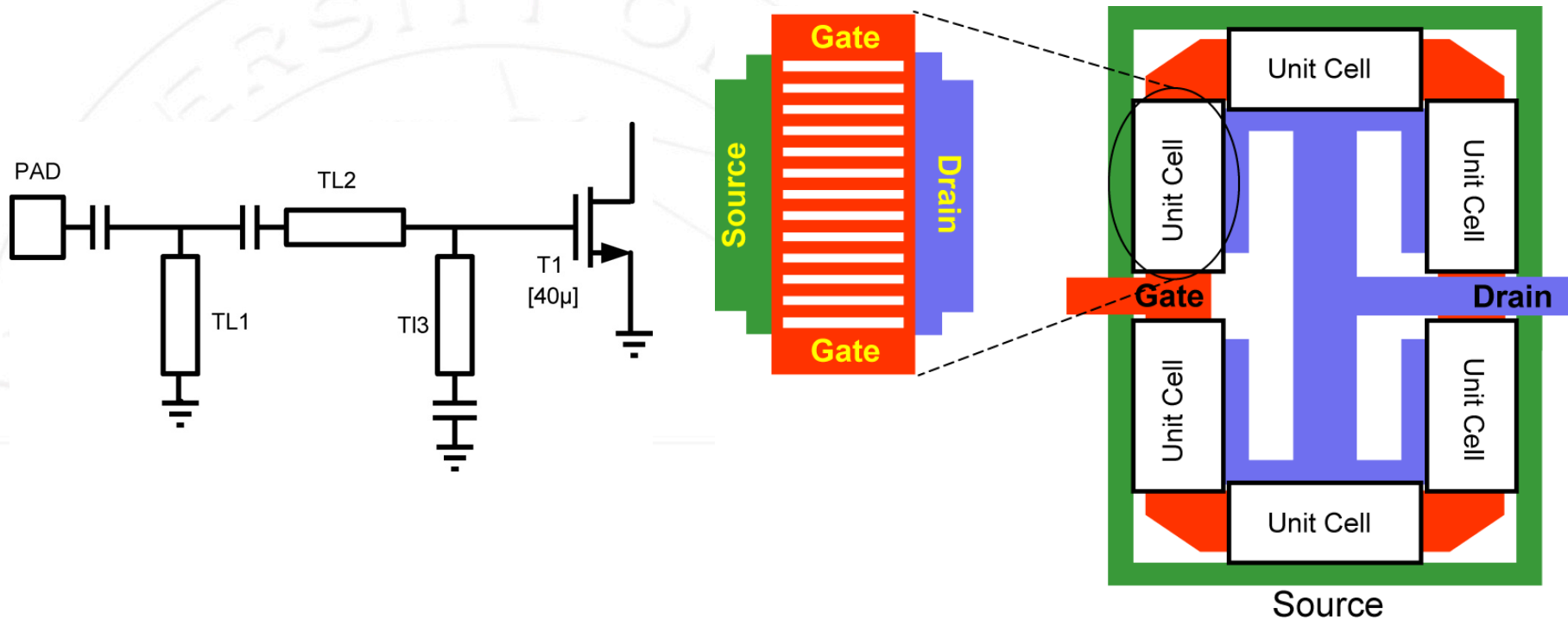
Output Stage Network



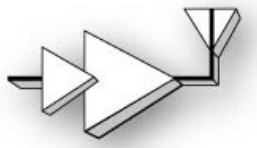
Power Device



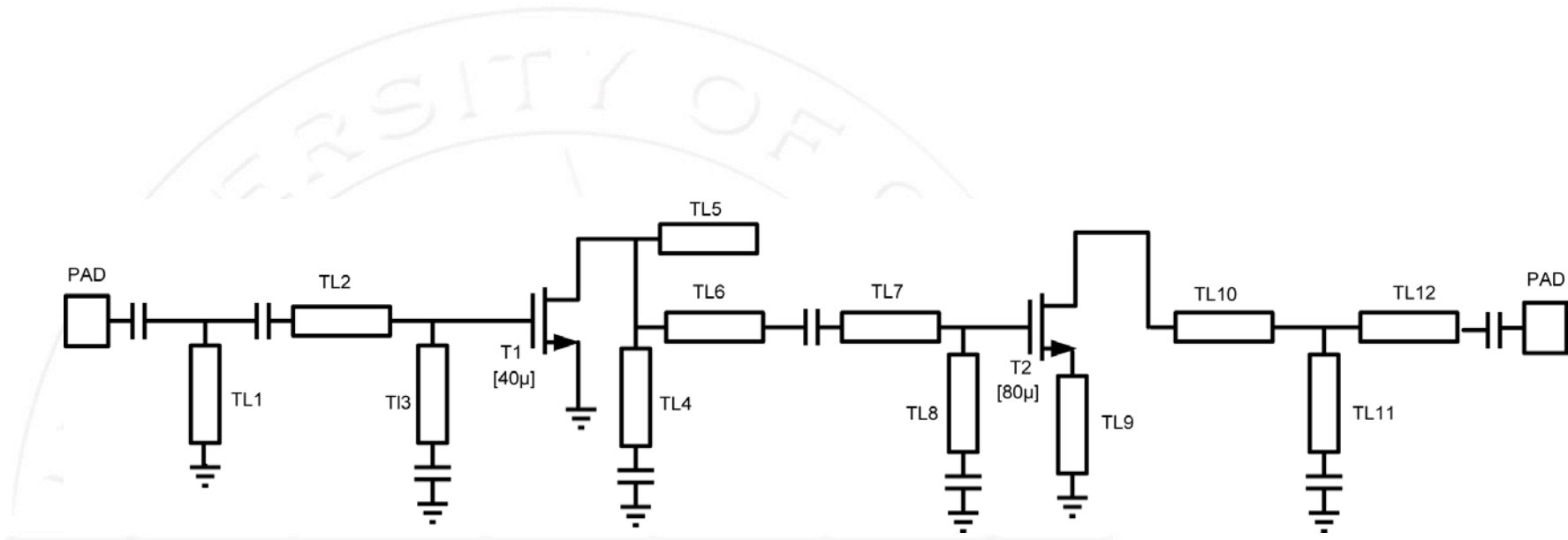
Gain Stage



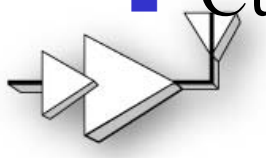
- The first Stage is optimized to give the maximum Gain
- Round-table device was used to achieve the maximum available gain (MSG=8.5dB)



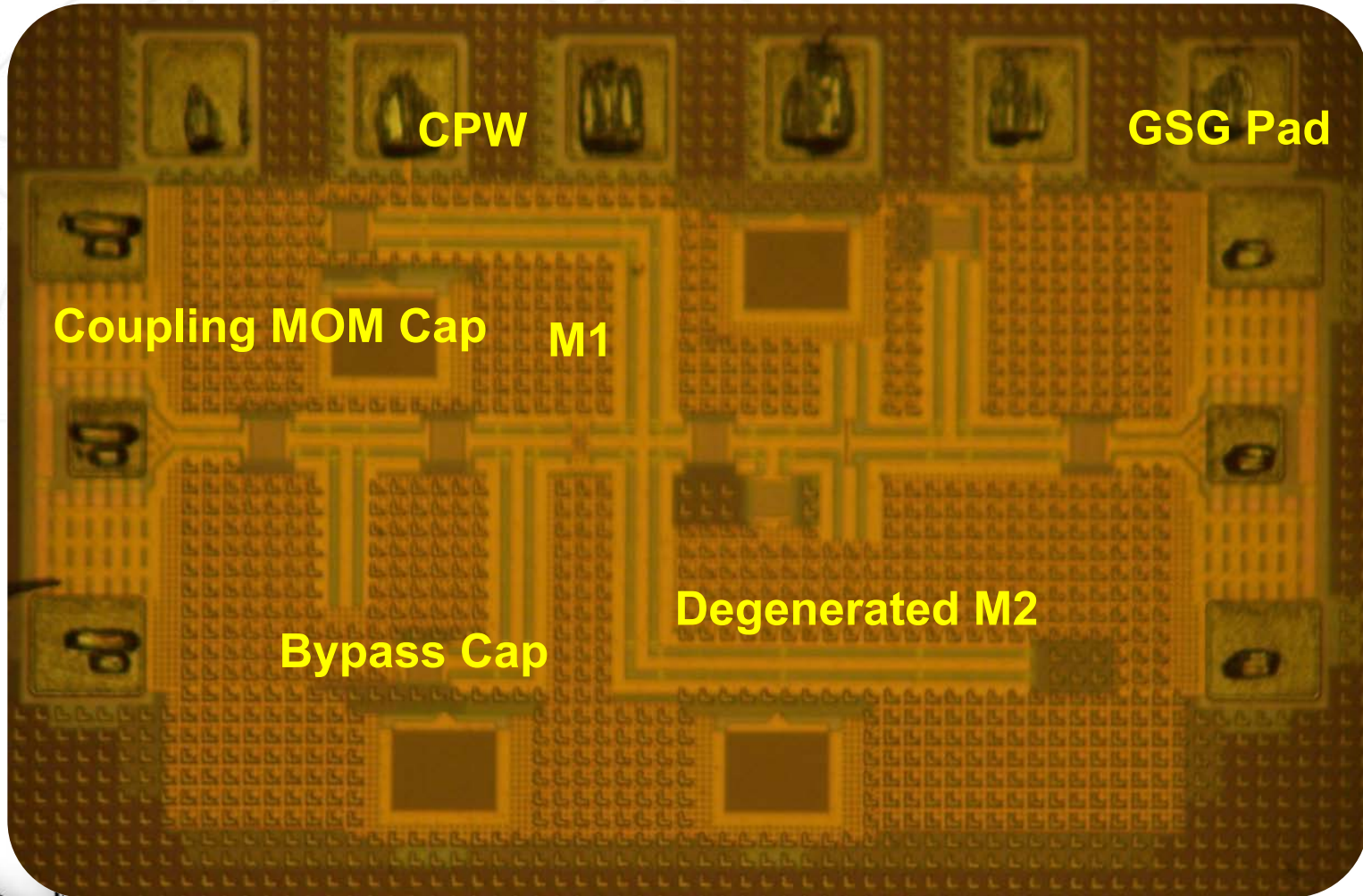
PA Schematic



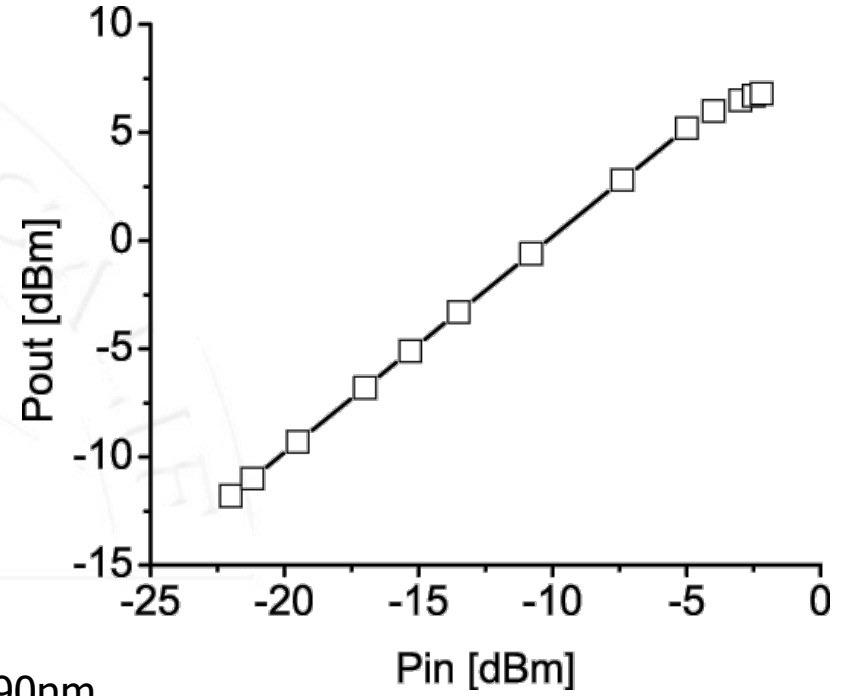
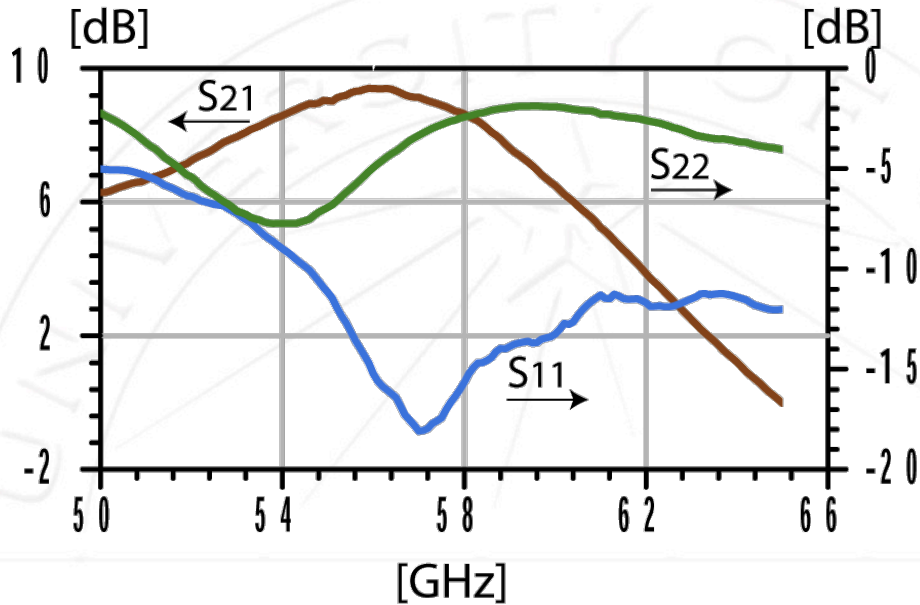
- Two-stage design single-ended design
- CPW matching, coupling caps (embedded)
- 40 μm driver, 80 μm output stage
- Custom bypass for low inductance



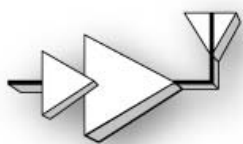
Chip Micrograph



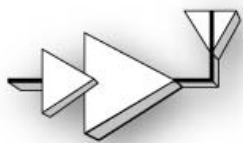
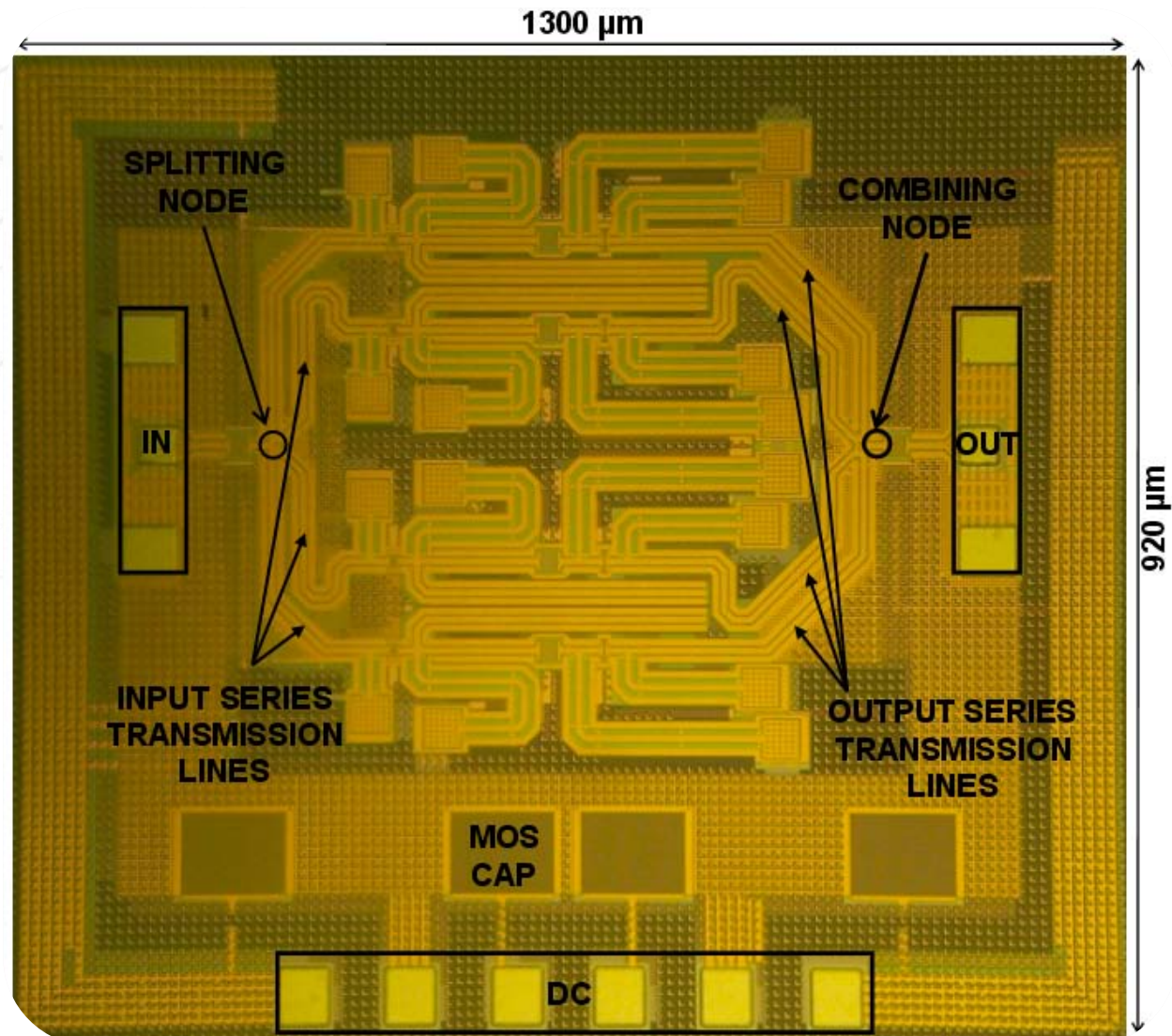
60 GHz PA Measurements



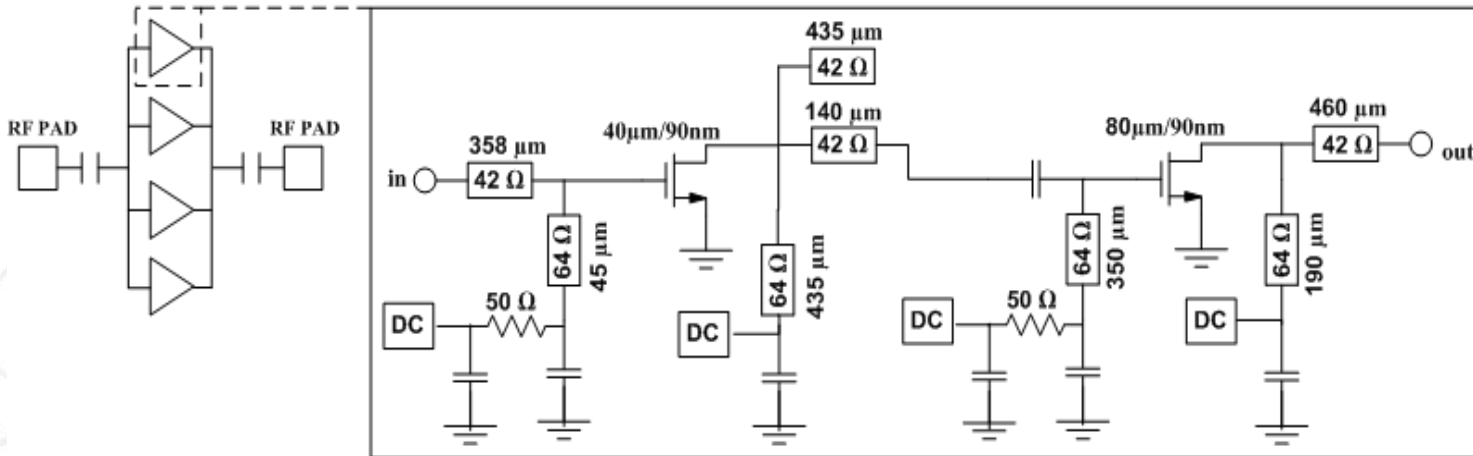
Technology	90nm CMOS (1V)
DC Power	23 mW
Gp	9.8 dB
P _{-1dB}	6.7 dBm
Efficiency	20%
S11 (57 GHz)	-18 dB



Current Combing Power Amplifier

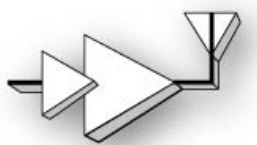


Current Combining Power Amplifier

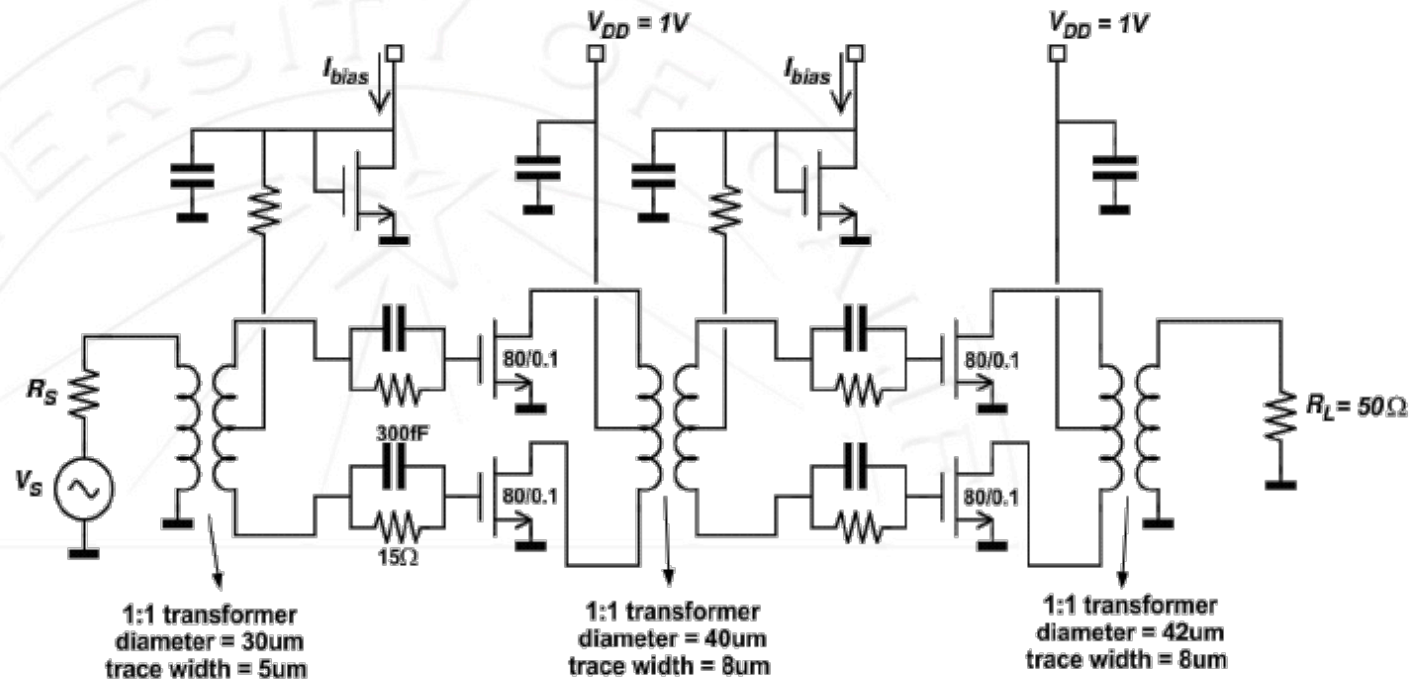


	2-Way	4-Way
Output P_{1dB}	10.1 dBm (10.5)	12.1 dBm (12.8)
Output $P_{saturation}$	11.6 dBm (12.2)	14.2 dBm (15.0)
Power Gain	8.2 dB (9.0)	4.2 dB (6.2)
1dB compression drain efficiency	12.6% (13.8%)	11.2 % (13.2)
Saturation efficiency	17.7% (20.5%)	18.1 % (20.7)
Maximum PAE	11.5% (12.5%)	5.8 % (9.8)

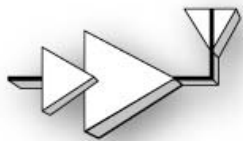
Meas (Sim)



Broadband PA

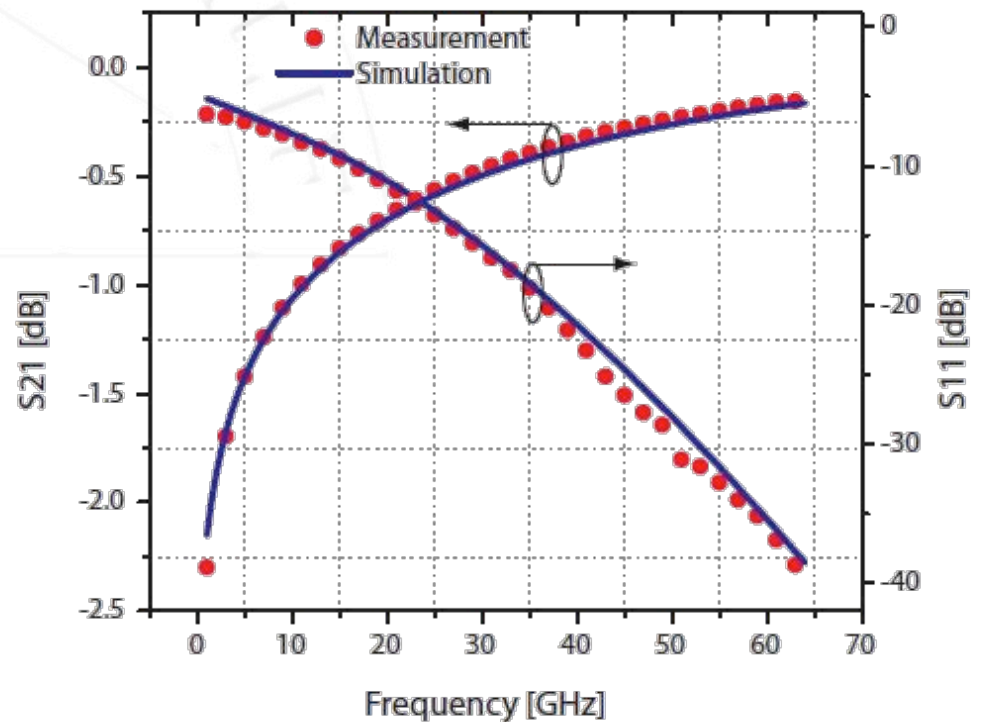
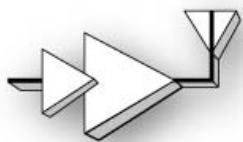
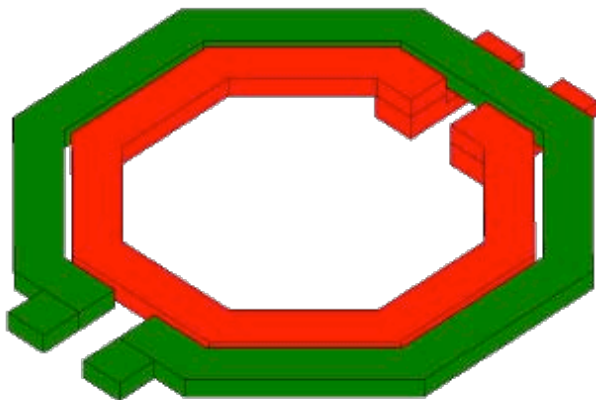


- Two-stage transformer coupled PA
- Pseudo-differential design
- Transformer used for tuning, AC coupling, and biasing

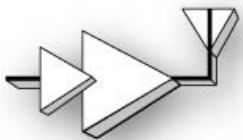
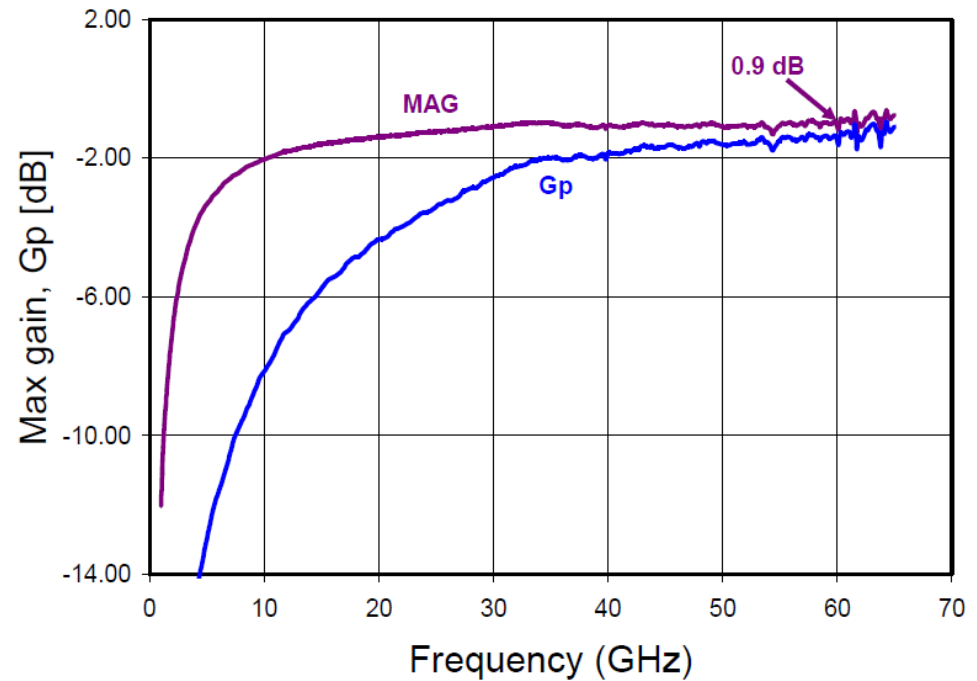
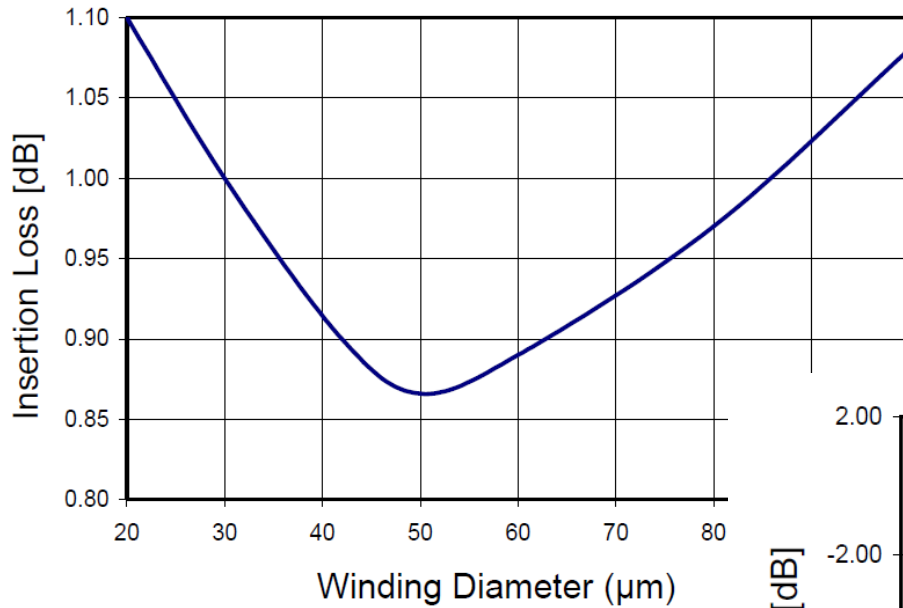


Transformers Scale to mm-Waves

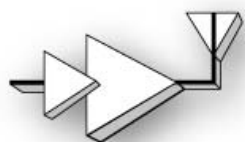
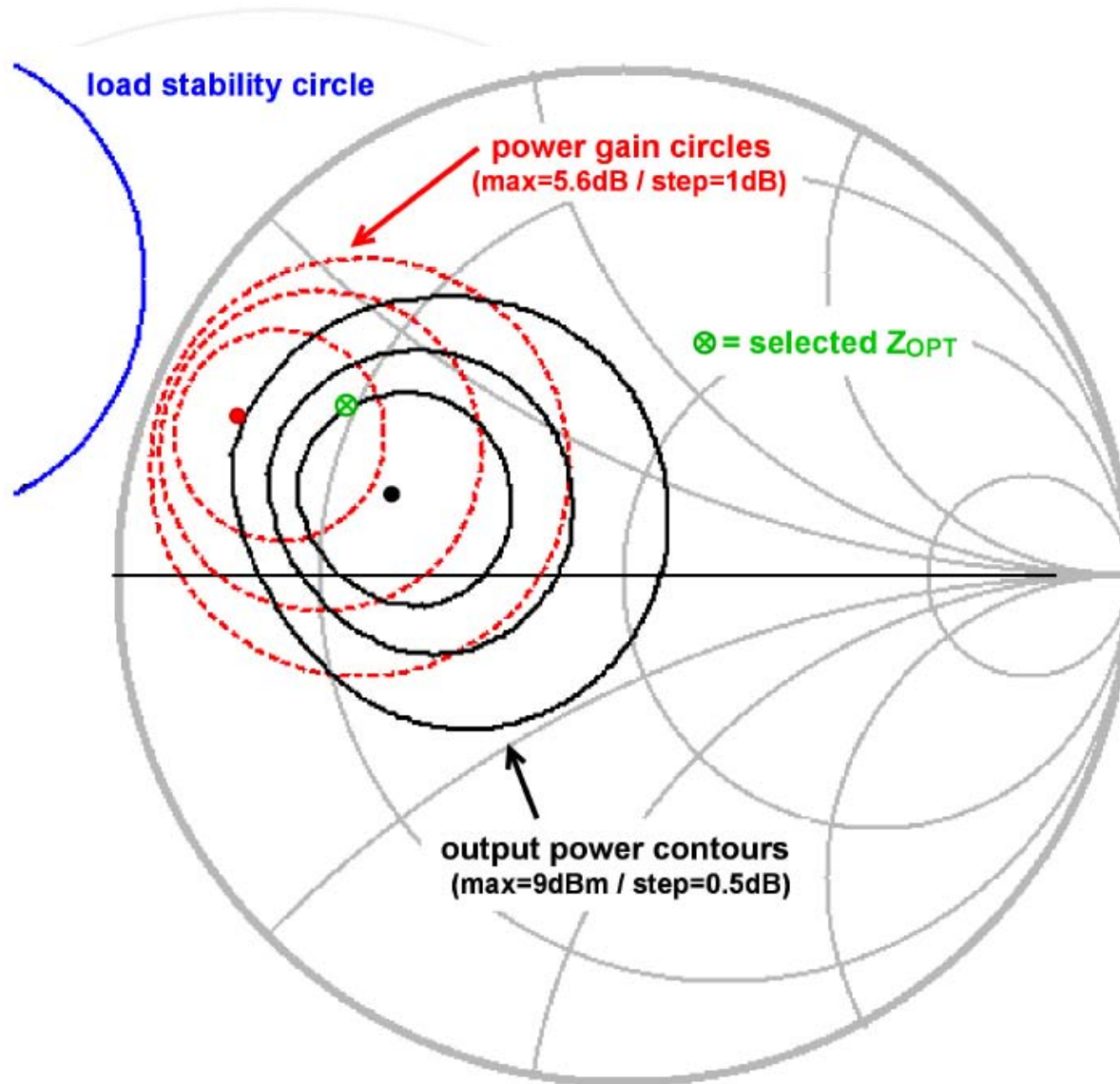
- Isolation, impedance matching, biasing ...
- Good insertion loss
- Compact layout compared to T-lines



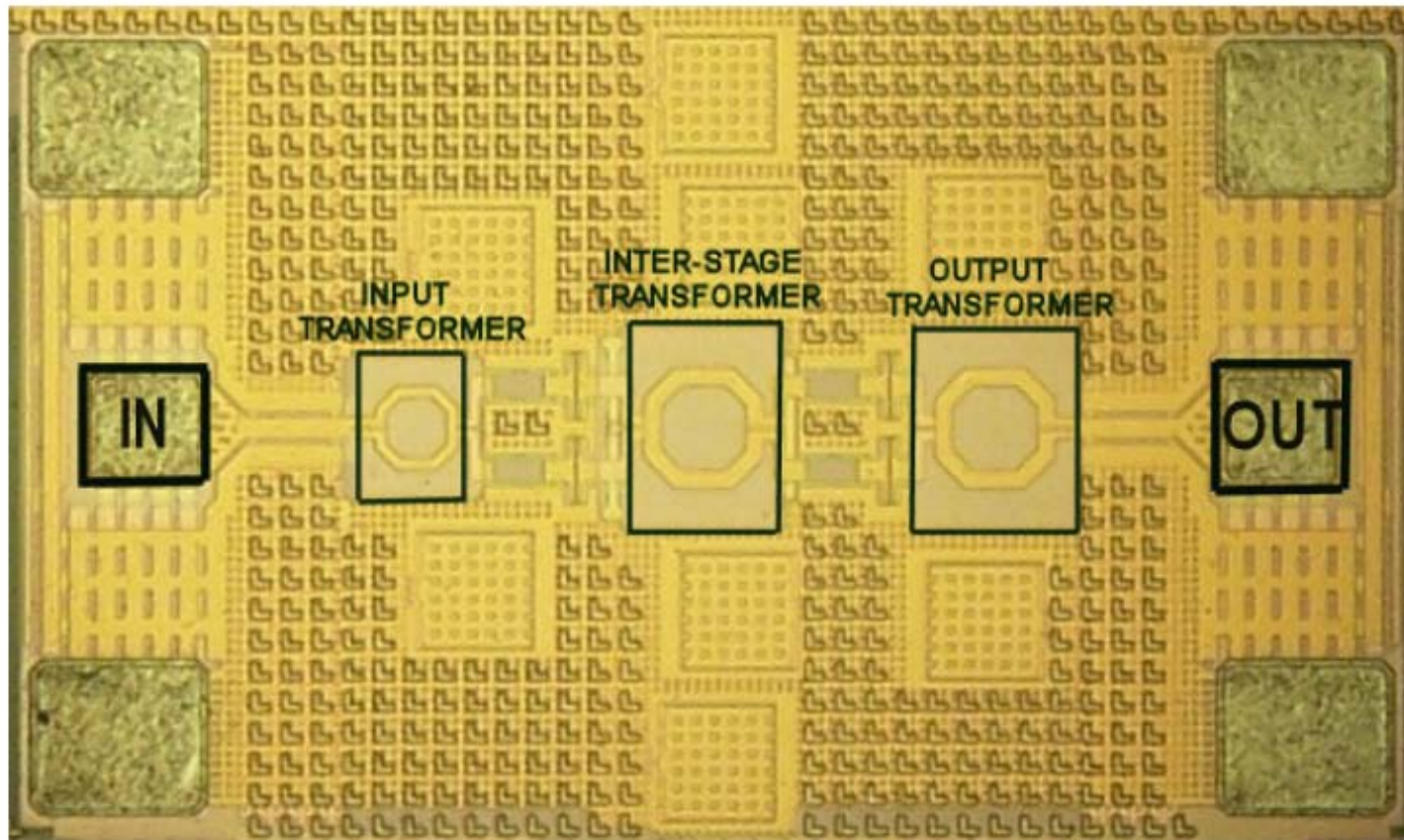
Transformer Design



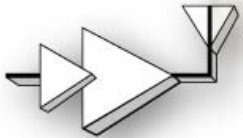
Impedance Matching



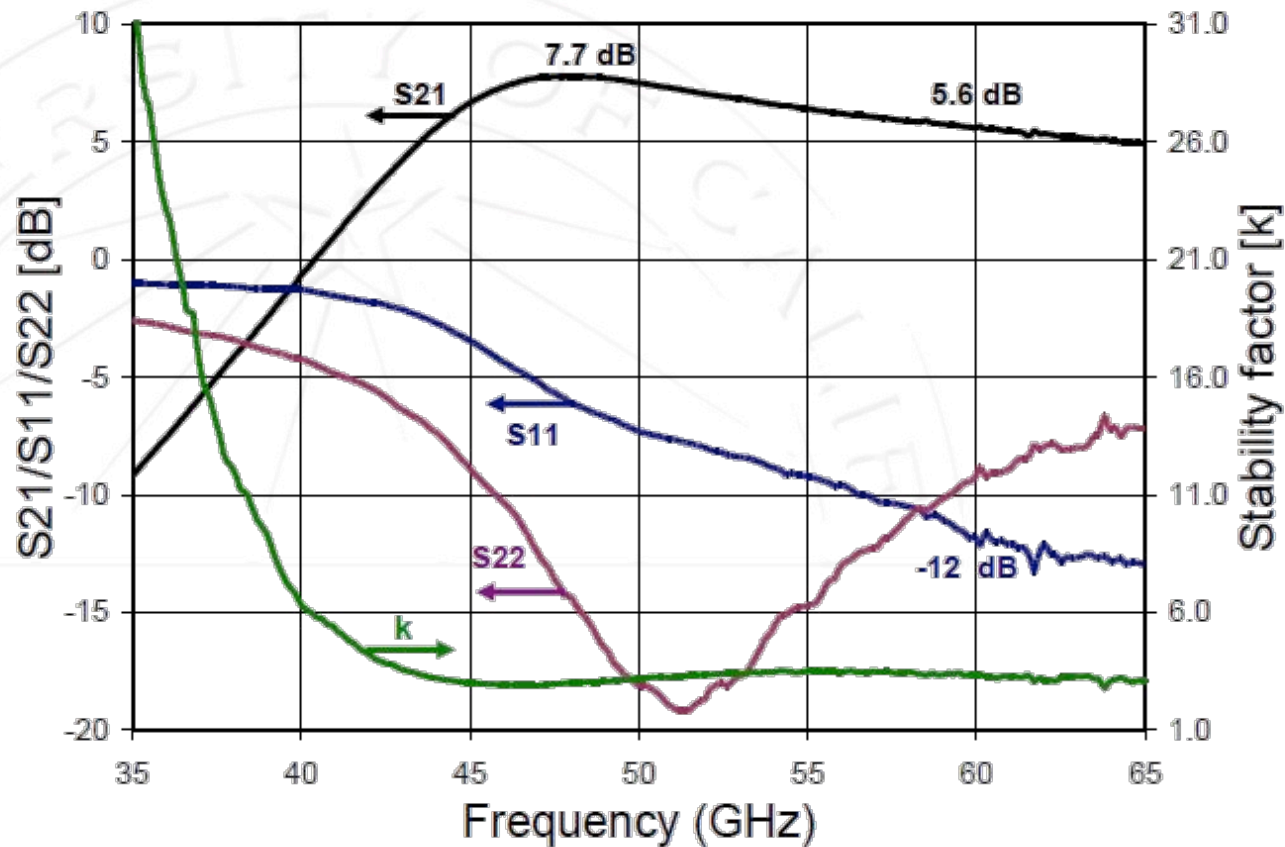
PA Die Photo



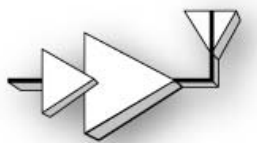
- Area: 0.25 mm^2
- Small area due to transformers



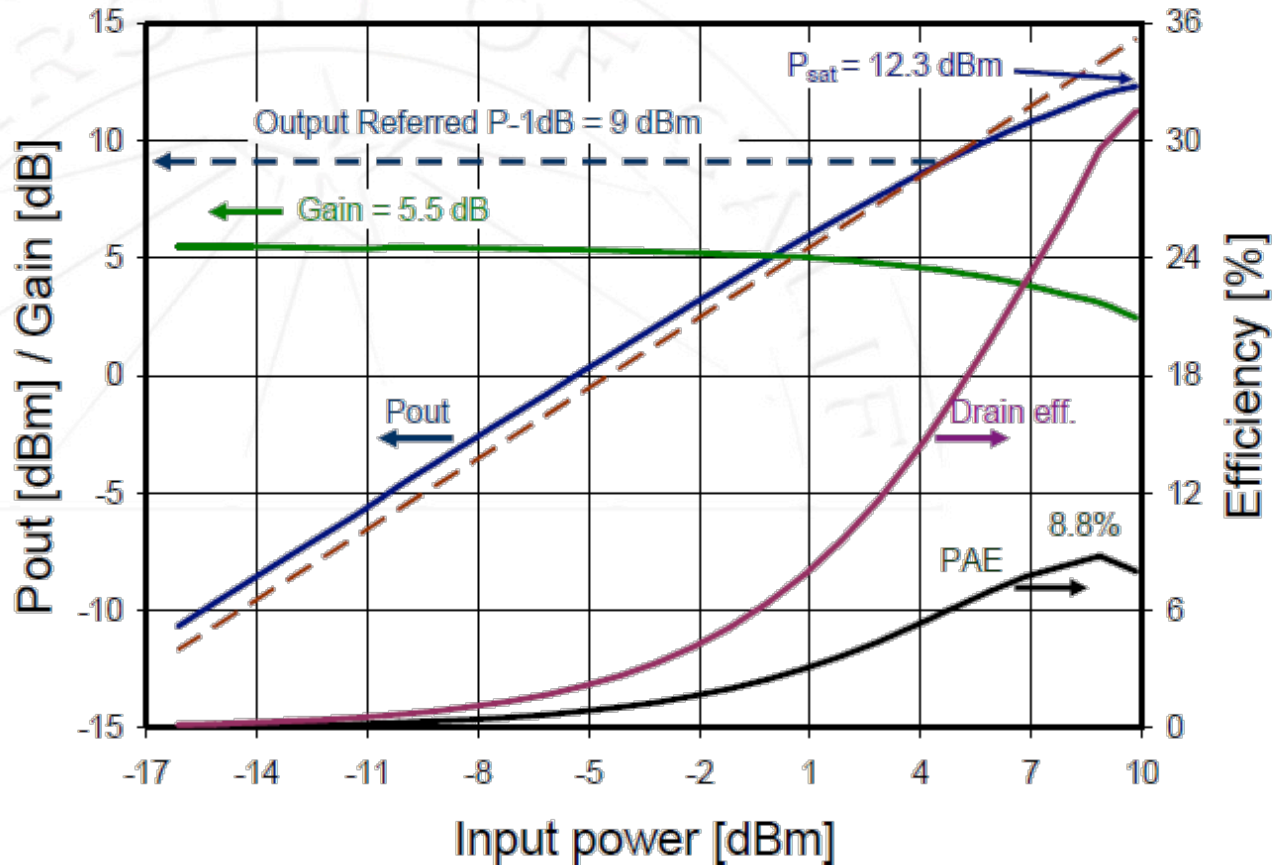
Measured S-Parameters



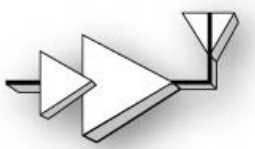
- Broadband gain (45 - 65 GHz)
- Good matching (55 - 65 GHz)
- Stable ($K > 1$)



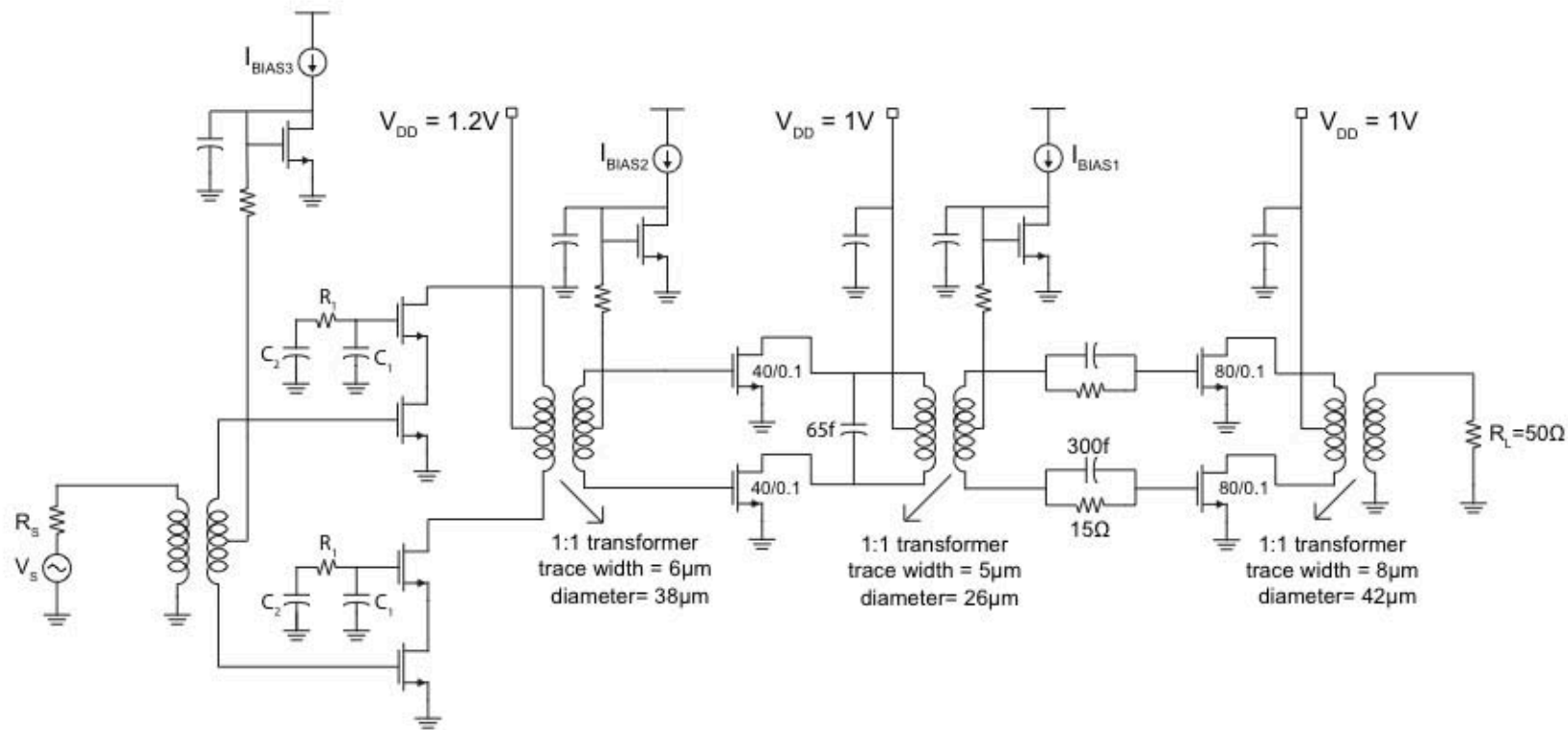
Power Measurements



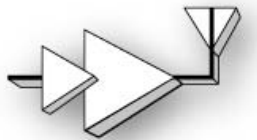
- $P_{-1dB} > 9\text{dBm}$ (up to 10dBm measured)
- $P_{\text{sat}} = 12.3\text{ dBm}$



Improved Three-Stage PA

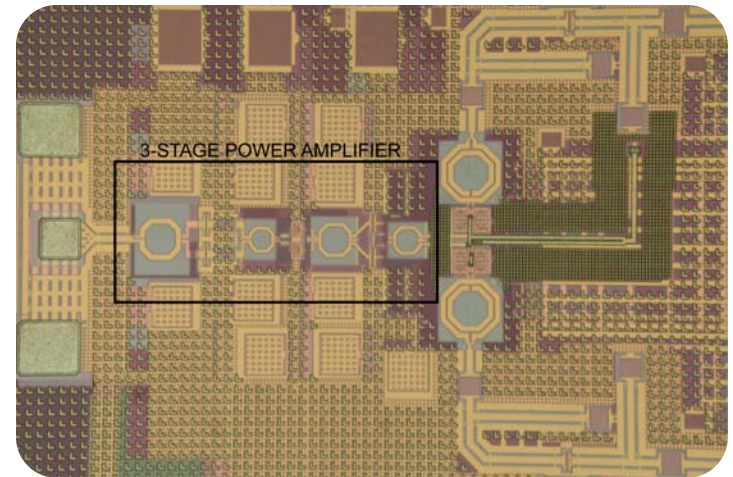
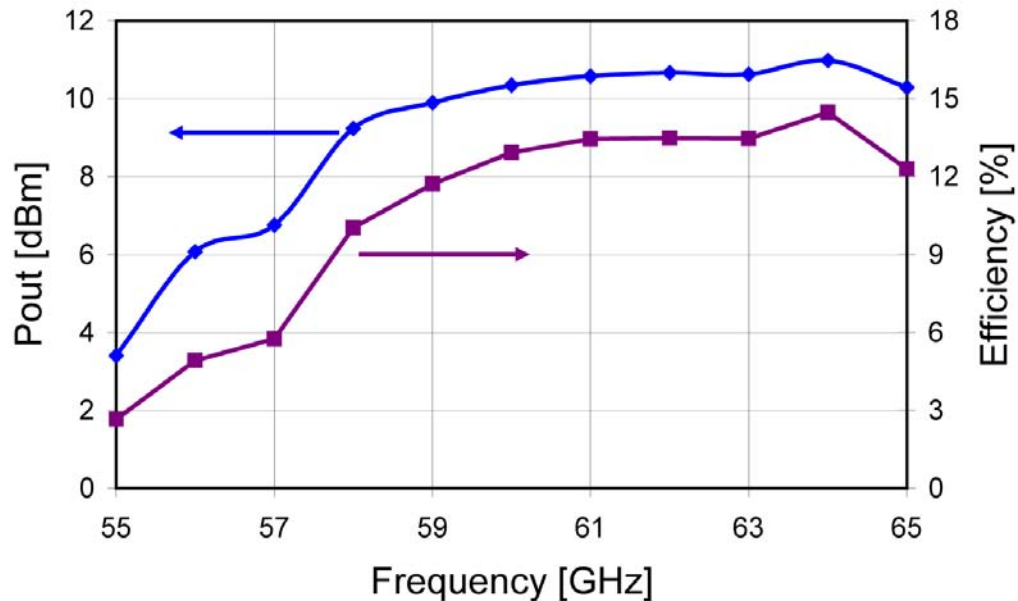


- Optimized driver stage (smaller transistors) for higher gain
- First driver stage cascode configuration for slightly higher gain and unconditional stability at 60GHz

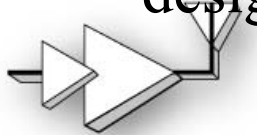


Three-Stage PA Measurements

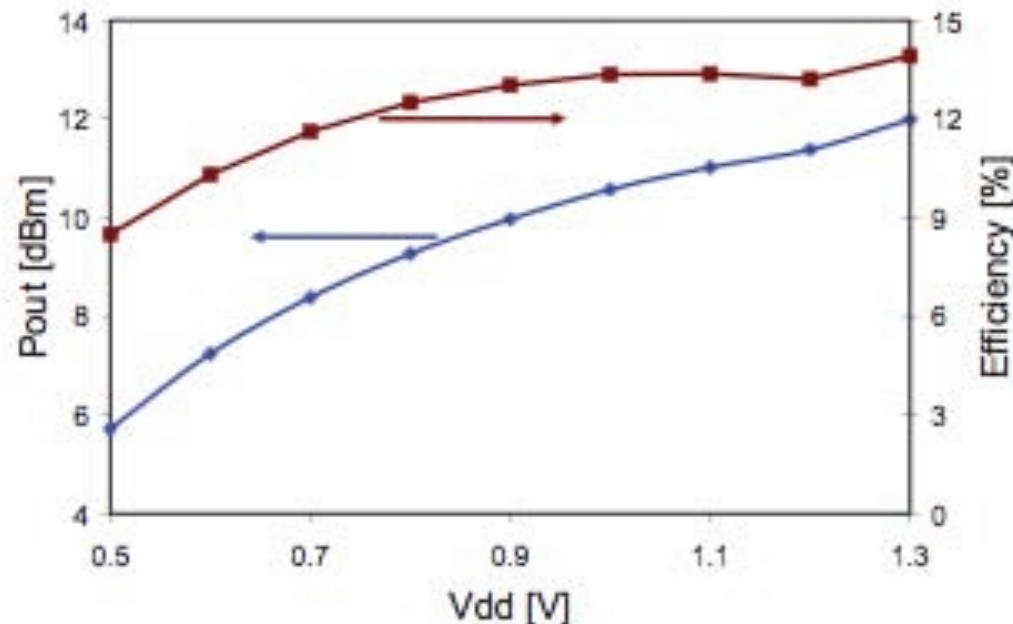
Measured Output Power vs Frequency



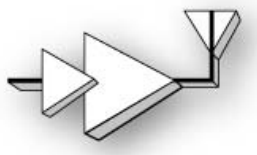
- Driver design critical since MSG at mm-wave frequency low → simultaneous gain-output power based optimization necessary
- Measured PAE close to 15% (nearly double the two-stage design) with 14dB of power gain at 60GHz



PA Output / PAE versus Supply

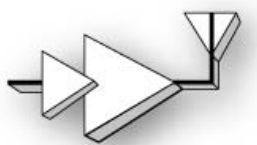


- As expected, output power increases with supply.
- Reliability is a major concern for CMOS devices. In our design we operate the CMOS PA at a lower supply voltage.

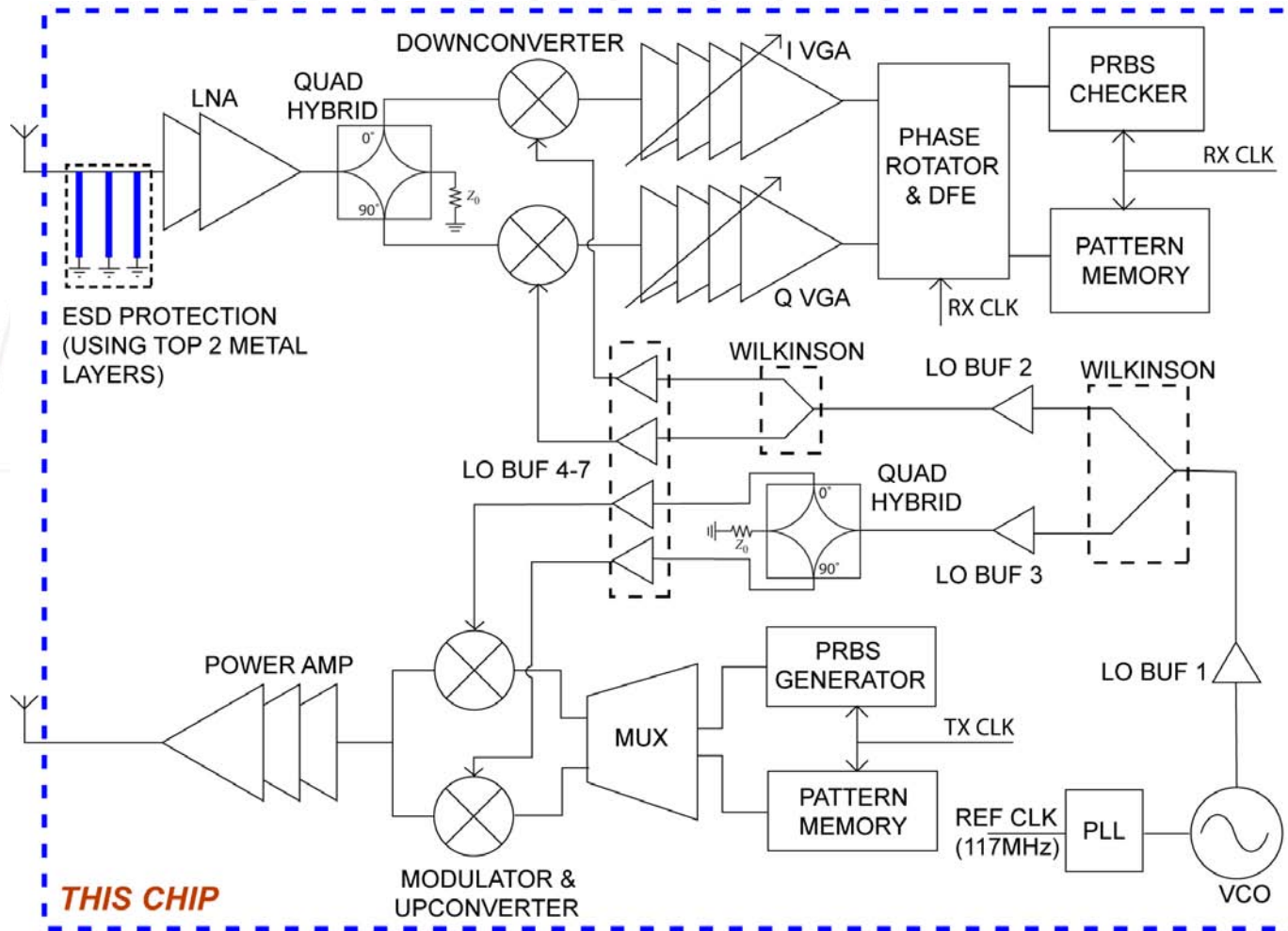




60 GHz TRANSMITTER



Transceiver Block Diagram



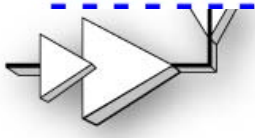
Vdd = 1.2V

~5GHz RF BW

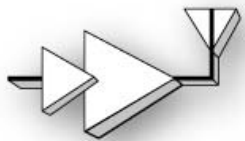
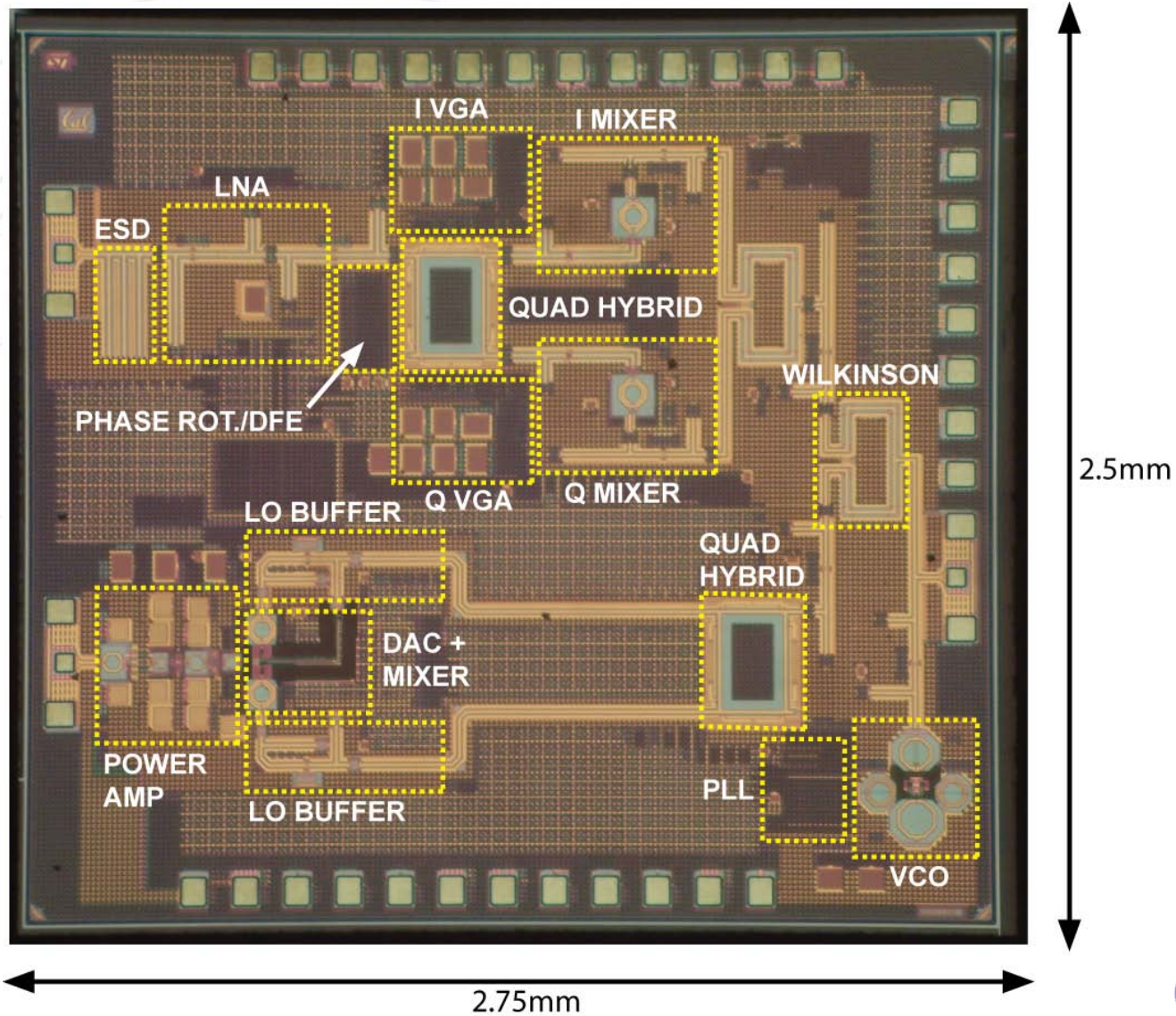
TX: 170mW

RX: 138mW

THIS CHIP

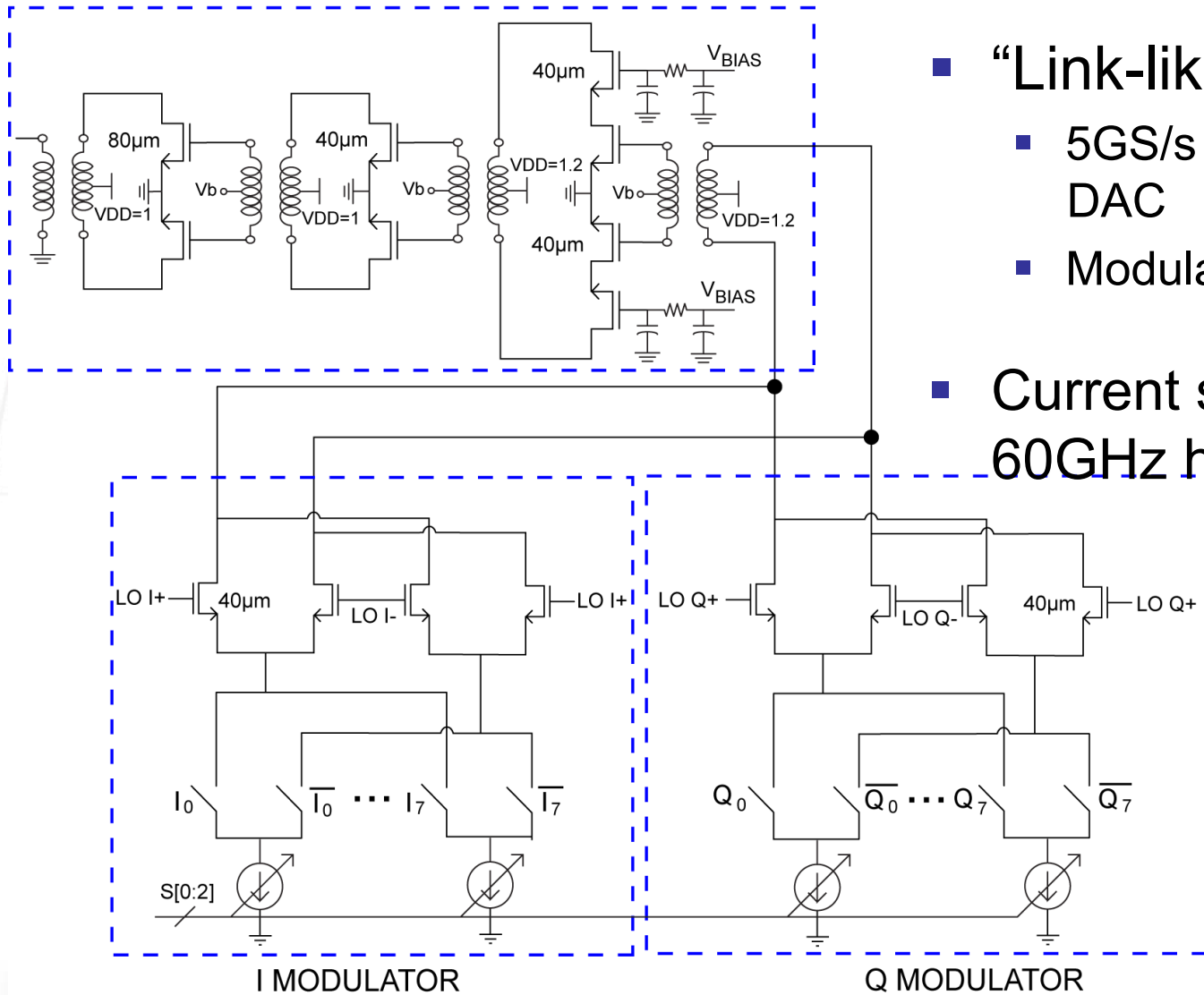


Chip Layout



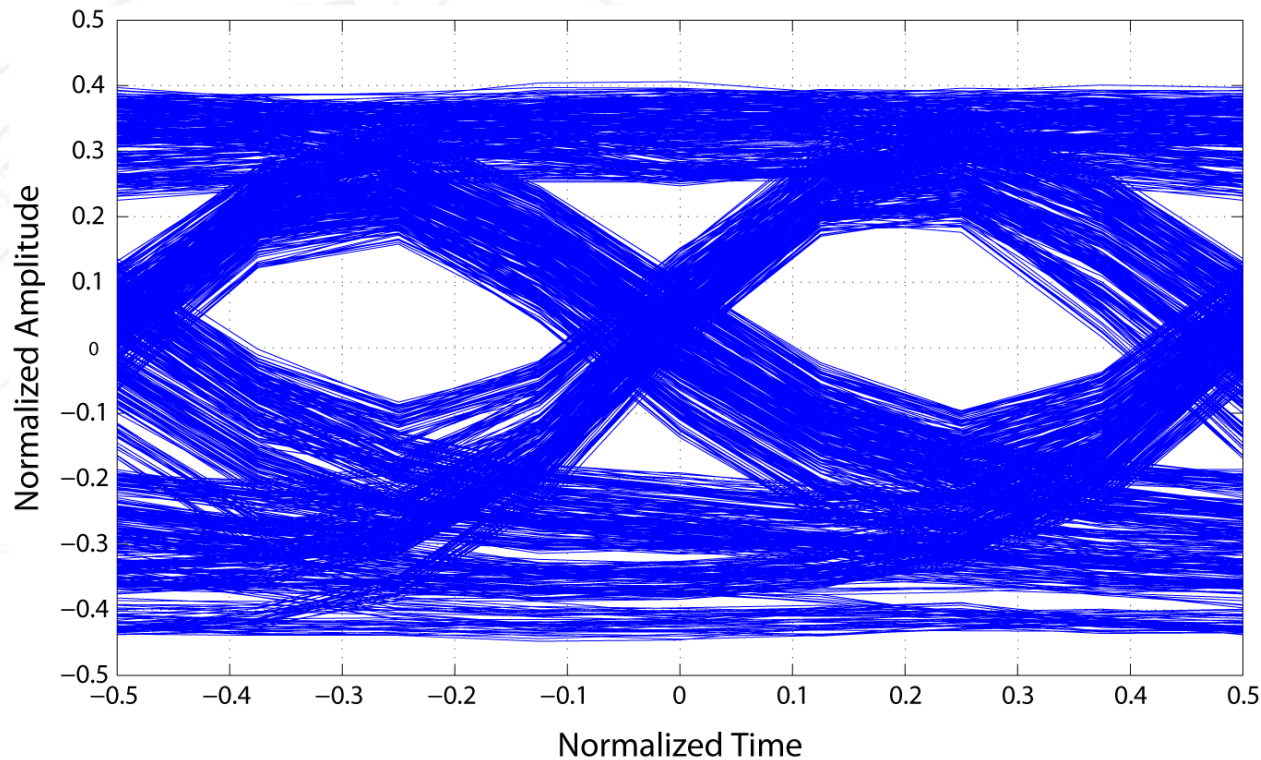
Modulator and PA

3-STAGE DIFFERENTIAL PA

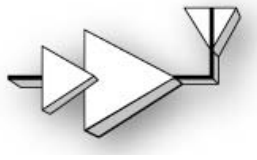


- “Link-like” TX:
 - 5GS/s 3-bit current mode DAC
 - Modulator power ~22mW
- Current summation at 60GHz hard
 - PA input needs low impedance

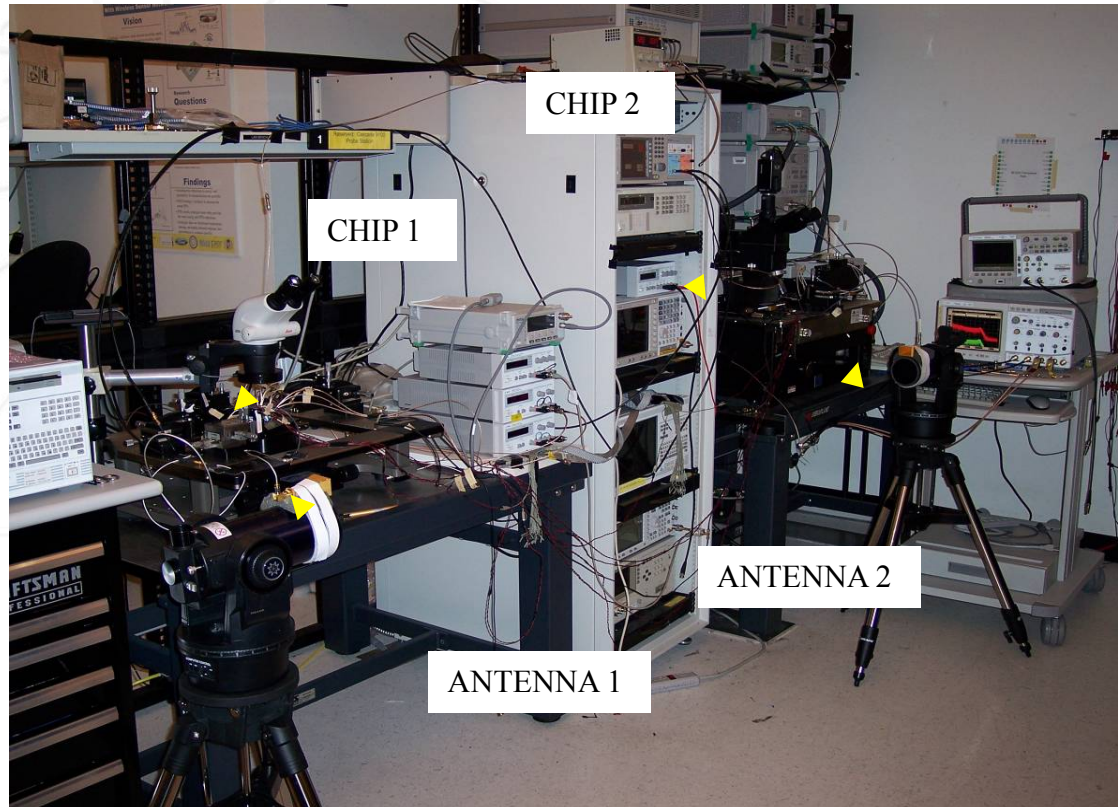
Measured Eye Diagram



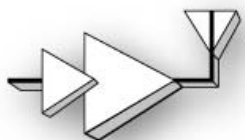
- Simulated modulator output power: -2.3dBm
 - Power from just I or Q is -1dBm → loading
- Measured PA output power: ~10dBm



Wireless Test

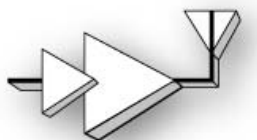


- 1m distance (+ ~2m cables), 25dBi horn antennas
- Received up to 4Gb/s at 10^{-11}



Conclusion

- CMOS device have $F_t \sim$ mm-wave range. Low voltage devices make mm-wave operation challenging.
- Optimized layout results in $F_{\max} \sim 2-3 F_t$
- CMOS power amplifiers with $P_{\text{sat}} \sim 12$ dBm can be realized in 90nm technology (1V supply). Higher power levels is challenging.
- A complete transceiver is demonstrated in 60 GHz with record energy consumption
- CMOS of tomorrow will enable dream of millions of RF/mm-wave transistors allowing EM to bits



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