Pulsed Load Modulation (PLM) 0.35μm pHEMT Power Amplifier

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Outline

- Background
- Pulsed Load Modulation (PLM)
- 2GHz PLM PA module
- Testing Results – WCDMA
- Conclusions

Background

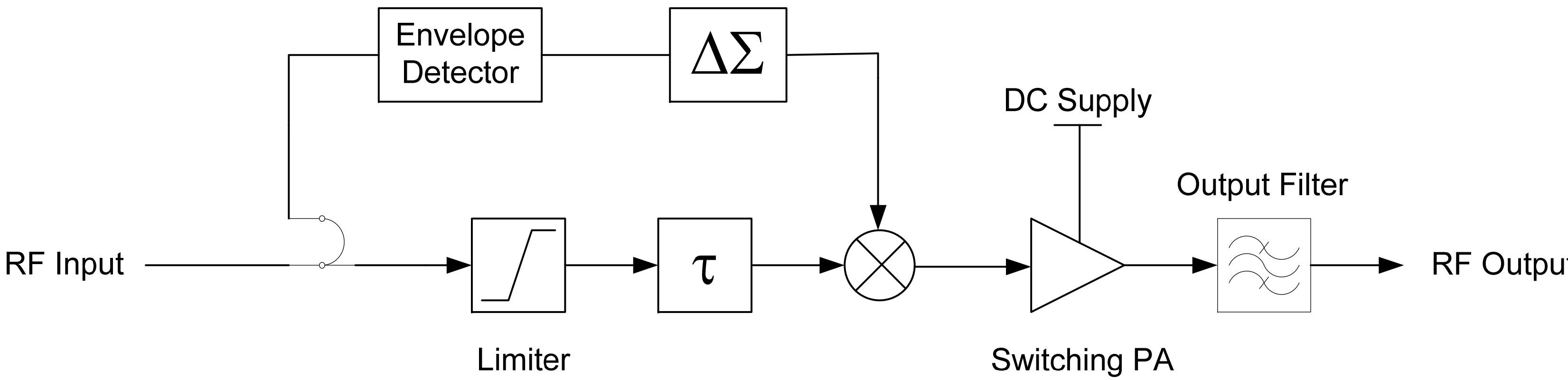
Digital RF transmitters have been envisioned in the past decade, due to their potential for

- Synthesizing and retaining digital modulations precisely
- High efficiency amplification through the use of switched mode PA

Delta-sigma modulation based transmitter architectures [Jayarama et. al. MGWL, Mar. 1998]

- Quantize the RF signals into pulses
- Amplify the pulses through switched mode amplifiers
- Restore original non-constant-envelope through a filter at the output

Envelope Delta Sigma Modulation (EDSM)

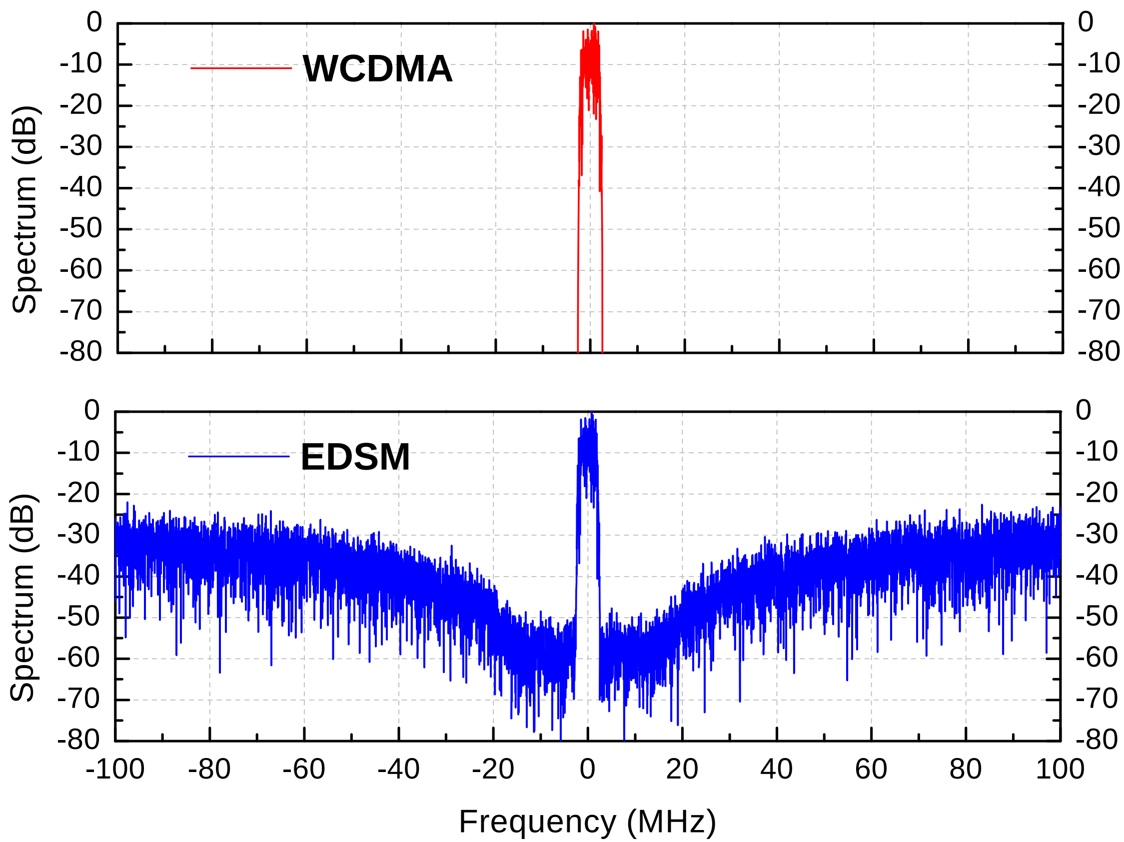


[Wang, MTT-S, June. 2003]

- Low sampling clock rate – only the envelope is oversampled
- Gate control, no large current voltage regulator
- Minimum delay mismatch between AM and PM path
- Wide bandwidth and can be scaled to millimeter wave PA

An Example for EDSM

single channel WCDMA signal (10.8dB PAR)



Sample clock rate: 495.36Mbps

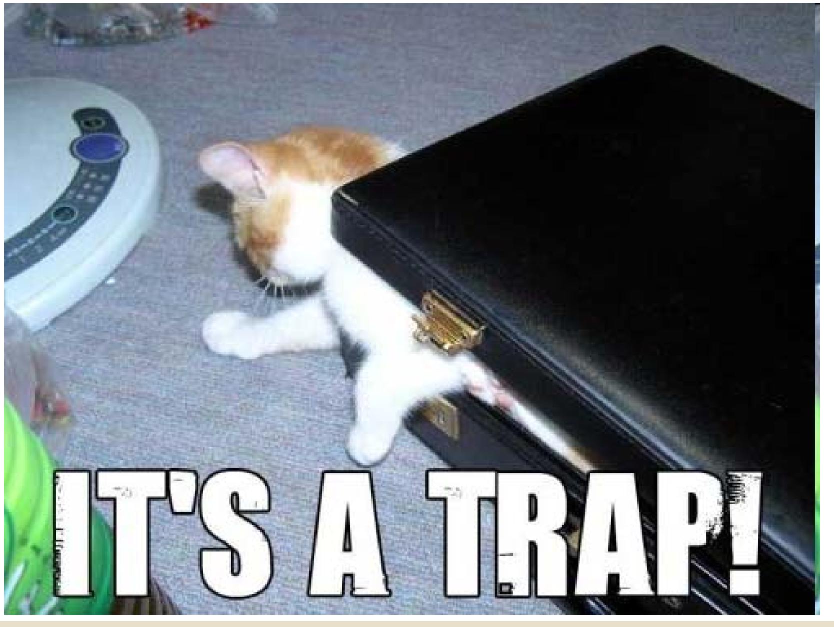
ACPR @ 5MHz: 45dBc

Noise shaping pushes quantization noise away from the signal band

Filter will be used to filter out the noise outside the 30MHz bandwidth

High Efficiency?

- High-Q Bandpass filter is needed to filter out the quantization noise
- In general, a filter with bandwidth narrower than the PA output behaves like a complex, time-varying load impedance to the PA



Efficiency for Non-Constant Envelope

For a single-ended amplifier such as a Class-B, E & F transistor drain (collector) efficiency is given by

$$\eta = \eta_{\max} \frac{V_{RF}}{V_{DC}} = \eta_{\max} \cdot \sqrt{r} \longleftarrow \text{Power backoff ratio}$$

To prevent the efficiency drop, one needs either **maintain the V_{RF}** or **decrease V_{DC}** accordingly when the output power drops

Drain (collector) modulations

(Kahn techniques, ET)

$$V_{DC} = V_{RF}$$

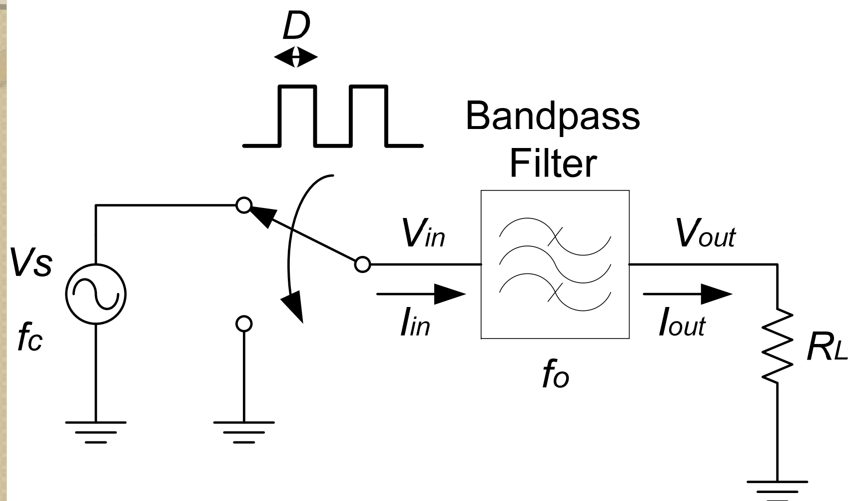
Load modulations

(Doherty's, Chireix's outphasing)

$$R_L = R_{opt} / r$$

Pulsed Load Modulation (PLM)

Switched resonator [Kim et. al., TCAS I, 2006]



Assumptions

switching rate >> bandwidth of filter

Current filter (series type) ➔ $I_{in} = I_{out}$

voltage amplitude of RF source = V_o

resonance frequency, $f_o = f_c$

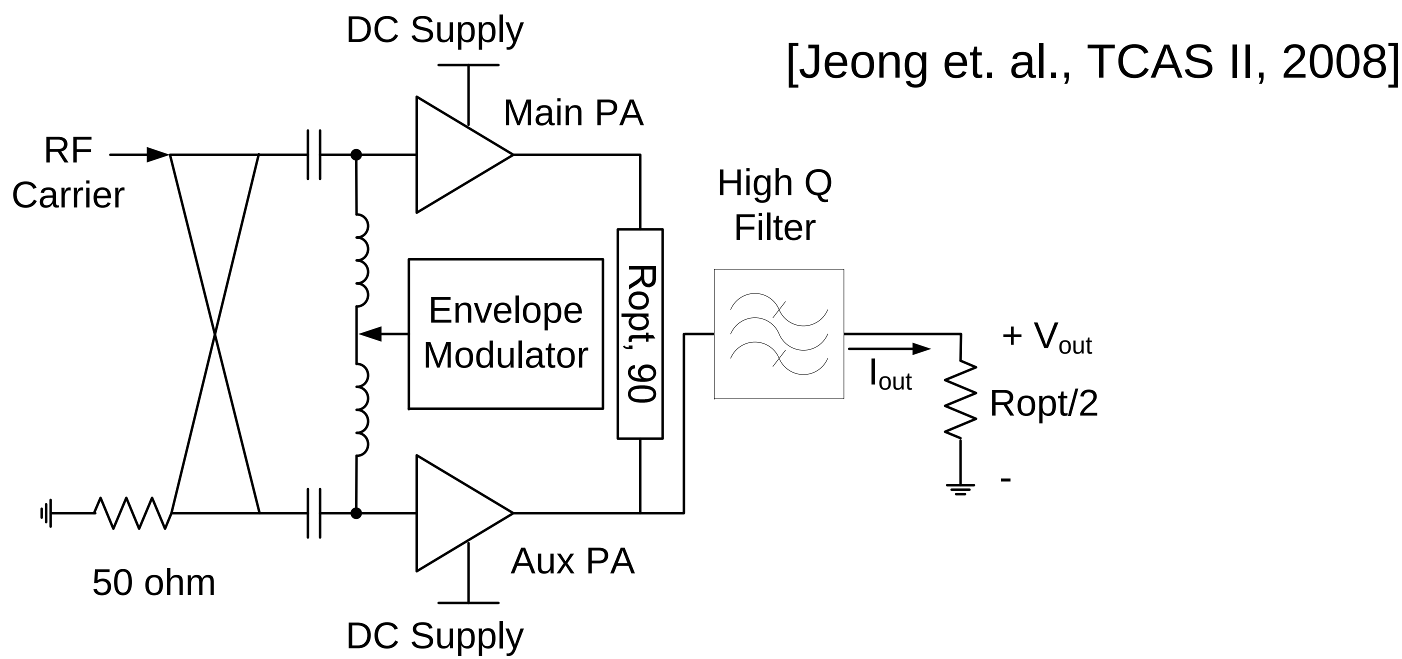
$$R_{eff} = \frac{1}{\sqrt{r}} R_L = \frac{1}{D} \cdot R_L$$

Duty cycle

Power back off ratio

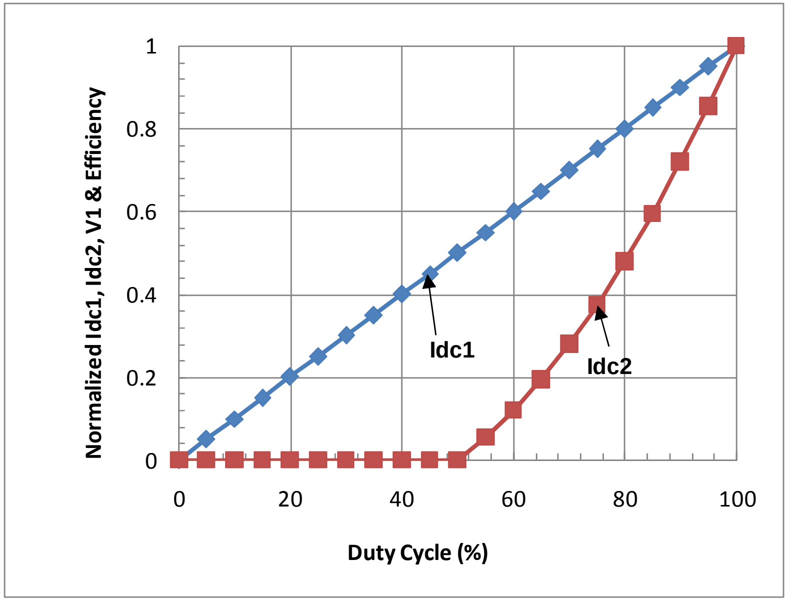
The optimum load modulation characteristics is obtained !!!

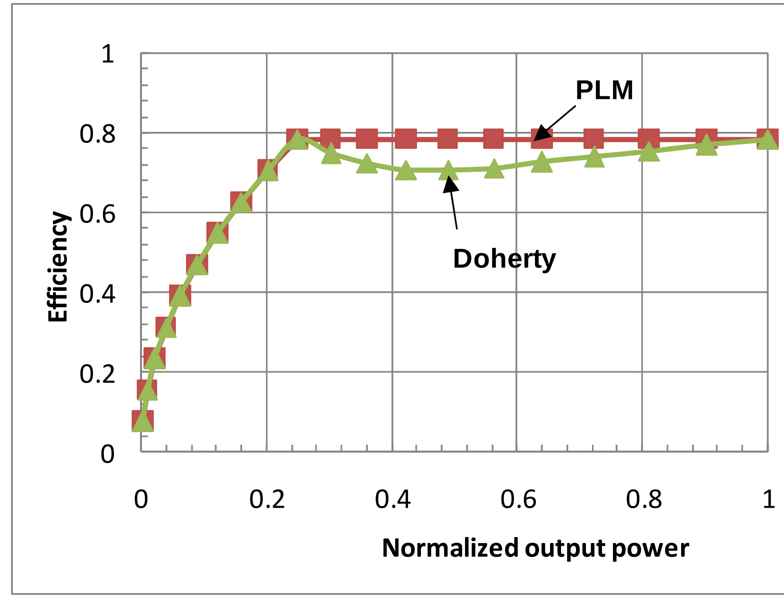
A Practical Implementation of PLM



- Balanced amplifier to simplify input matching
- Both PAs are controlled by the same envelope modulator
- ***on-state*** **:** Both PAs remain saturated until 6 dB back off
- ***off-state*** **:** Output impedance of Main PA transformed to RF short

Theoretical Efficiency vs. Output Power

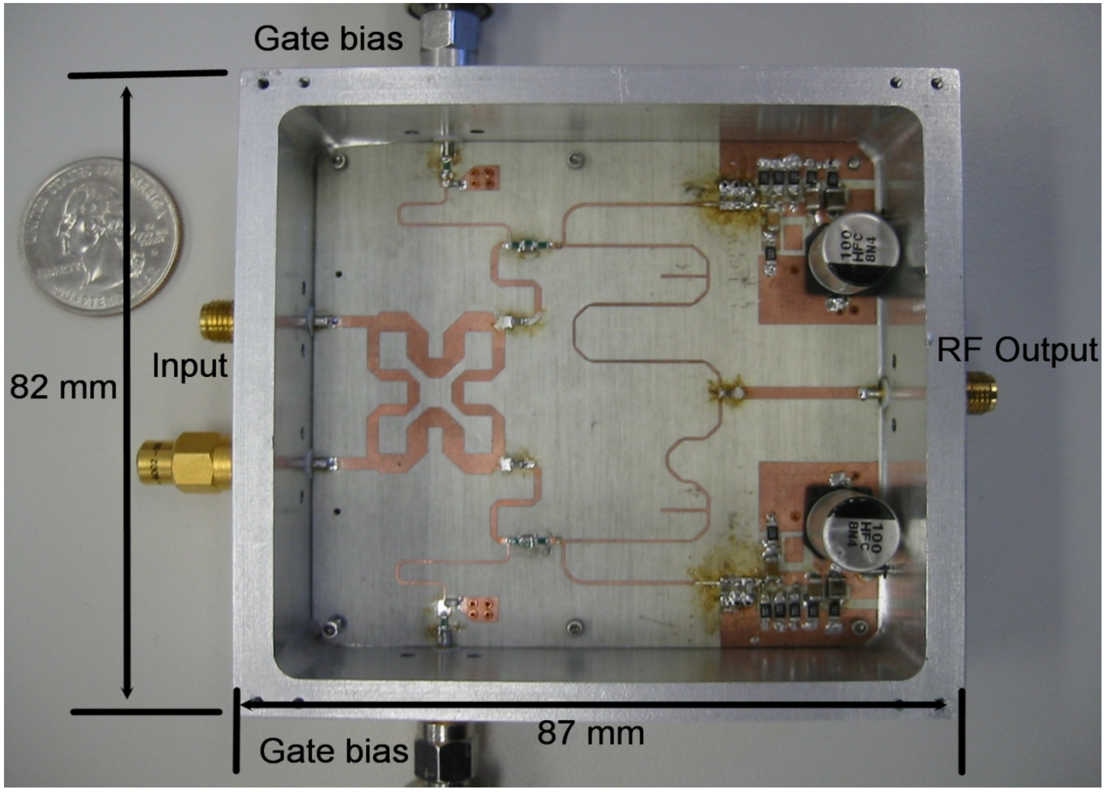




1. I_{dc1} linearly proportional to duty cycle
2. I_{dc2} decreases to 0 when D=0.5
3. Both transistor remain in saturation when 0.5<D<1
4. Efficiency remain constant until D=0.5

1.9GHz PLM Amplifier Module

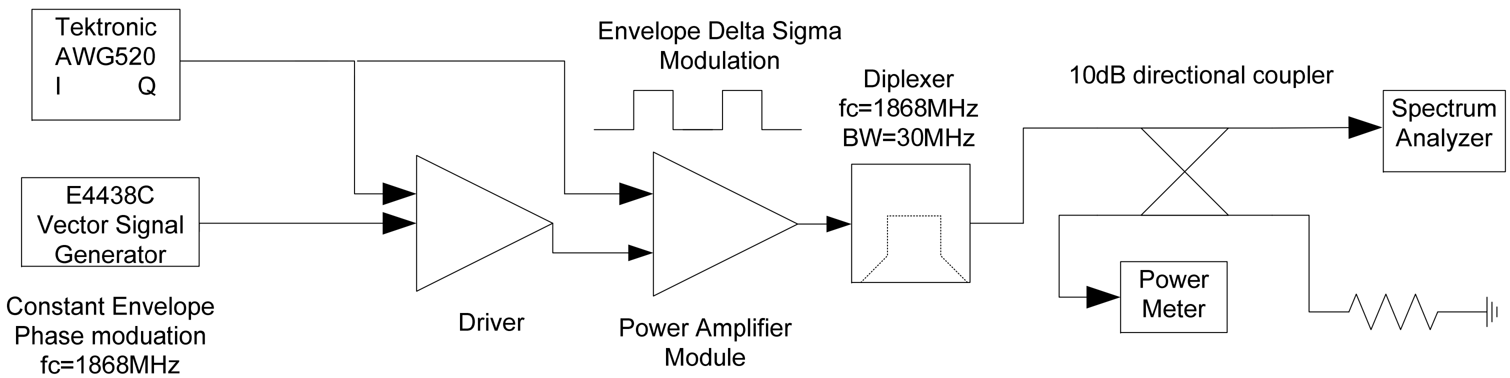
Made of a pair of 0.35um pHEMT devices from Triquint



Measurement Setup

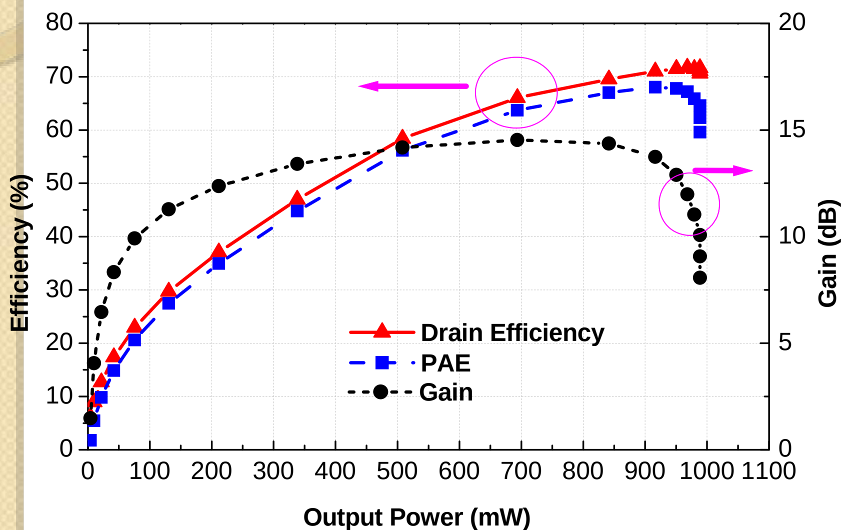
•CW test:
1.Drain Efficiency, PAE and Gain measurement without filter
2.Class B mode bias

•Duty cycle test:
1.Power amplifier module with Diplexer as high Q filter
2.Biased at Class B mode
3.10%~100% Duty cycle with different oversampling clock rate
4.Drain efficiency comparison to ideal Class B mode



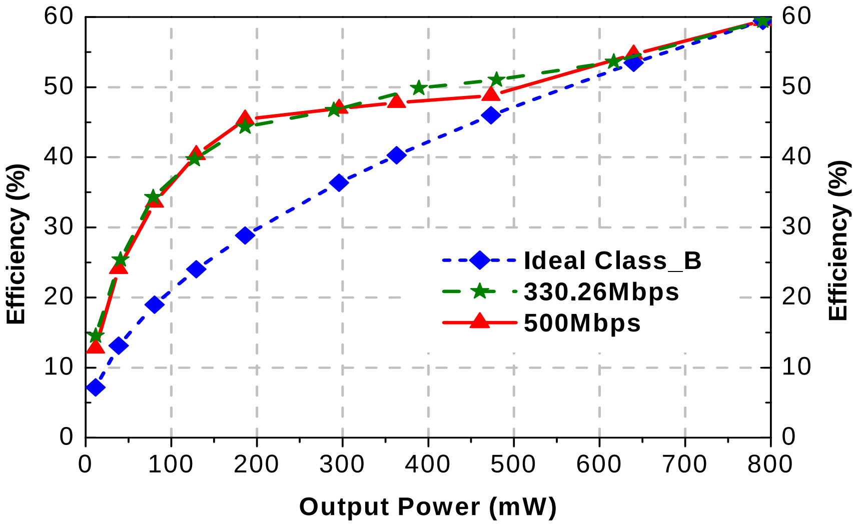
Test Results

CW Test



Maximum Drain Efficiency: 71%
Output power : 29.62dBm
Gain: 13.74dB

Duty Cycle Test



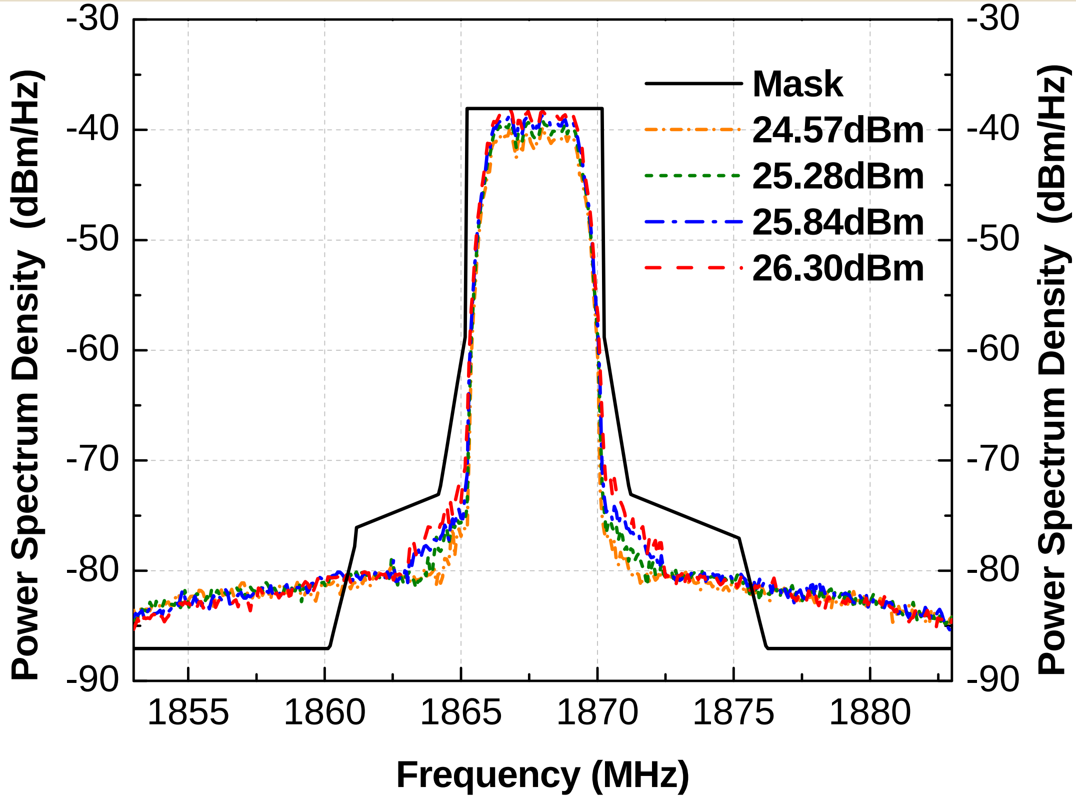
Maximum Drain Efficiency:59.5%
Output power : 29dBm
Gain:12.1dB

0.8dB filter loss is included !

Test of WCDMA Modulations

- A single channel WCDMA signal without PAR reduction is used (PAR=10.8dB) as the testing signal
- Envelop and phase modulation is separated in software
- DSM is applied to the envelop signal in software, output is transferred to the AWG digital outputs
- Output power is varied by adjusting the input of DSM, not the output of AWG or the carrier power input to the PA
- IQ components of phase modulations are sent the analogue outputs of AWG and then modulated on the carrier through the VSG

WCDMA Test Results



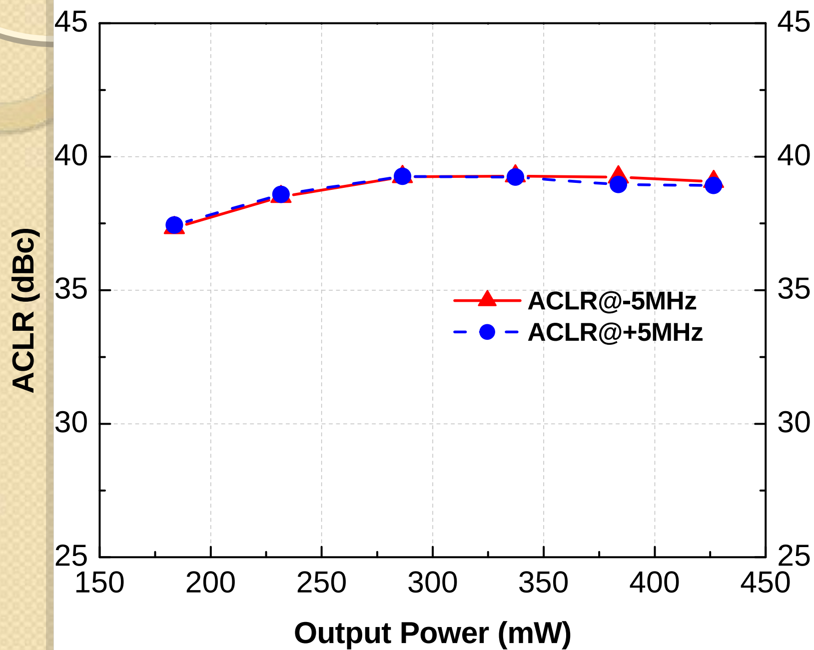
Quantization noise removed by filter to restore linearity

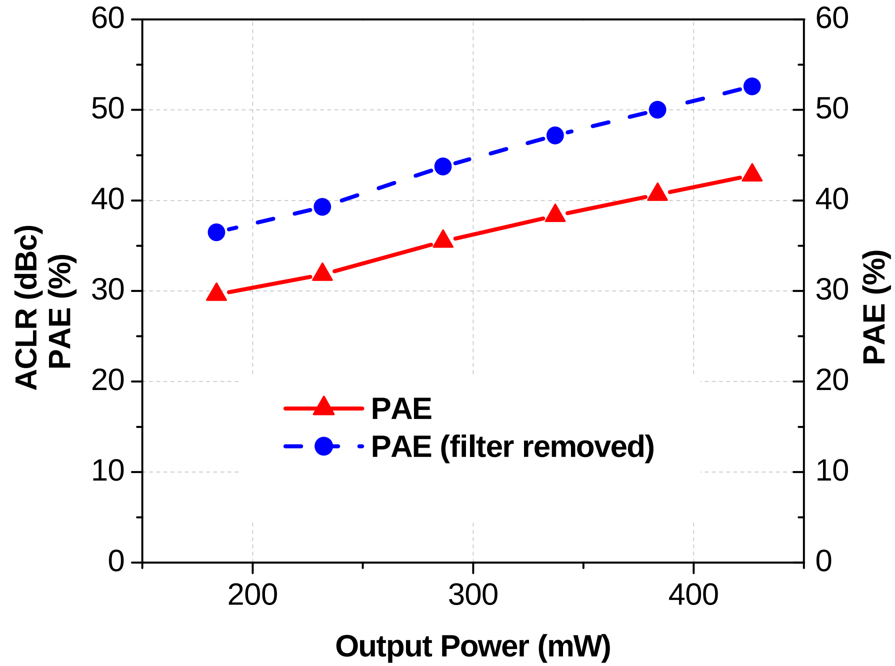
~39 dBc ACPR @ 5MHz, without additional linearization

~43% PAE (filter loss included)

52.6% PAE (filter loss de-embedded)

PAE&ACLR vs. Output Power





- Power efficiency increase with the output power
- ACLR remains stable over a certain range of output power

Summary of WCDMA Testing results

EDSM experimental result (filter loss de-embedded)	
Sampling Clock	*495.36Mbps*
OSR	*8*
$P_{out,peak}$	*27.1dBm*
PAE_{peak}	*52.6%*
Drain efficiency	*58.3%*
ACLR@-5MHz	*39dBc*
ACLR@+5MHz	*38.9dBc*
ACLR@-10MHz	*42.86dBc*
ACLR@+10MHz	*42.79dBc*

Comparison with Other Techniques

Reference	*Enhancement Scheme*	*Output power*	*PAE*	*Drain Efficiency*	ACLR
This work	*EDSM+PLM*	*27.1dBm*	*52.6%*	*58.3%*	*39dBc@5MHz* *42.8dBc@10MHz*
[1]	*Doherty*	*35.13dBm*	*42.7%*	-	*27dBc@2.5MHz* -
	Doherty+DPD	*35.13dBm*	*41.5%*	-	*49.6dBc@2.5MHz* -
[2}	*Doherty+DPD*	*31.5dBm*	-	*41.6%*	*29dBc@5MHz* *31dBc@10MHz*
[3]	*ET+DPD*	*41.5dBm*	*47%*	*49%*	*48dBc@5MHz* *53dBc@10MHz*

[1]J. Moon, J. Kim, I. Kim and B. Kim, "Highly efficient three-way saturated Doherty Amplifier with digital feedback predistortion," *IEEE* *Microwave and Wireless Components Letters*, Aug. 2008.
[2]W. C. E. Neo, J. Qureshi, M. J. Pelk, J. R. Gajadharsing and L. C. N. de Vreede, "A mixed-signal approach towards linear and efficient n-way Doherty amplifiers," *IEEE Trans. Microwave Theory & Tech*.,, May. 2007.
[3]D. Kimball, K. Myoungbo, P. Draxler, J. Jinseong, H. Chin, C. Steinbeiser, T. Landon, O. Krutko, L. Larson and P. Asbeck, "High Efficiency WCDMA Envelope Tracking Base-Station Amplifier Implemented with GaAs HVHBTs," IEEE Compound Semiconductor Integrated Circuits Symposium, Oct. 2008.

Conclusions

- PLM is able to improve the power efficiency of PA under non-constant-envelope modulations with reasonable linearity performance out-of-the-box

- Digital pre-distortion or digital feedback (including the PA in the Delta-Sigma loop) may be used for better linearity

- Suited for broadband, high PAR applications