A 2.4-GHz 24-dBm SOI CMOS Power Amplifier with Fully Integrated Output Balun and Switched Capacitors for Load Line Adaptation

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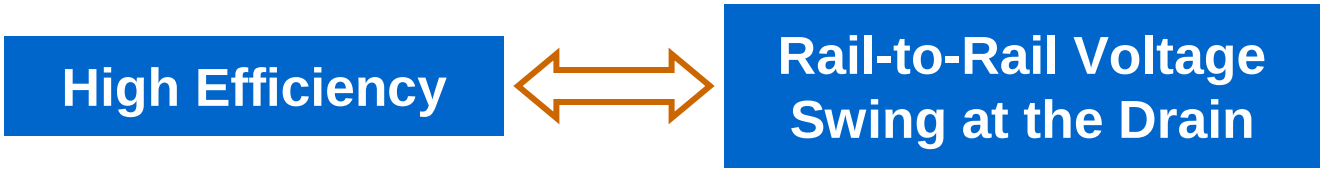
Efficiency Enhancement in Power Back-Off

- TX power control is needed to save battery life and mitigate multi-user interference
- "Simple" PAs exhibit best efficiency at maximum output power only

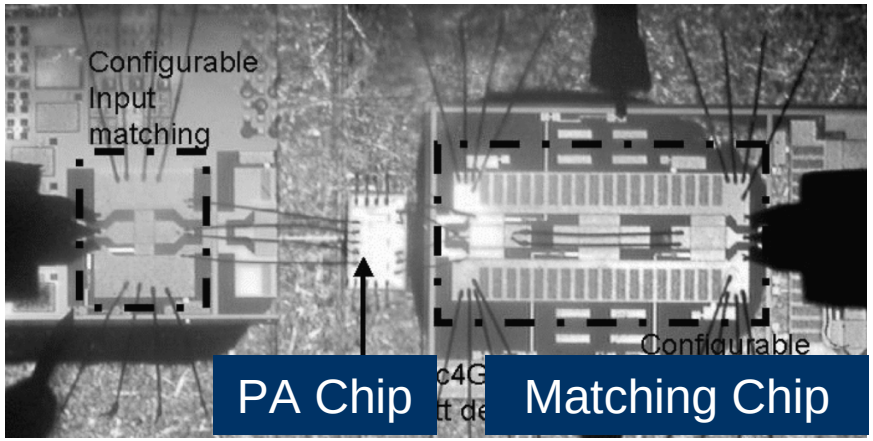


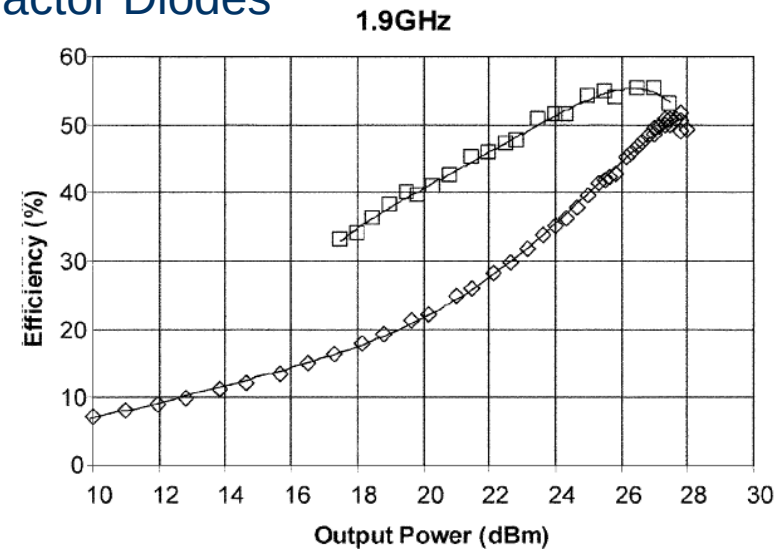
Maintaining high efficiency in power back off:

1. Reduce the supply voltage
   - Envelope Tracking, EER …
2. Adapt PA loadline
   - Active load adaptation (e.g., Doherty)
   - **Passive load adaptation**

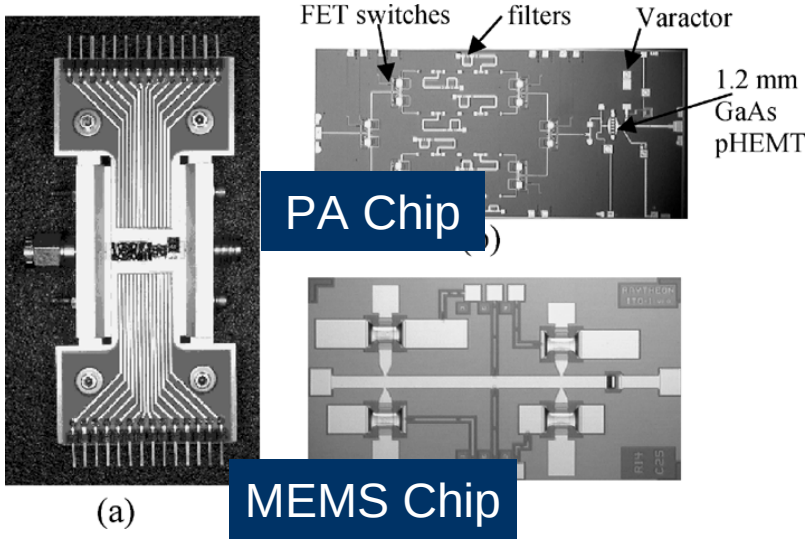
Variable Matching Networks: Recent Results

- Neo et al., JSSC 2009: Silicon-on-Glass Varactor Diodes





- Qiao et al., TMTT 2005: pHEMT PA + MEMS varactor tuner



Objective:

Load-Line Adaptation in a Fully-Integrated Silicon PA

Outline

Device Characterization

- SOI CMOS technology
- Load-pull experimental results
- Single-transistor latch-up

Integrated PA

- Circuit design
- Measured efficiency improvement
- Load optimization for linearity

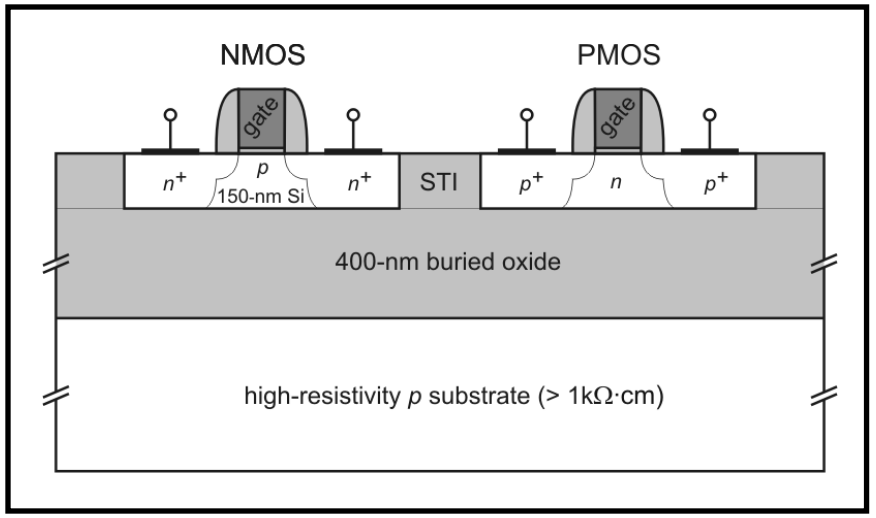
Technology Choice: SOI CMOS

Front-end:

- 0.13-µm SOI CMOS process
- High-resistivity substrate (>1kΩ·cm), 400-nm BOX, 150-nm Si layer
- 2nm / 5nm gate oxide thickness for 1.2V / 2.5V applications
- Floating-body (FB) and body-contact (BC) NMOS and PMOS

Back-end:

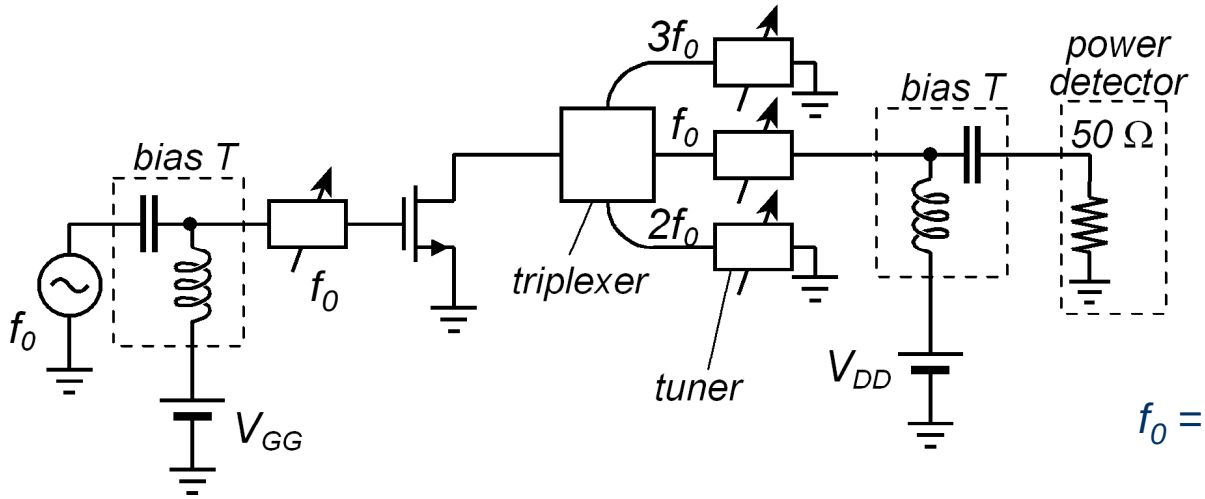
- 6 damascene Cu metal levels (thick-copper for last) + ALUCAP
- MIM capacitors, HIPO resistors, High-Q spiral inductors



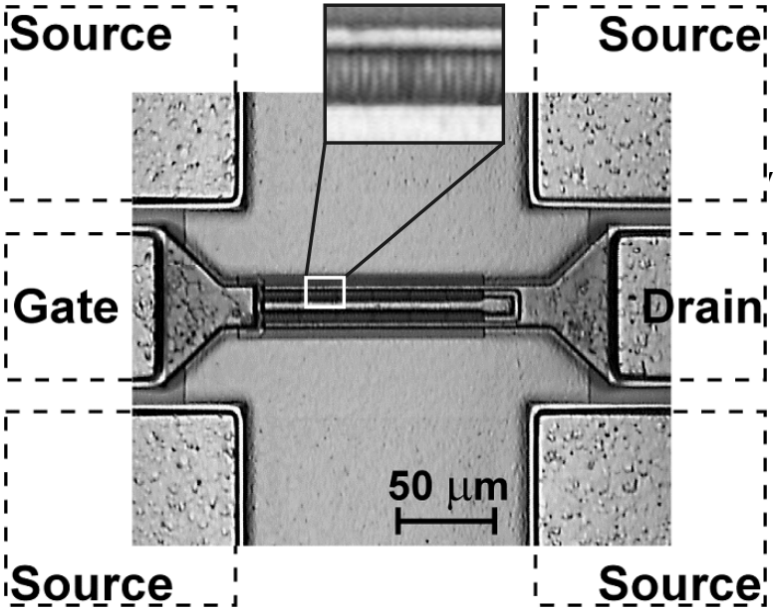
Enabling technology for RF SoCs:

- Higher speed / lower consumption
- High-Q Inductors and T. Lines
- Better cross-talk isolation
- Floating Substrate: FET Stacking
  - High-voltage PAs
  - High-voltage RF switches
  - High-voltage Switched Capacitors

On-Wafer Multi-Harmonic Load-Pull



f_0 = 1.9 GHz

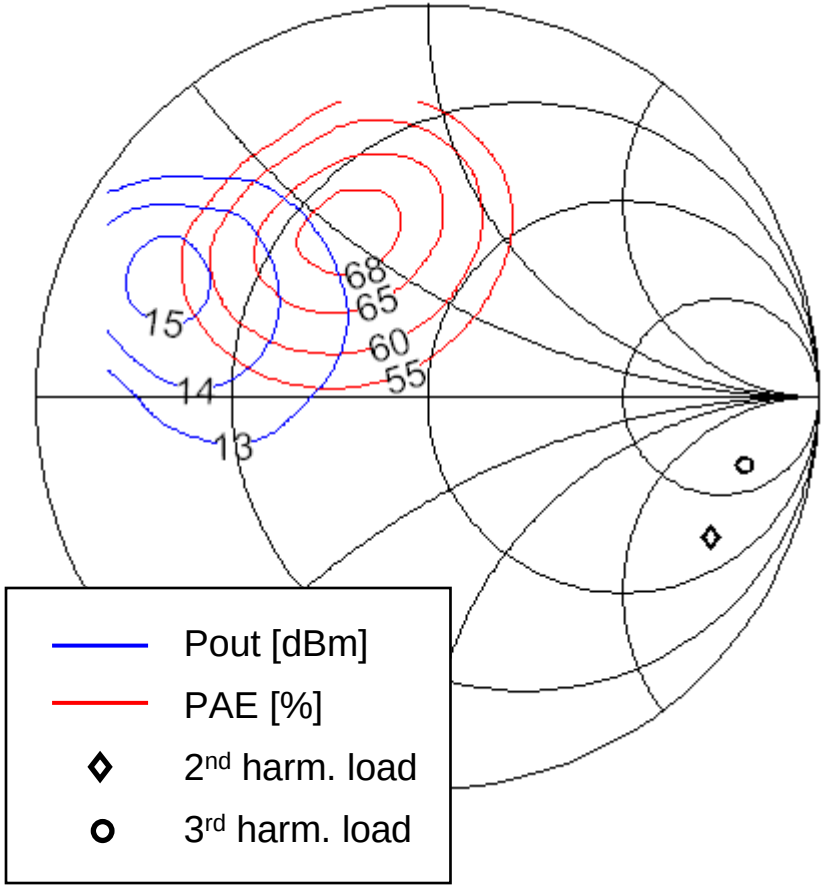


Device Under Test

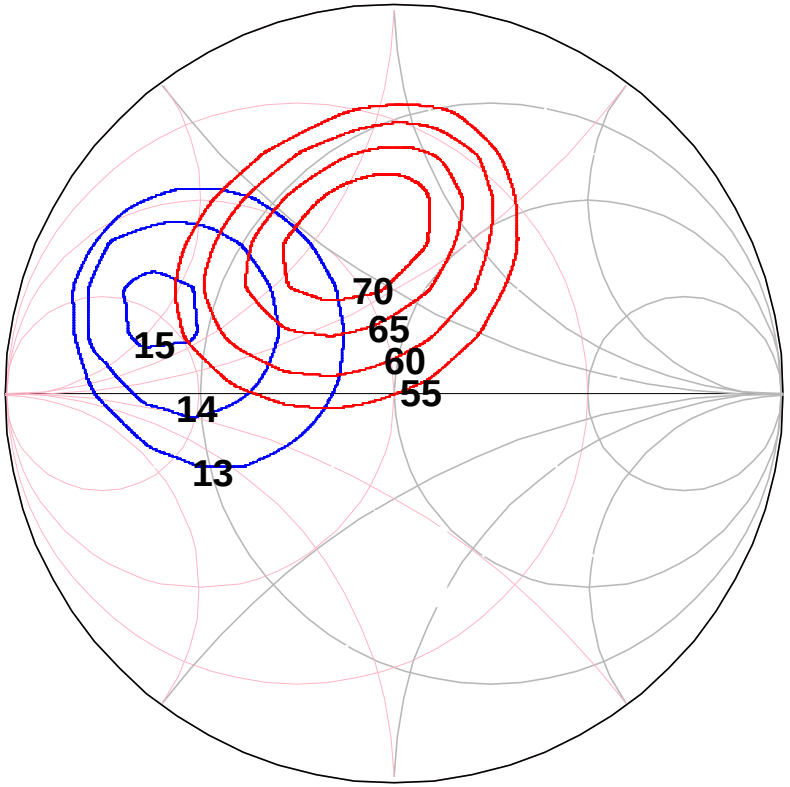
- L = 0.28 μm
- 2.5-μm gate fingers (total W = 960 μm)
- Optimized for modular layout
- Higher metal layers and multiple vias to reduce extrinsic parasitic resistance

Load-pull contours at V_{DD} 1.1 V

Measurement



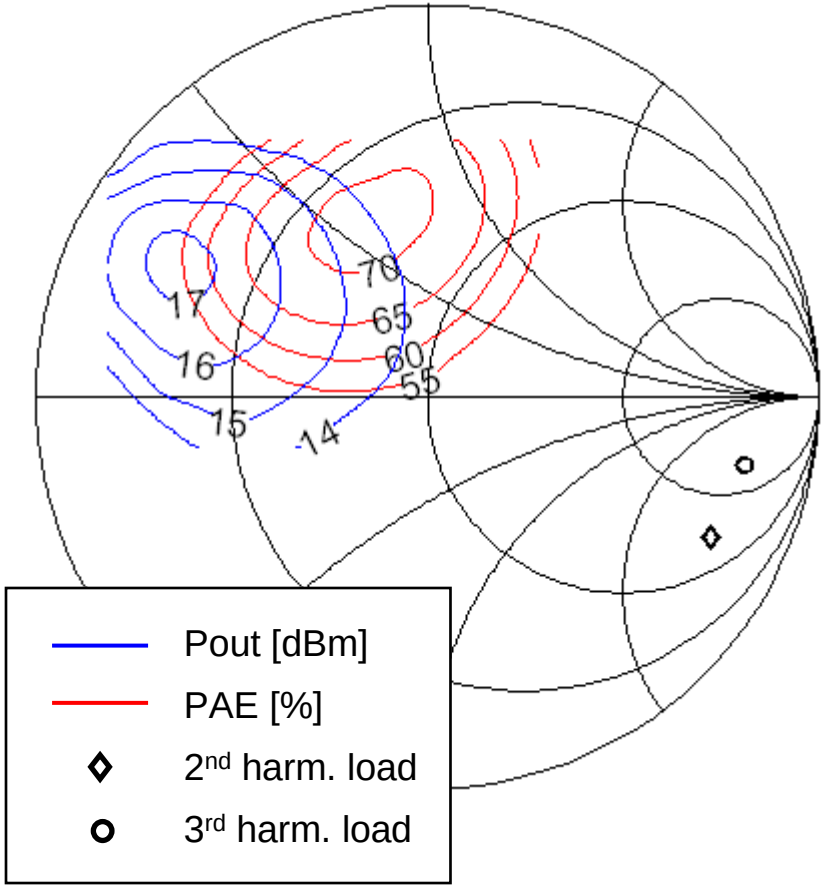
Simulation



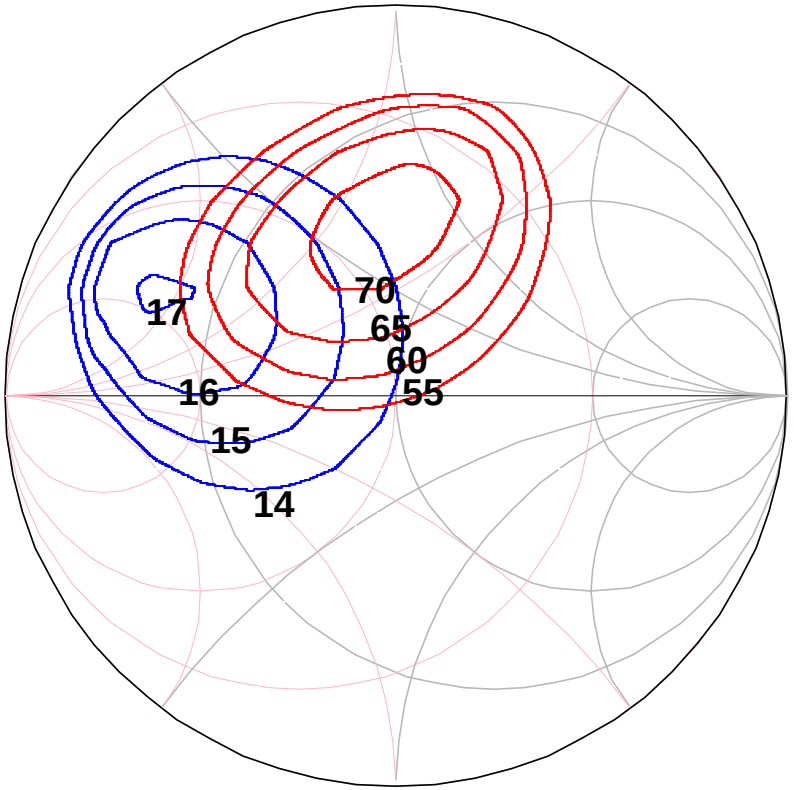
f_0 = 1.9 GHz, $P_{in(av)}$ = 2 dBm, single tone CW input,
class-E-like operation (2nd, 3rd harmonics open)

Load-pull contours at V_{DD} 1.4 V

Measurement



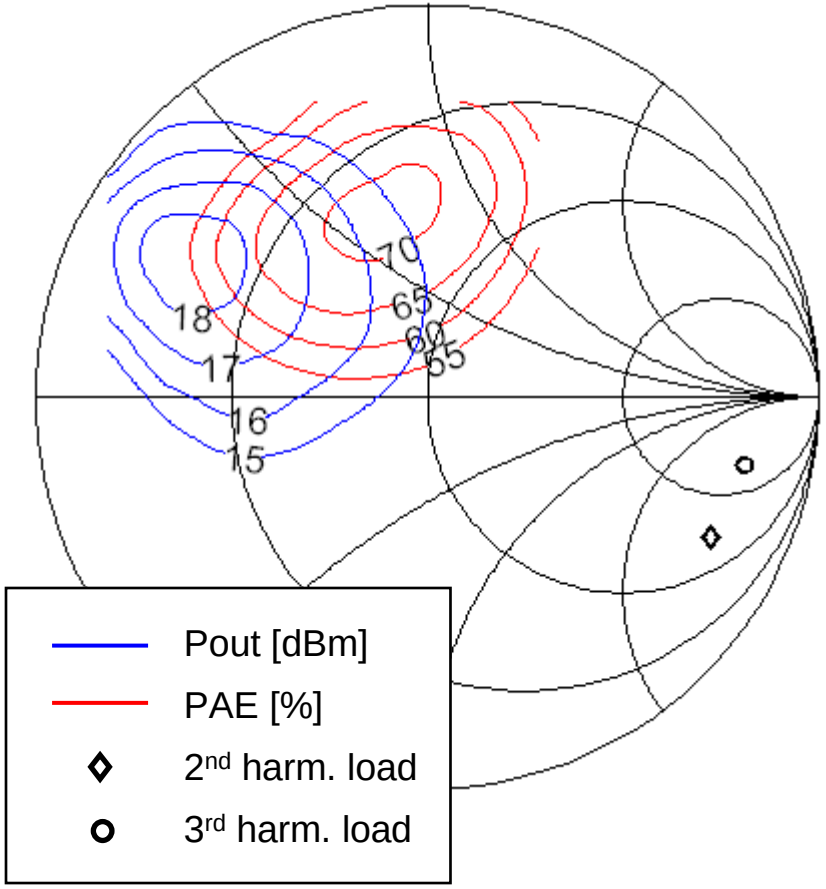
Simulation



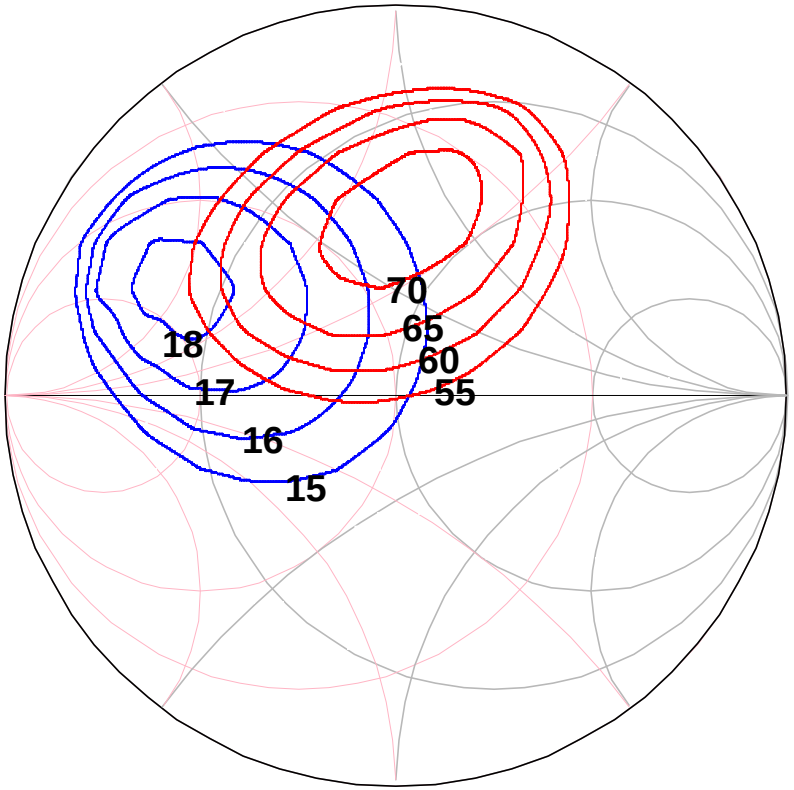
f_0 = 1.9 GHz, $P_{in(av)}$ = 2 dBm, single tone CW input,
class-E-like operation (2nd, 3rd harmonics open)

Load-pull contours at V_{DD} 1.7 V

Measurement



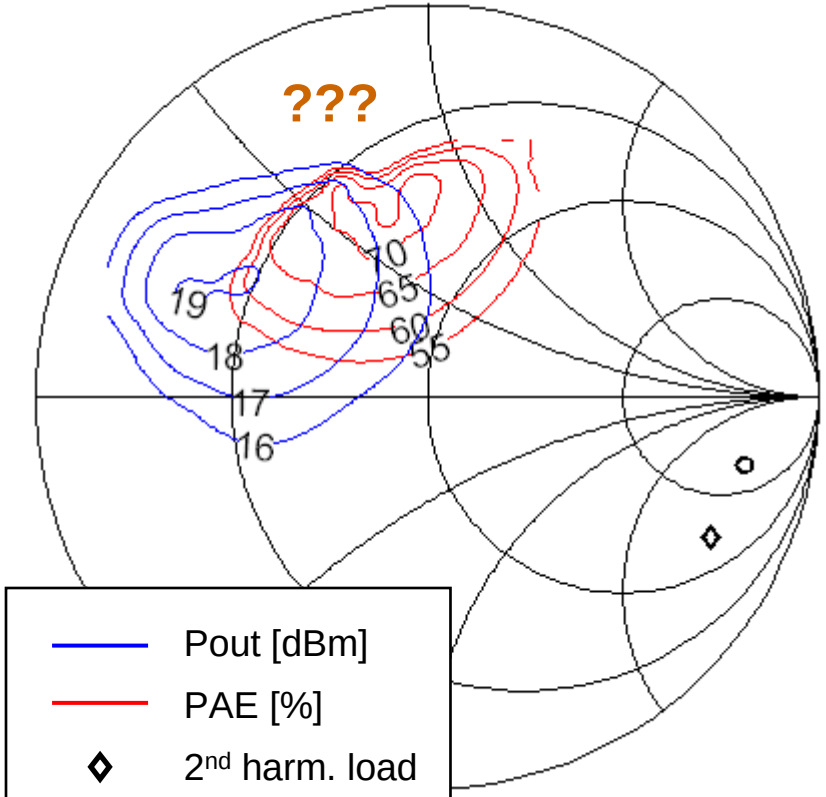
Simulation



f_0 = 1.9 GHz, $P_{in(av)}$ = 2 dBm, single tone CW input,
class-E-like operation (2nd, 3rd harmonics open)

Load-pull contours at V_{DD} 2.0 V

Measurement



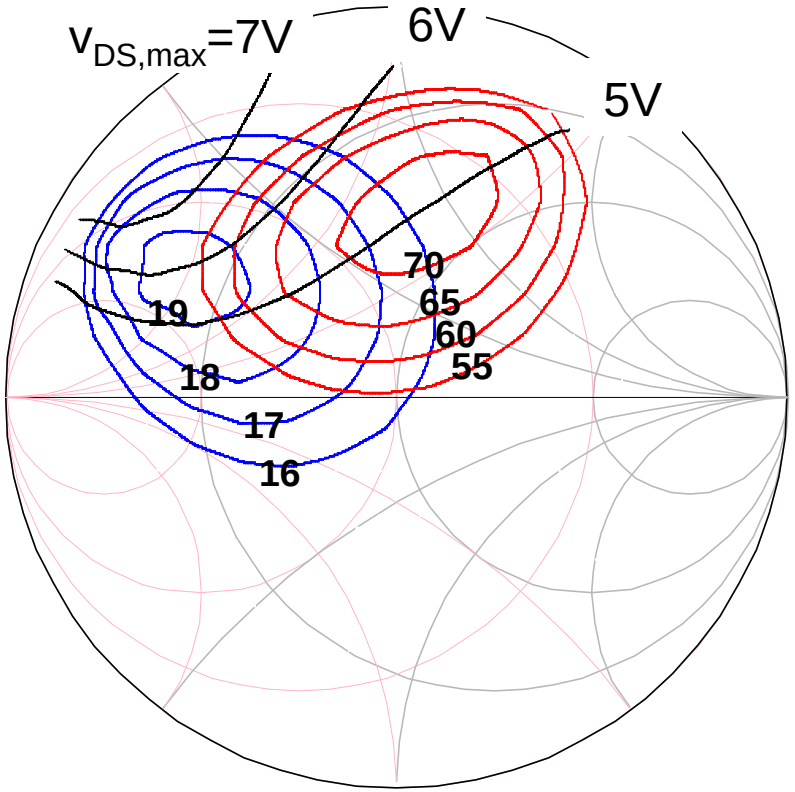
Pout [dBm]

PAE [%]

2nd harm. load

3rd harm. load

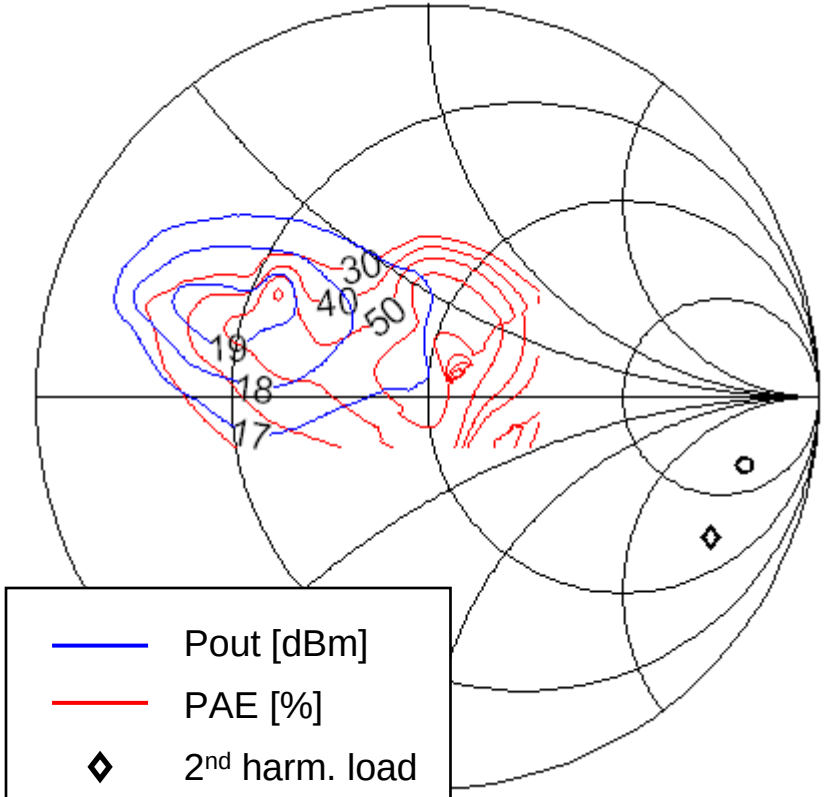
Simulation



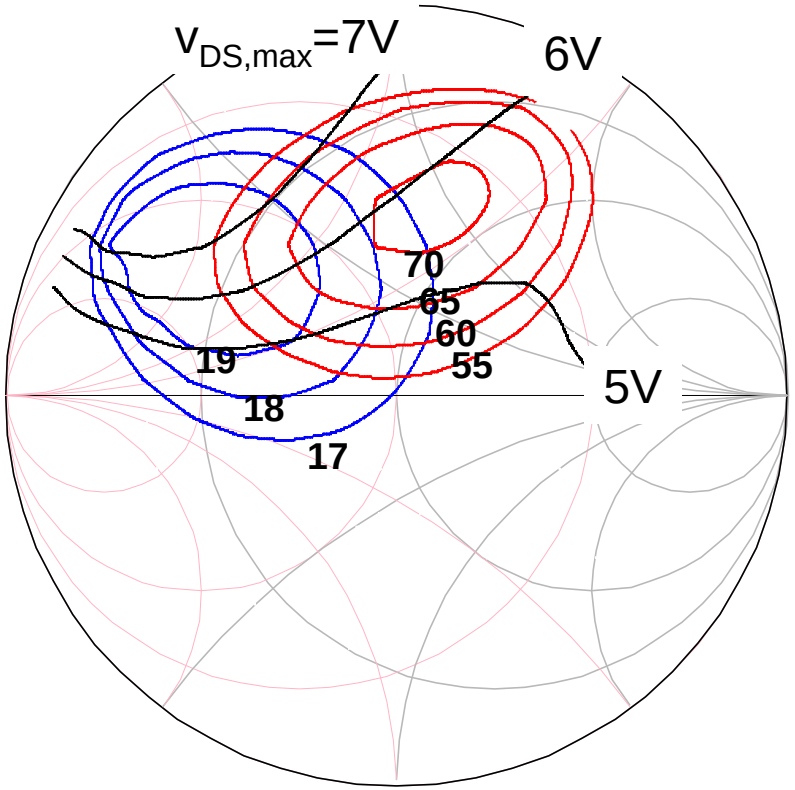
- Discrepancy b/w measurement and simulation
- Worse in the region of high V_{DS}

Load-pull contours at V_{DD} 2.3 V

Measurement

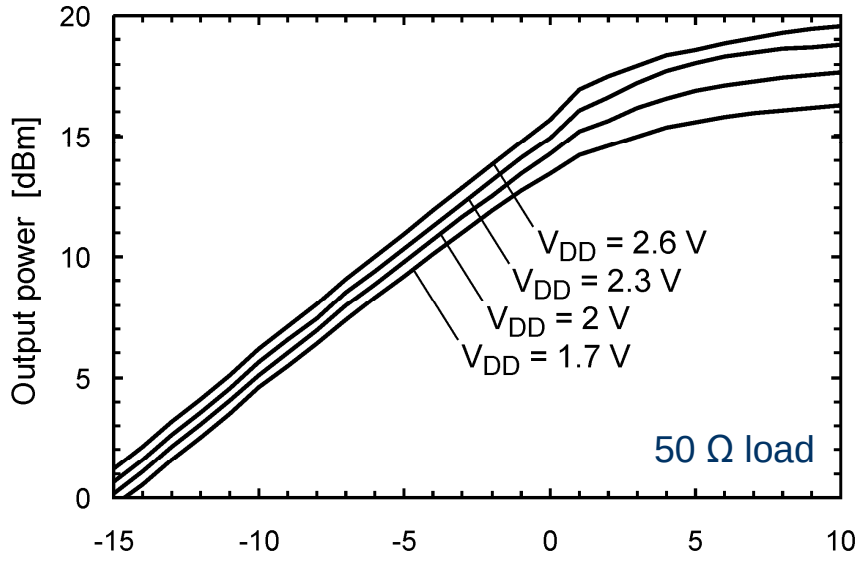


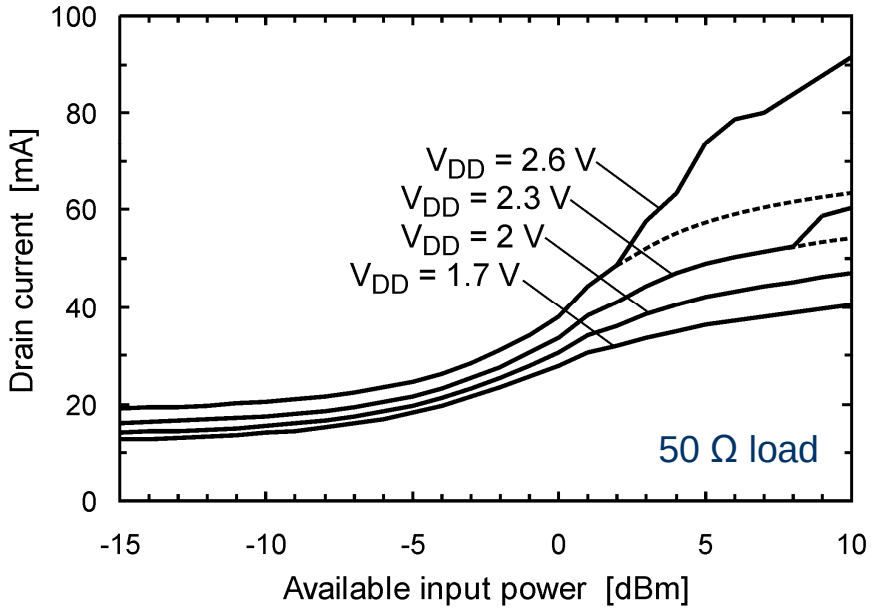
Simulation

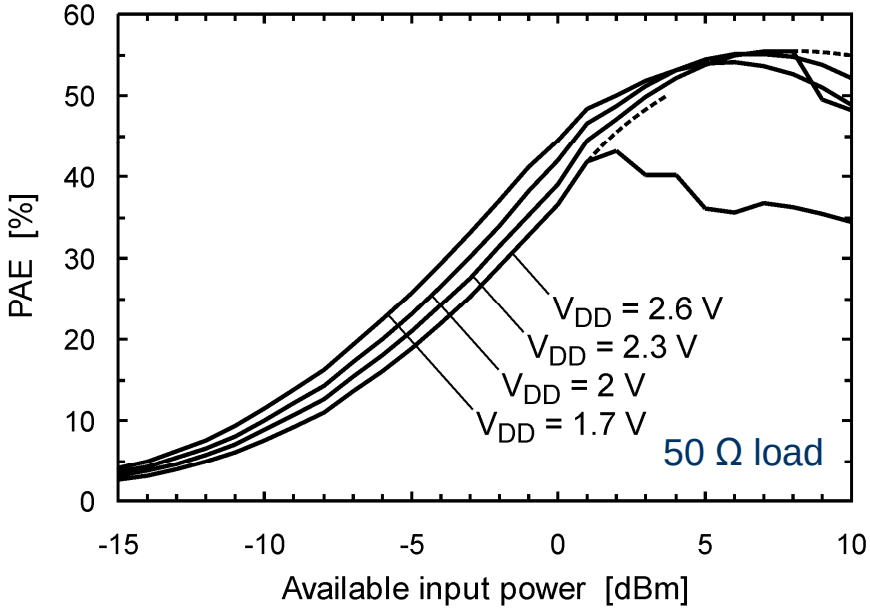


- Device operation at 2.3 V is compromised

Performance vs. V_{DD} (50 Ω Load)

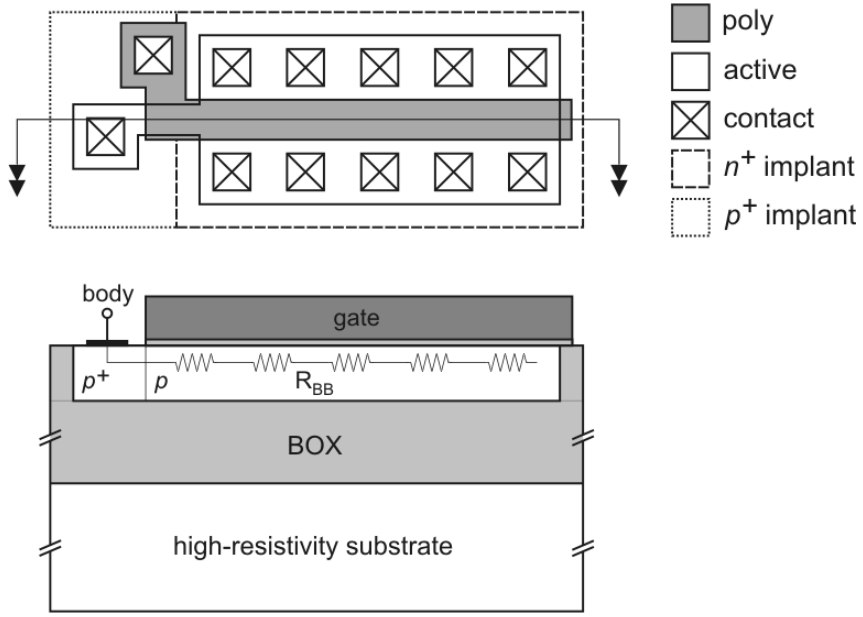


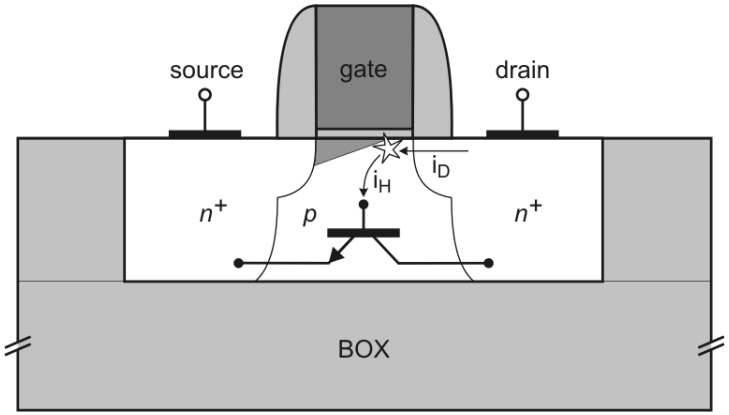


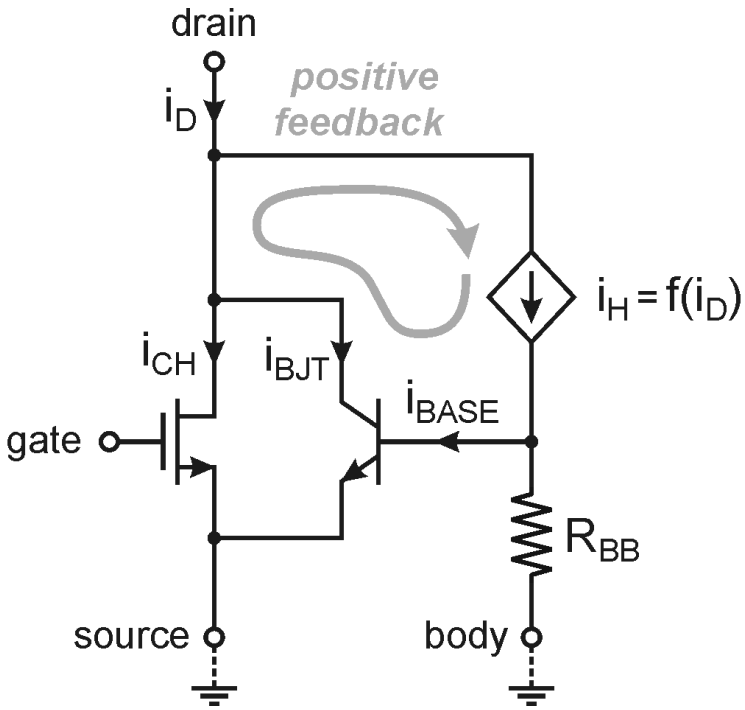


- Drain current runaway with large-signal input
- Self-sustaining (high I_{DD} even after RFin is switched off)
- Non destructive (safe gate oxide)
- Clean output spectrum (no RF instability / oscillation)

Single-Transistor Latch-up in SOI





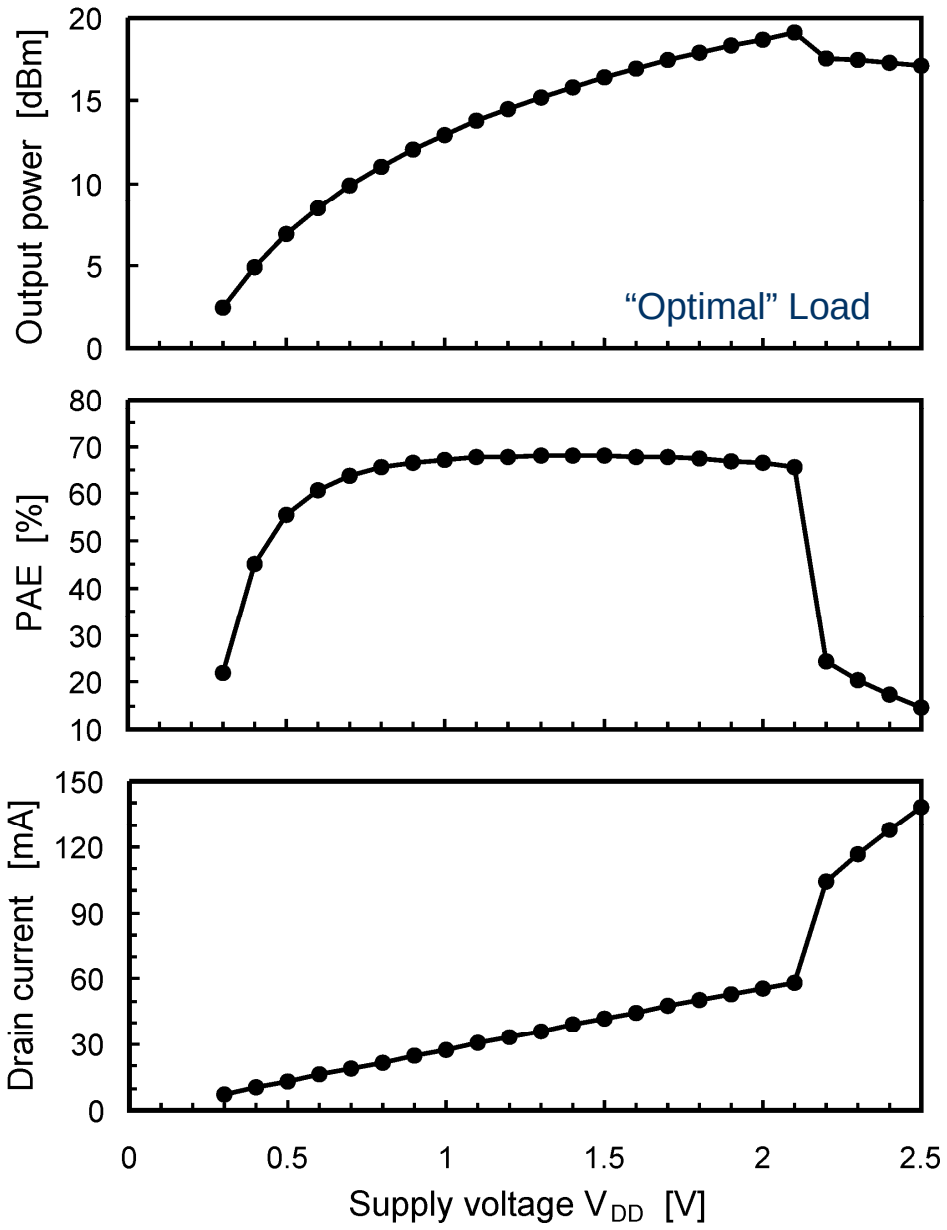


- Parasitic body resistance R_{BB}
- Narrow body finger $\rightarrow$ R_{BB} can much larger than in bulk (tens of kΩ / finger!)
- To avoid positive feedback, keep the BJT off:

$$v_{BS} < v_{BS,ON} = 0.7\text{V}$$

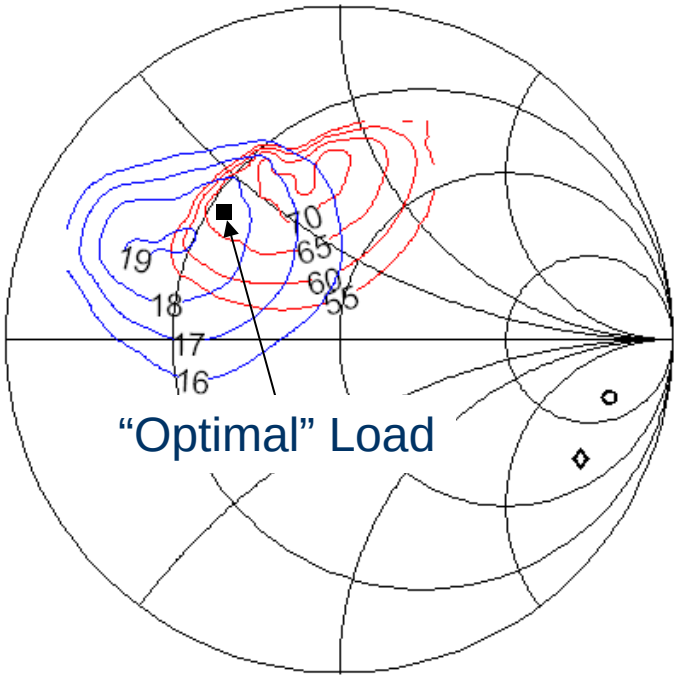
- Use short gate fingers

Performance vs. V_{DD} (Optimal Load)



- Safe operation at 2-V supply voltage, using 2.5-µm fingers
- Effect of shorter fingers can be theoretical estimated:

$$v_{BS,\max} = \frac{1}{2} j_H \, r_{BB} \, W_f^2$$



Outline

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Integrated PA

- Circuit design
- Measured efficiency improvement
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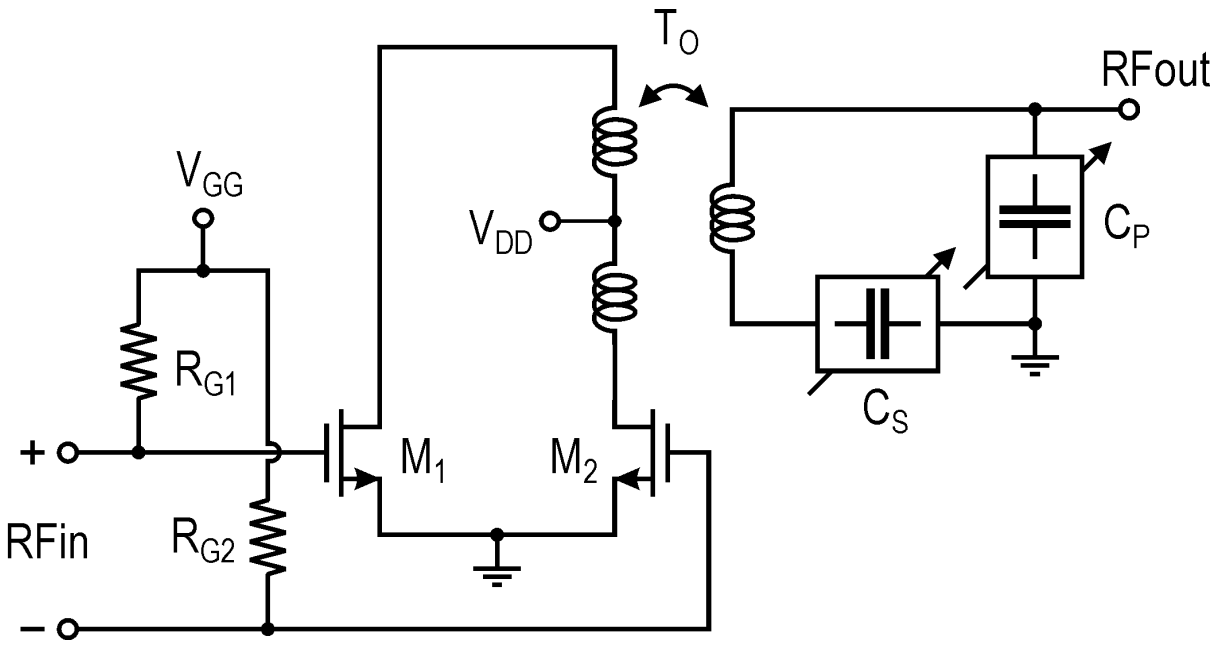
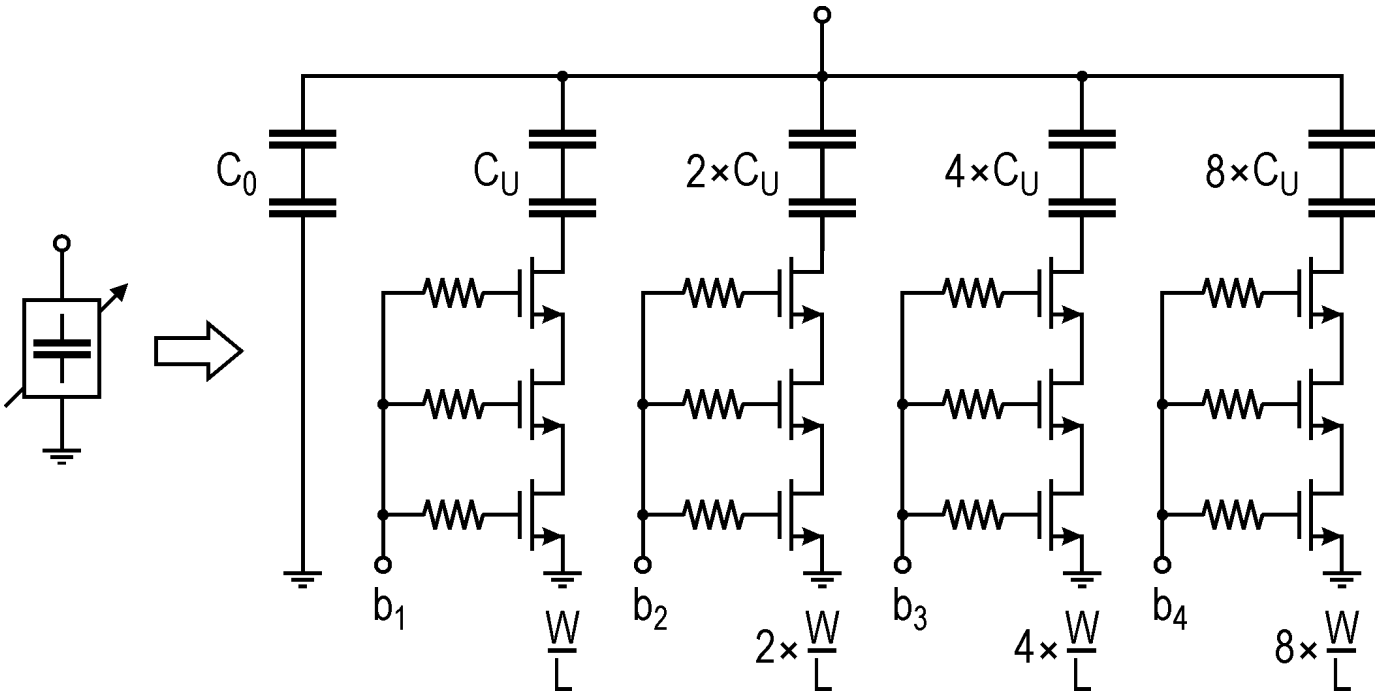
Simplified PA Schematic



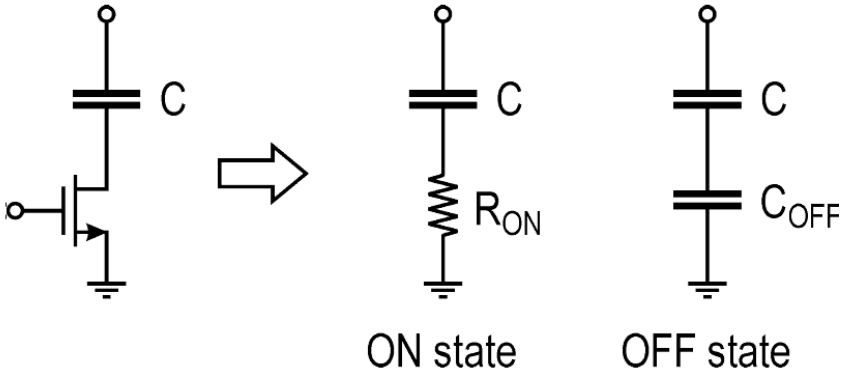
- Fully integrated tunable output matching
- Differential topology helps impedance transformation ratio (4x load impedance compared to single-ended)
- Two banks of variable capacitors

Tunable Output Matching Capacitors



- Bank of binary weighted switched caps (0.96 pF – 4.32 pF, 4 bits)
- Up to 10-V off state swing
  - → Transistor stacking for improved switch robustness (3 FB NMOS)
  - → 2 MIM capacitors in series

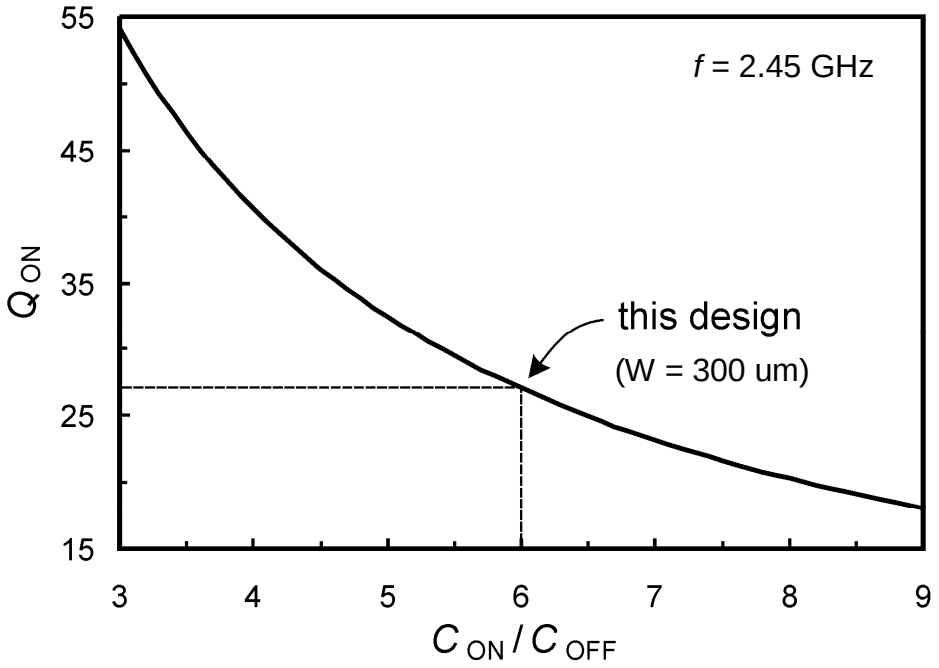
Tunable Capacitors: Design Criterion



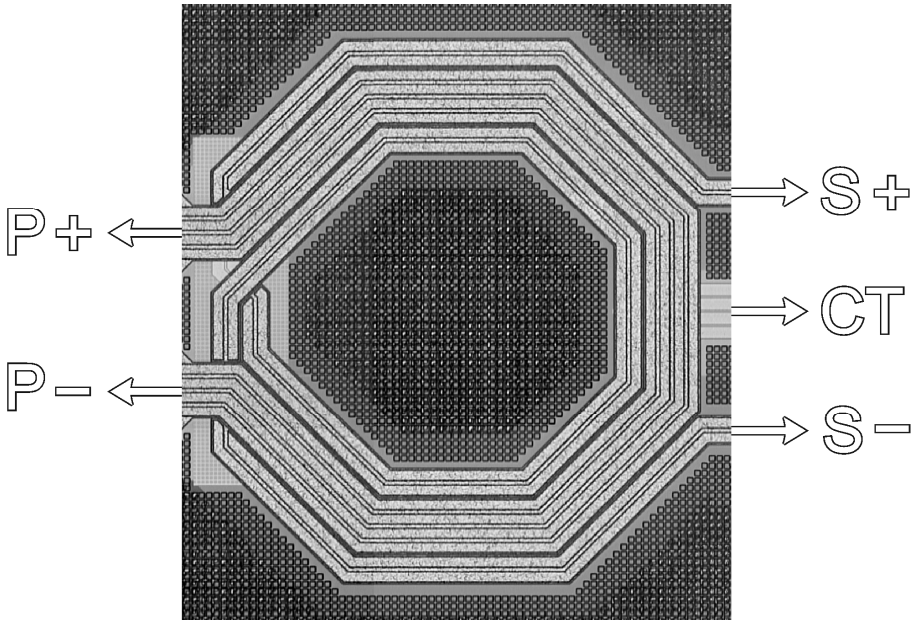
- Product τ is invariant with switch size and number of stacked transistors $\rightarrow$ Technology FoM
- $\tau \approx$ 400 fs for H9SOI
- Trade-off between capacitance quality factor and tunability

$$\tau = \mathrm{R}_{ON} \cdot \mathrm{C}_{OFF} = \text{constant}$$

$$\mathrm{Q}_{ON} \cdot \frac{\mathrm{C}_{ON}}{\mathrm{C}_{OFF}} = \frac{1}{\omega\tau} = \text{constant}$$



Output Transformer

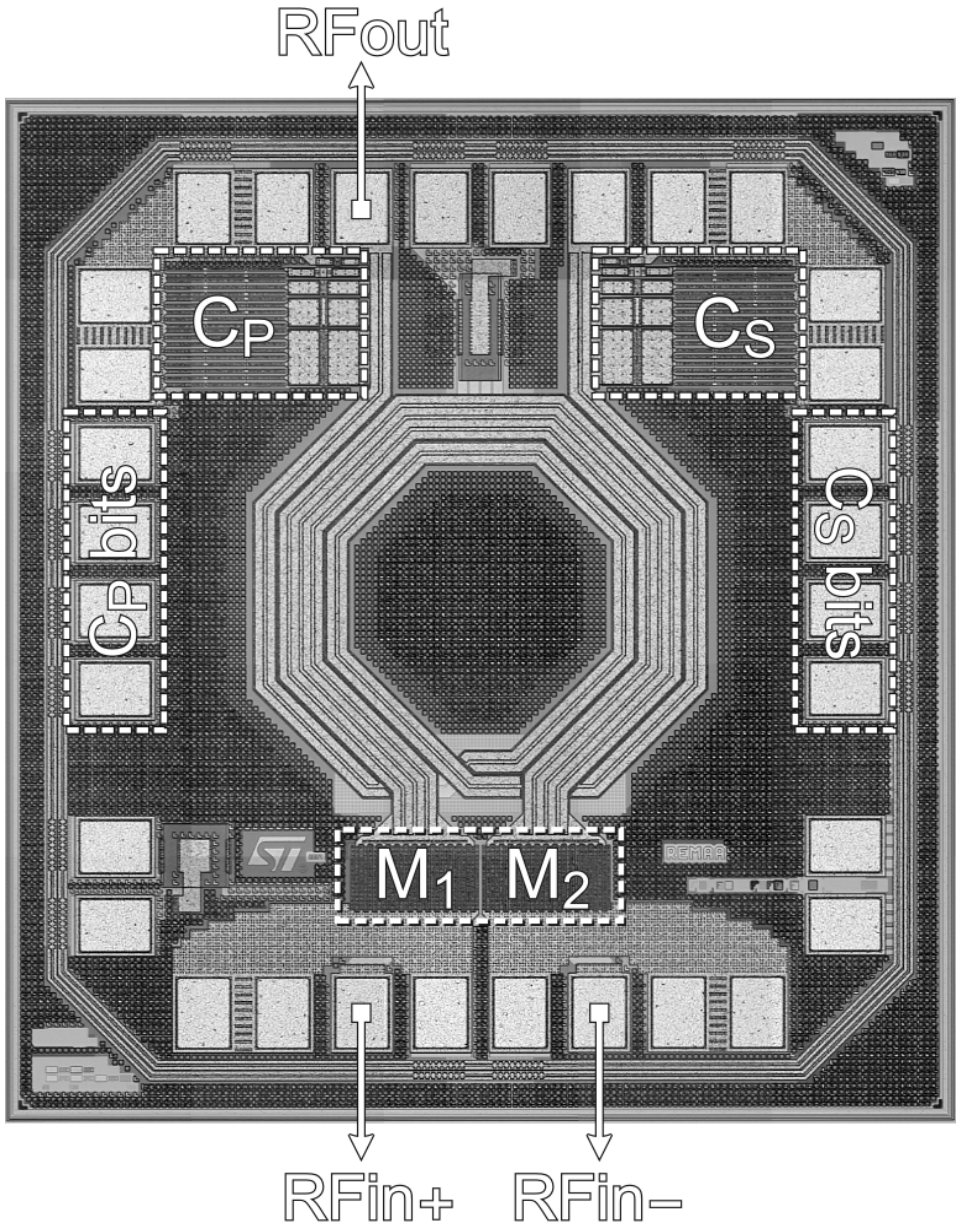


- Provides biasing, differential-to-single-ended conversion, and impedance matching
- Topmost metal layers paralleled to minimize series resistance
- No ground shield
- Large single-turn (no via) primary coil to carry dc current

Parameter	Primary coil	Secondary coil
Shape	Octagonal (interleaved)	
Number of turns	1 (center tap)	2
Trace width	52 µm	26 µm
Trace metal	MTL5 + MTL6 + ALUCAP	
External diameter	520 µm	
Inductance	690 pH	2.2 nH
Quality factor	12.2	12.6
Coupling factor	0.65	

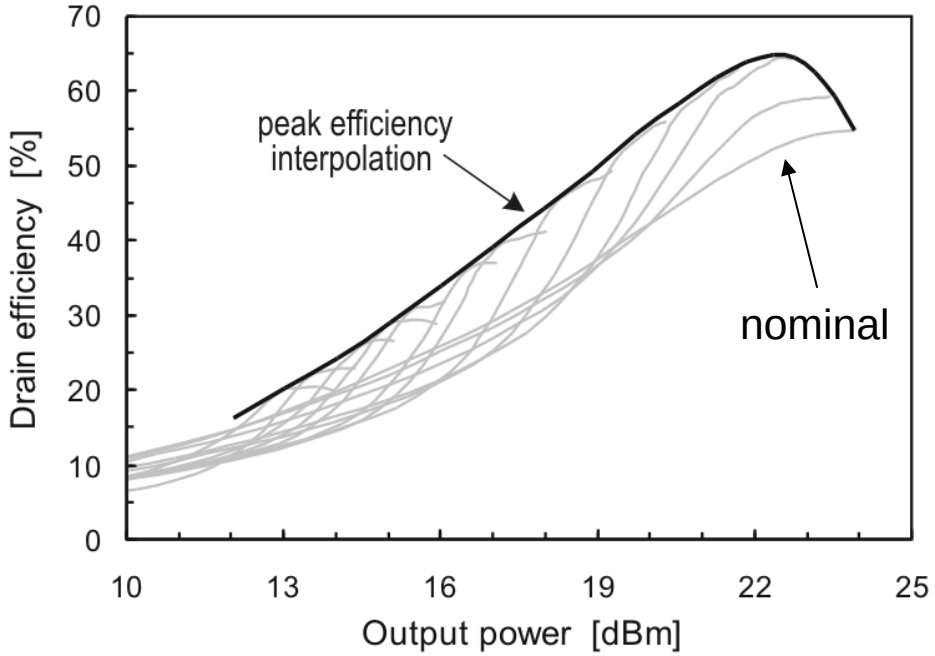
Circuit Layout and Assembly

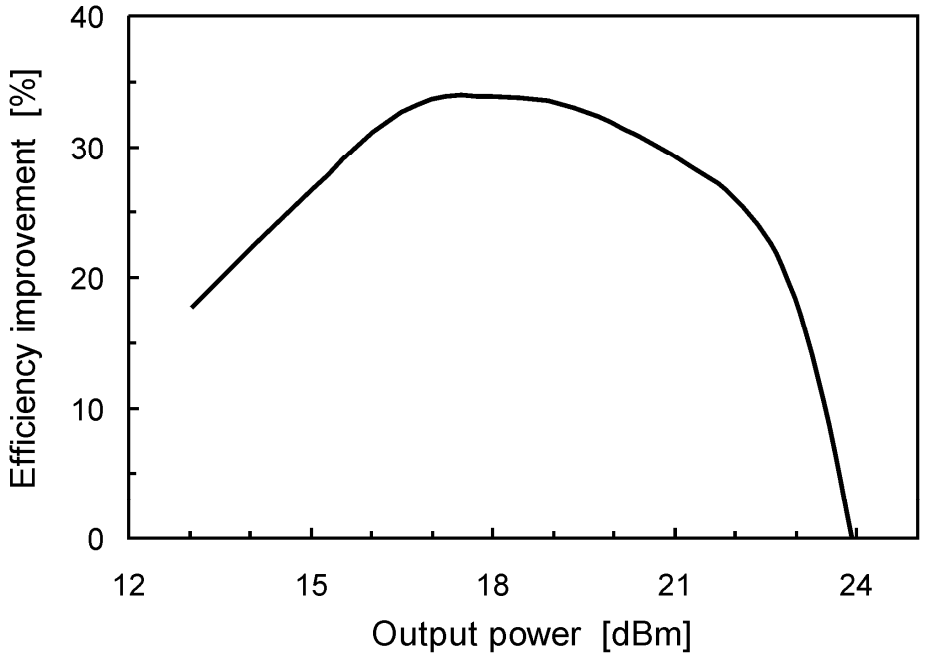
- Die area: 1.1 x 1.2 mm
- Chip-on-board assembly (wire bond)
- FR4 test board
- No matching refinement at the output
- Lumped matching and external SMA balun at the input



Experimental Characterization

Single-tone continuous-wave (CW) test at 2.45 GHz and 2-V supply voltage





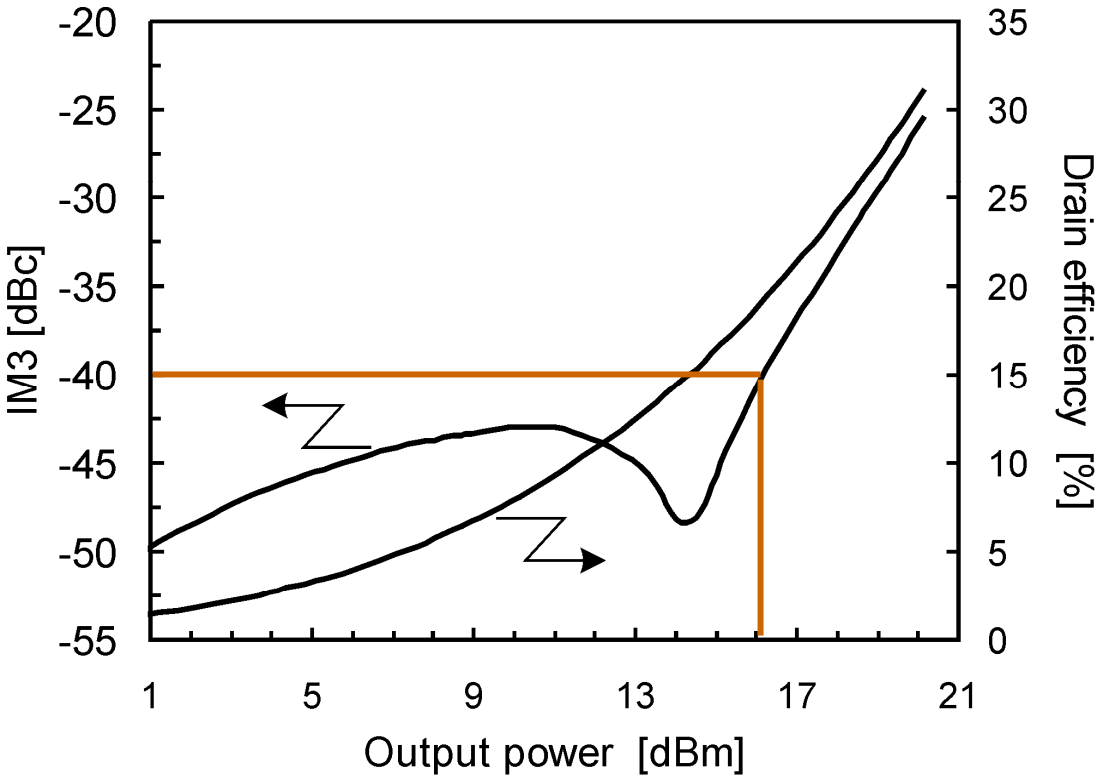
Procedure

- Output matching network firstly tuned for maximum output power
- Efficiency optimized at each individual power level

Results

- Peak performance: 23.9 dBm / 55% drain efficiency
- 65% maximum efficiency
- Up to 34% relative efficiency improvement in back off

Load Reconfiguration for Optimal Linearity



V_{DD} = 2 V, *f* = 2.45 GHz, I_Q = 40 mA, two-tone CW input with Δf = 15 MHz

- Load can be adapted to obtain optimized linearity
- A severe –40-dBc IM3 spec is met up to 16 dBm with 19% efficiency (15MHz tone spacing, WLAN-like testing)

Summary

Device characterization

- High PAE (72% at 1.9 GHz) and safe operation at nominal 2-V supply
- Single-transistor latch-up identified as main limitation for SOI PAs
- Device layout guidelines have been provided

Integrated PA Design

- First CMOS PA with fully integrated reconfigurable matching network
- Nominal performance: 24-dBm P_{out} with 55% efficiency at 2.4 GHz
- SOI process enables load adaptation (up to 34% relative efficiency enhancement)
- Load adaptation also exploited to improve linearity

Acknowledgements

- B. Rauber, C. Raynaud, STMicroelectronics for device fabrication
- A. Scuderi, STMicroelectronics, for helpful discussion