A Testbench for Analysis of Bias Network Effects in an RF Power Amplifier with DPD

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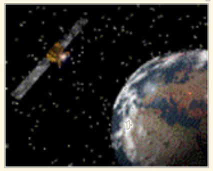
Outline

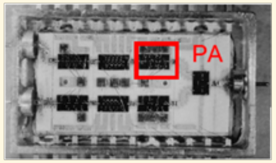
- Introduction
  - Motivation
  - Bias Network design
  - DPD
- Measurement Setup
- Experimental Results
- Conclusions

Introduction

- The power amplifier is a critical component in a wireless system
- Important power amplifier parameters:
  - Frequency band
  - Power
  - Bandwidth
  - Linearity
  - Efficiency
  - Size, cost ...
- Linearity vs. efficiency tradeoff
- Linearization, efficiency enhancement

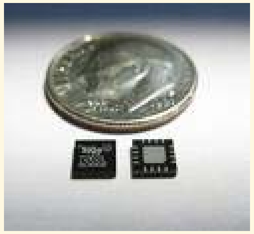
Satellite transmissions



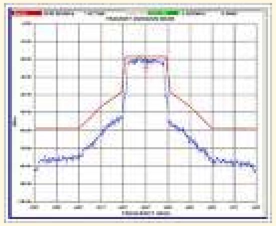


Cellular phones

Handset transmitters



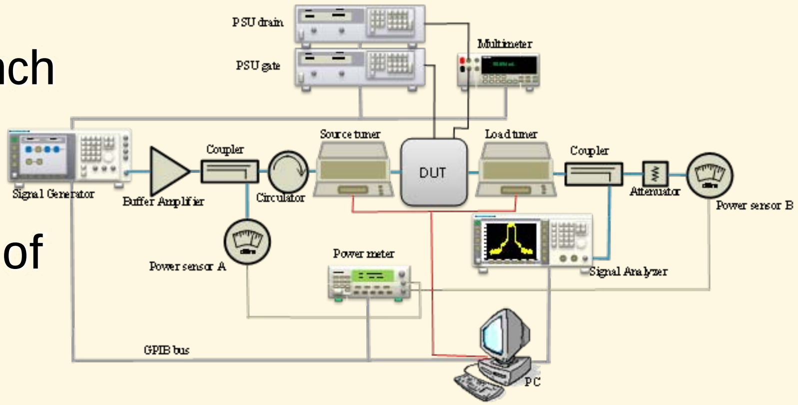
Size,cost

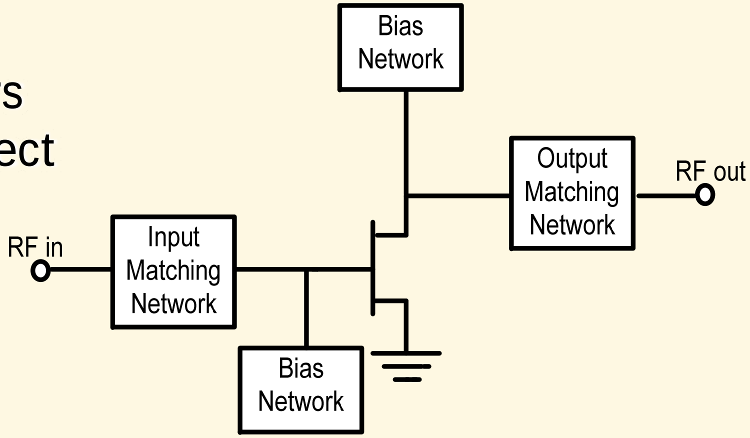


Spectral mask

Introduction

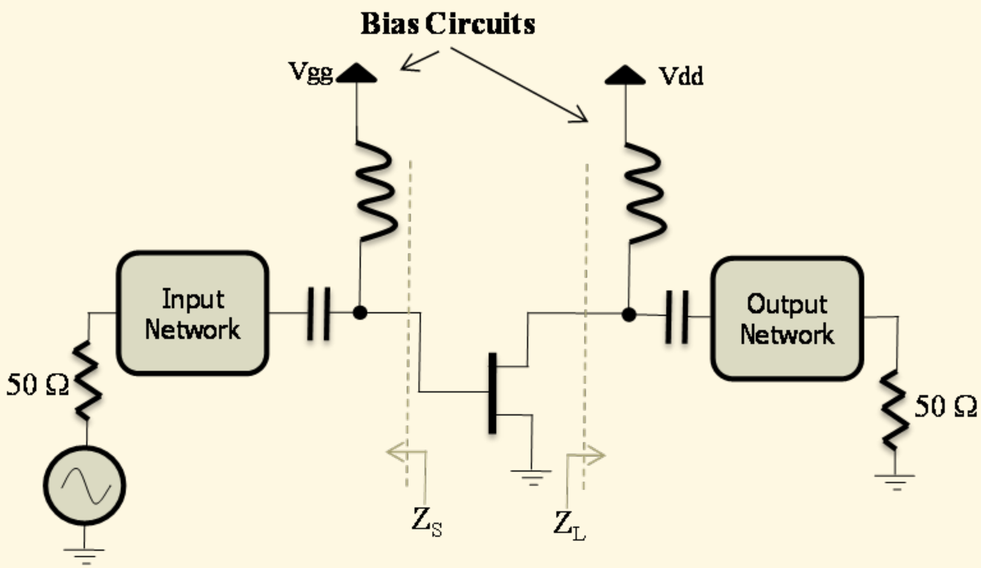
- The scope of this work is to build a testbench where we can do most measurements necessary for a PA design
- In addition we want to measure the effect of different bias network in the PA
- A power amplifier based on a pHEMT transistor is deigned for the experiments
- A standard bias network is first used for the experiments
- Two extreme variants where large inductors are used are tested to demonstrate the effect on the linearity
- The measurements are done with and without DPD





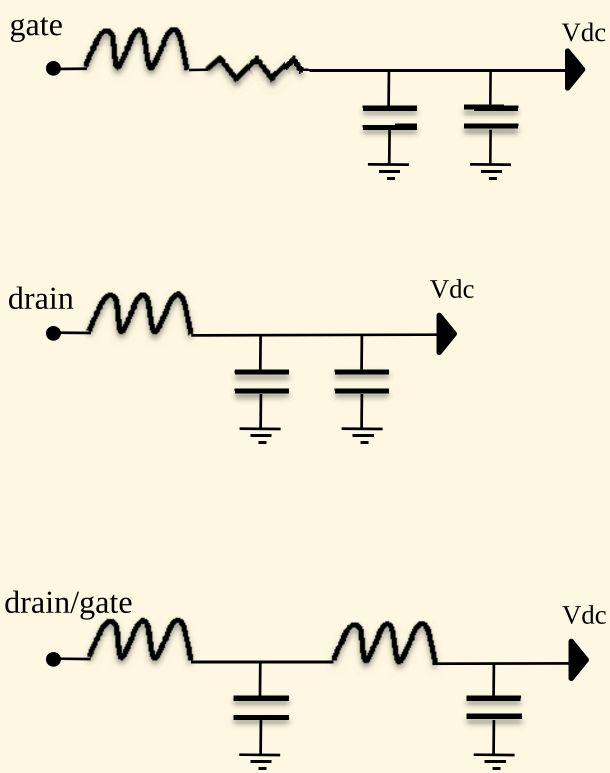
Introduction

- Bias network design
  - Isolate RF from DC
  - Important for stability at low frequencies
  - Defines the impedance at baseband
  - Often based on empirical design methods
  - More critical as the bandwith of the signal increases
  - Traditionally simplified to a large inductor in text books, but recently this topic is being covered (Cripps)



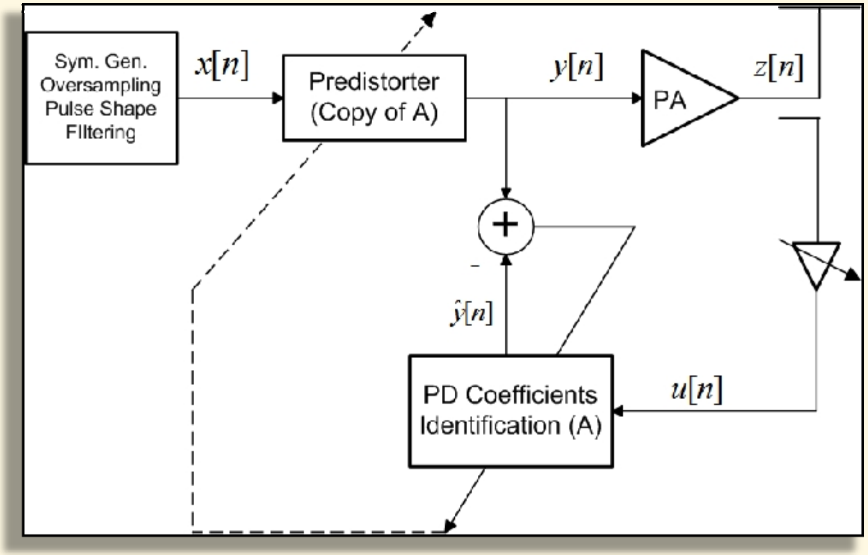
Introduction

- Different bias configurations
  - Resistor improve stability, but not desirable at drain
  - Large impedance at baseband can result in drain modulation/memory effects
  - Internal parasitics in SMD components



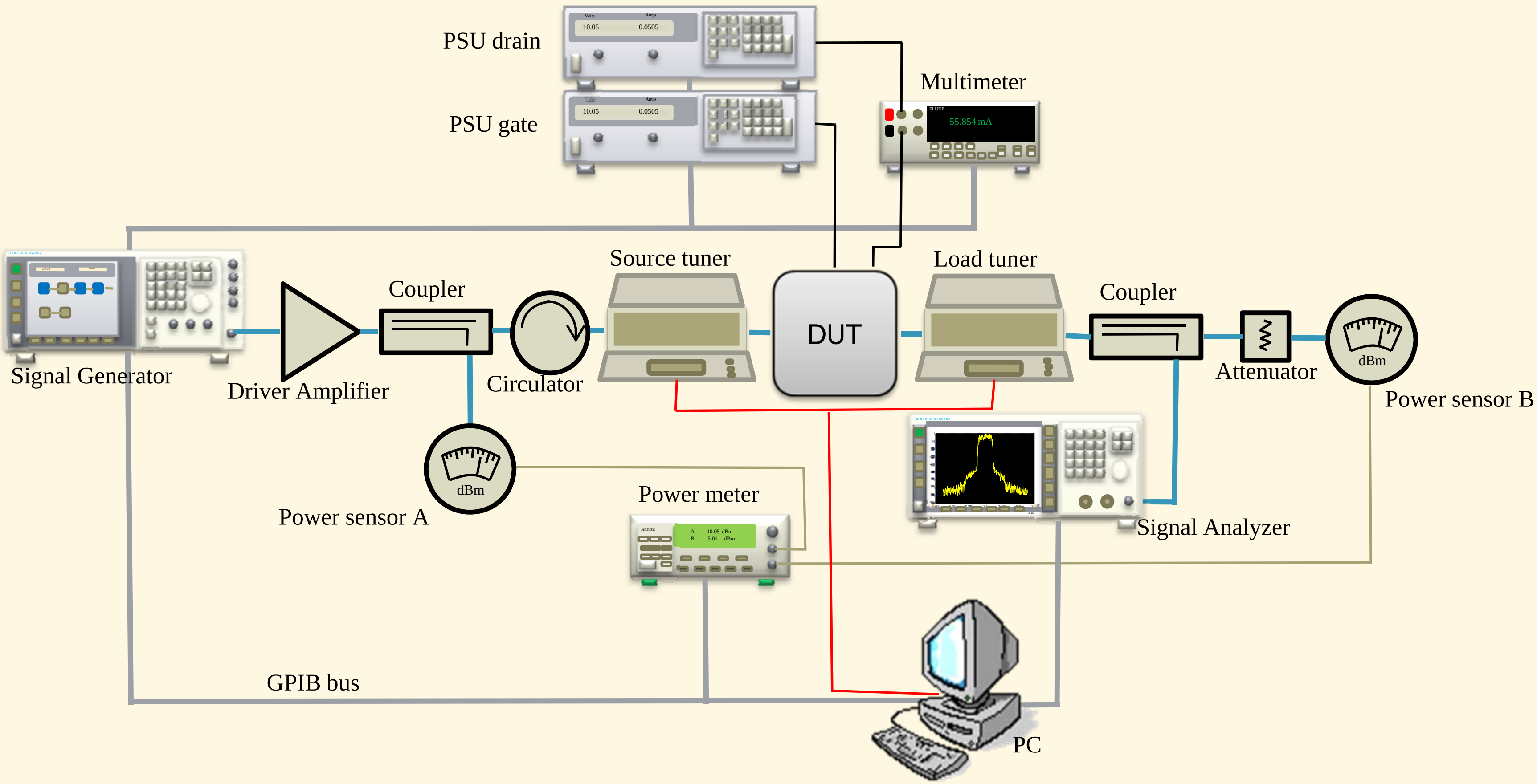
Introduction

- Simple memoryless DPD
  - Complex baseband samples at the input and output are recorded
  - A blockbased least square algorithm is applied to identify the DPD coefficients
  - The DPD algoritm and communication with the instruments is implemented in Matlab
  - The algoritm sensitive to memory that has its origin in the bias network



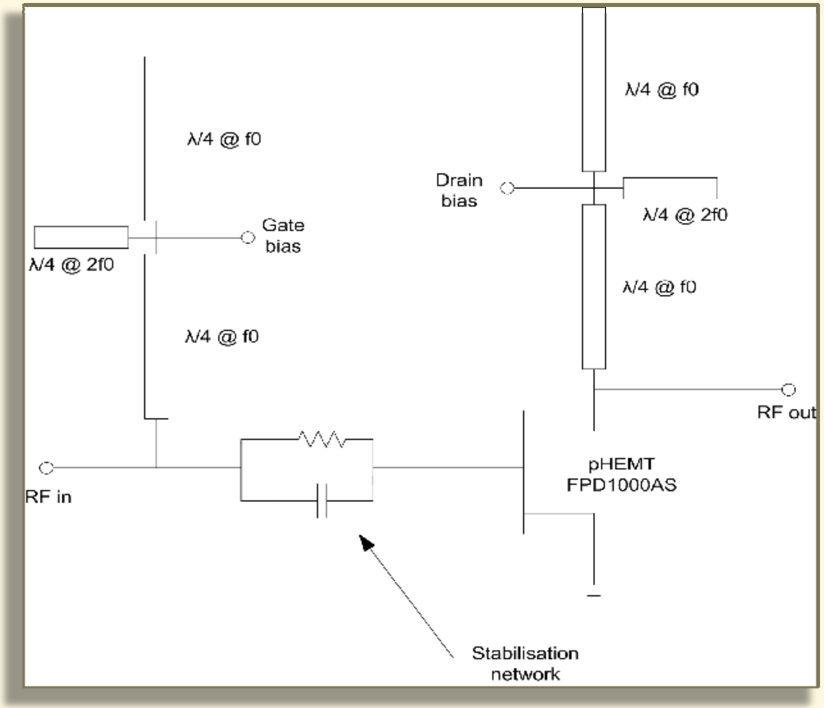
The baseband DPD model based on indirect learning architecture

Measurement Setup



Measurement Setup

- Combinations of quarter-wavelength transmission lines isolates bias circuitry from RF at f0 and 3f0, 2f0 shorted
- A 1 watt pHEMT transistor used in the experiments
- The transistor is biased in deep class AB
- 2.4 Ghz

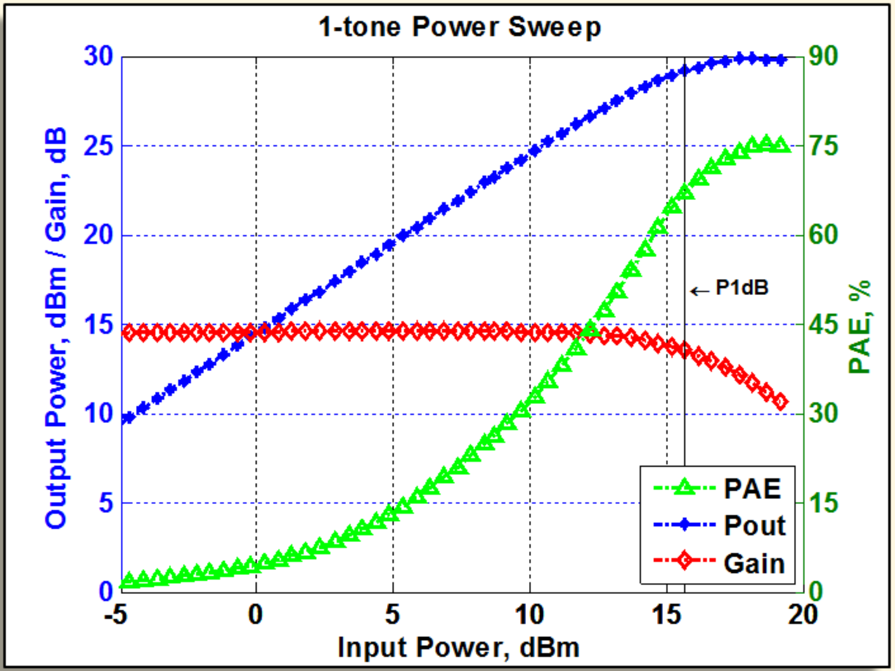


DUT

Experimental Results

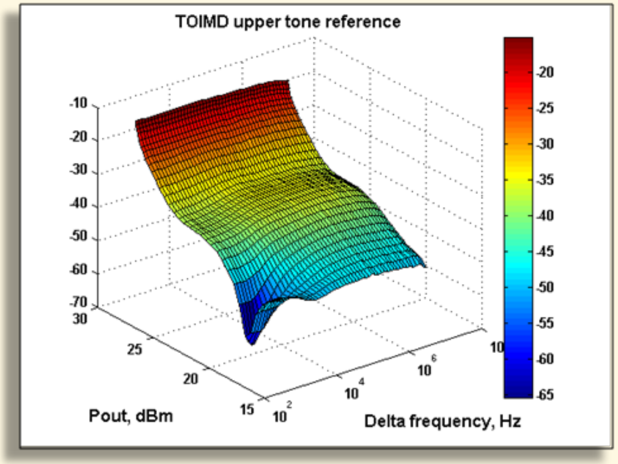
- 1-tone measurements
  - Source- and load impedance optimized for best efficiency
  - 1-tone measurements are independent on the bias circuit

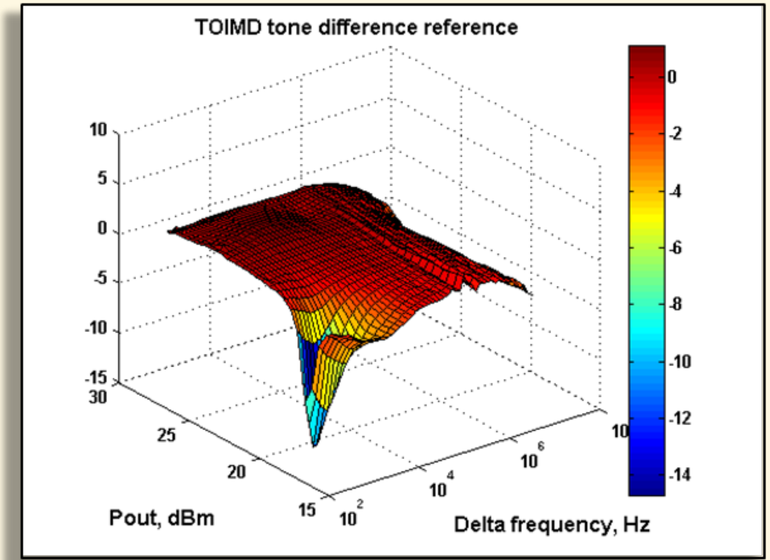
1 dB Compression	
Pout	29.2 dBm
PAE	67 %

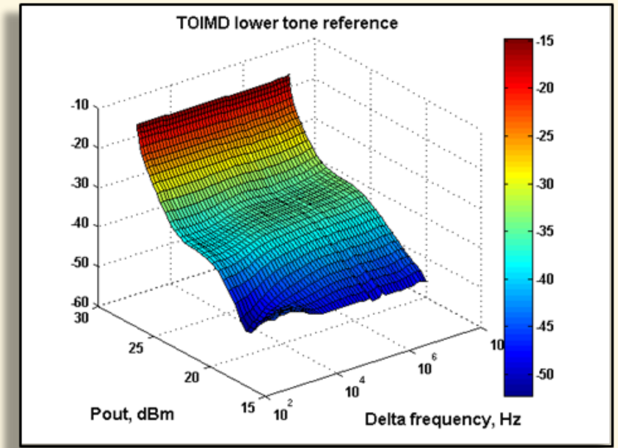


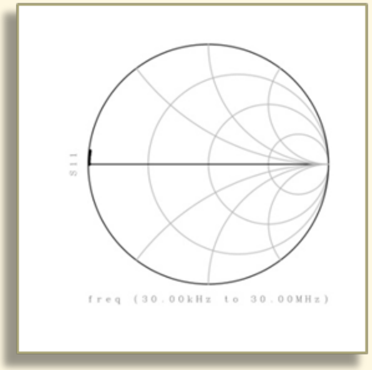
Experimental Results

- 2-tone measurements with reference bias
  - Close to short circuit at baseband at drain
  - Small differences between upper and lower IMD product, except one point





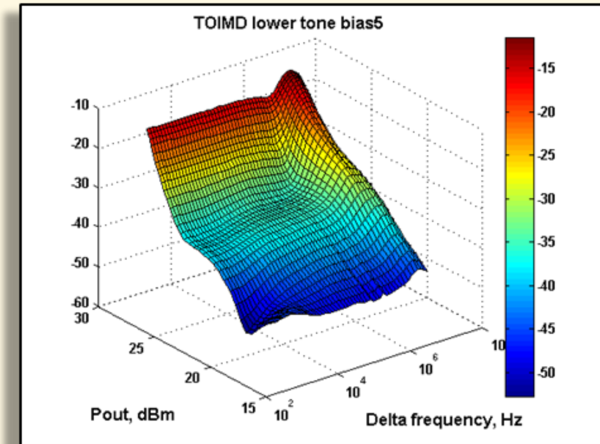


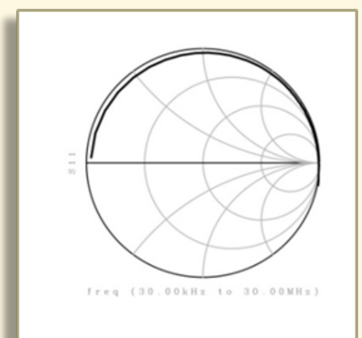


Bias circuit impedance

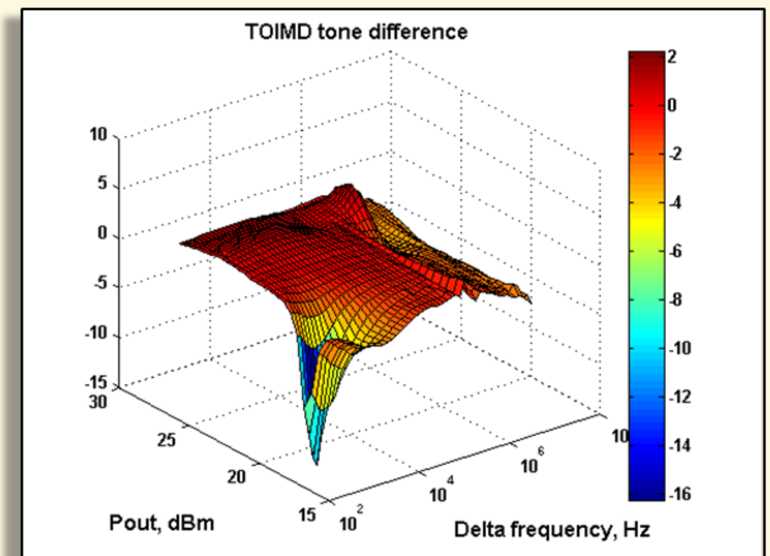
Experimental Results

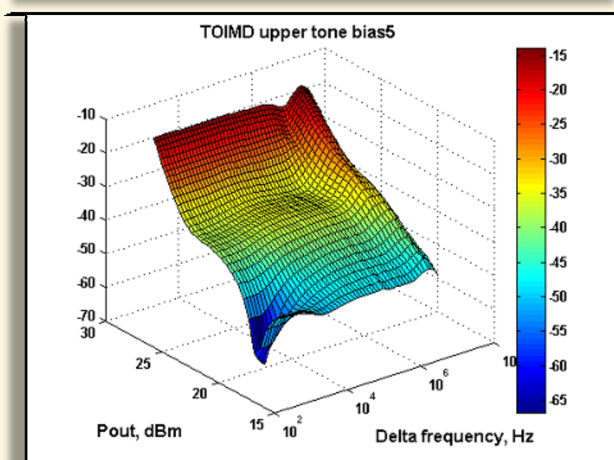
- 2 tone measurements with large inductor at drain
  - Increasing differens in lower and upper IMD product





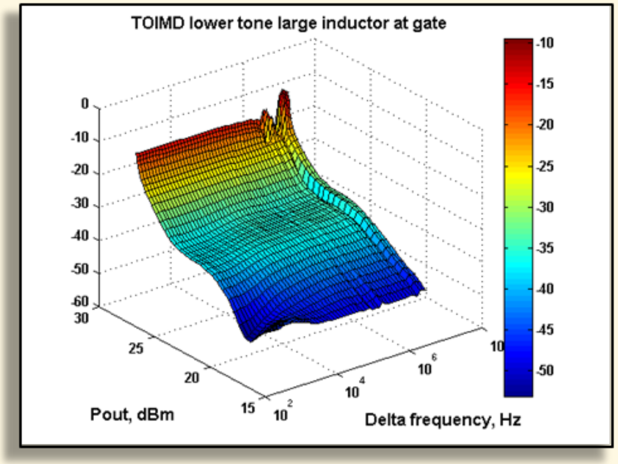
Bias circuit impedance drain



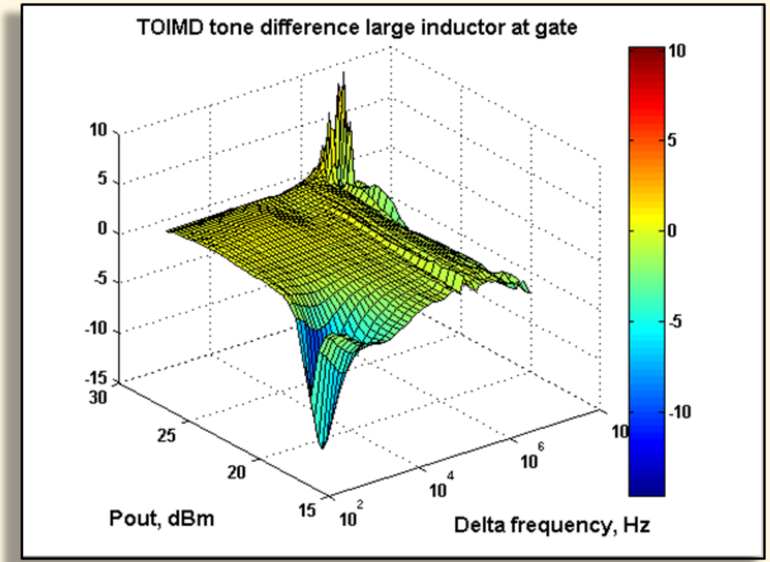


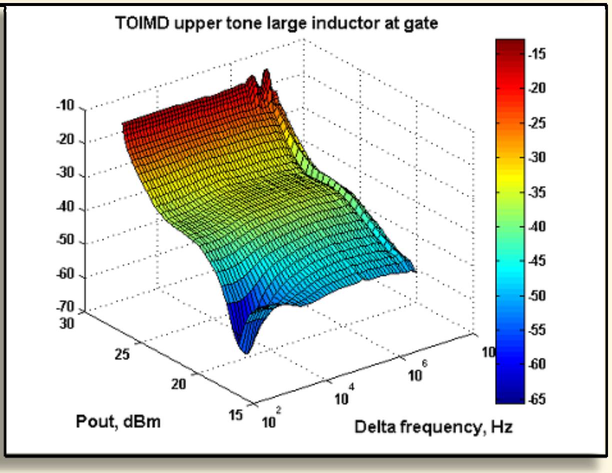
Experimental Results

- 2 tone measurements with large inductor at gate



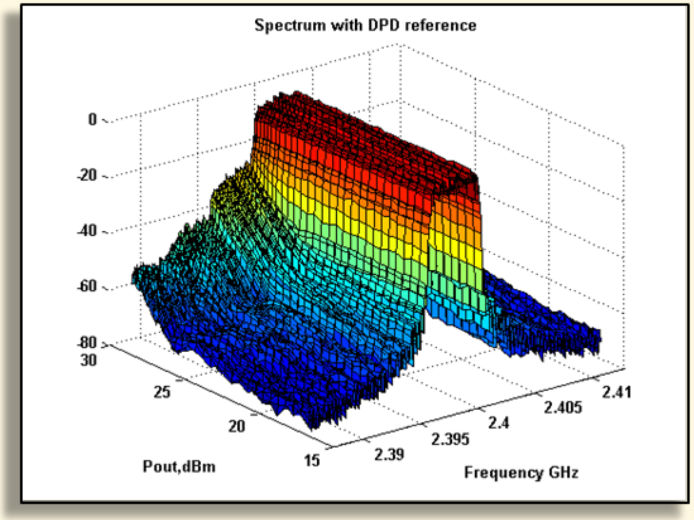
Bias circuit impedance gate

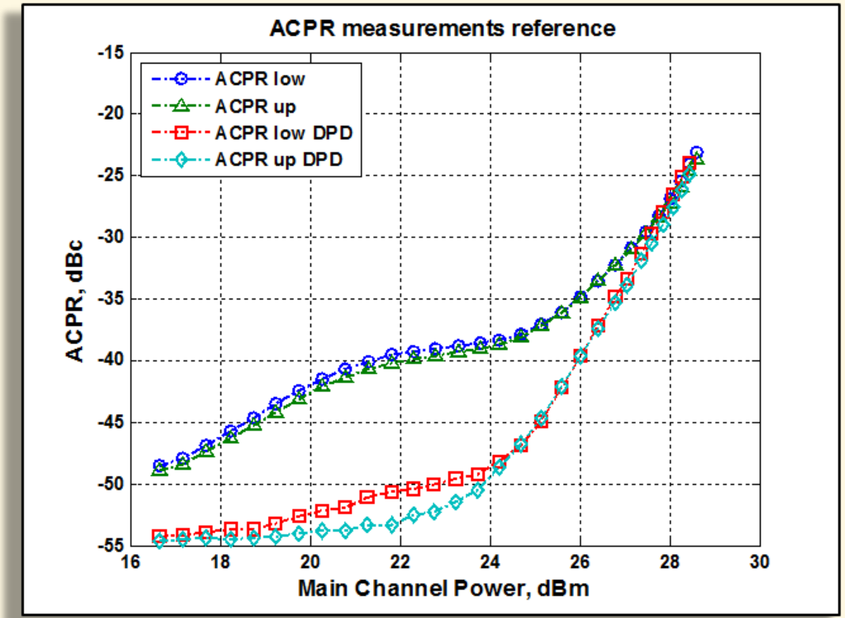


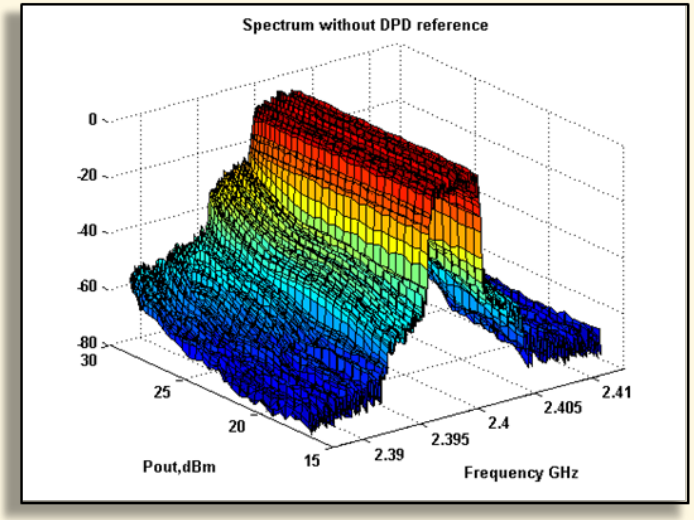


Experimental Results

- ACPR measurements with reference bias network
  - 16 QAM, symbolrate 3.84 MHz
  - About 10 dB improvement with DPD

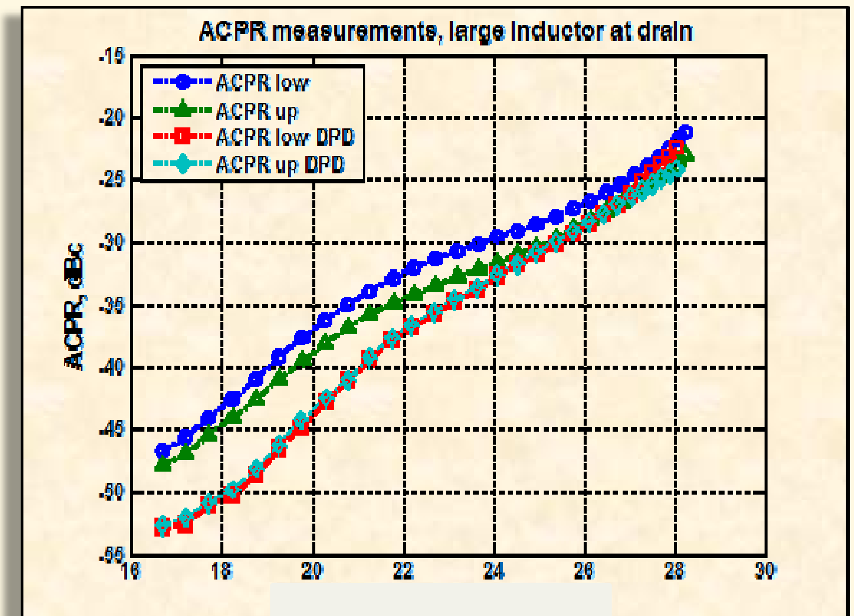


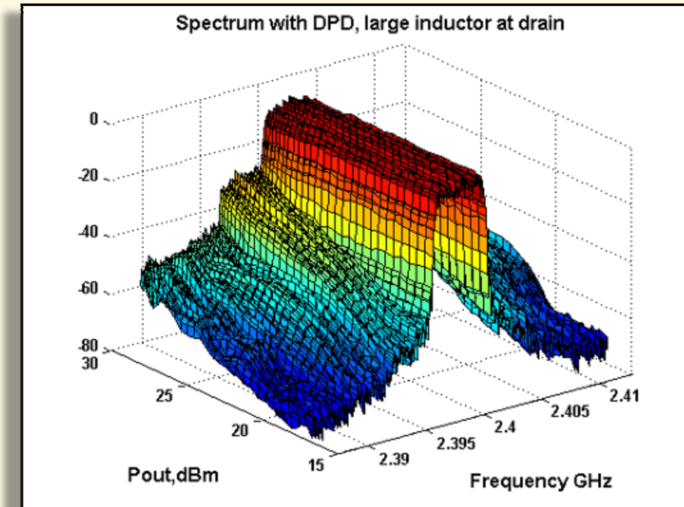


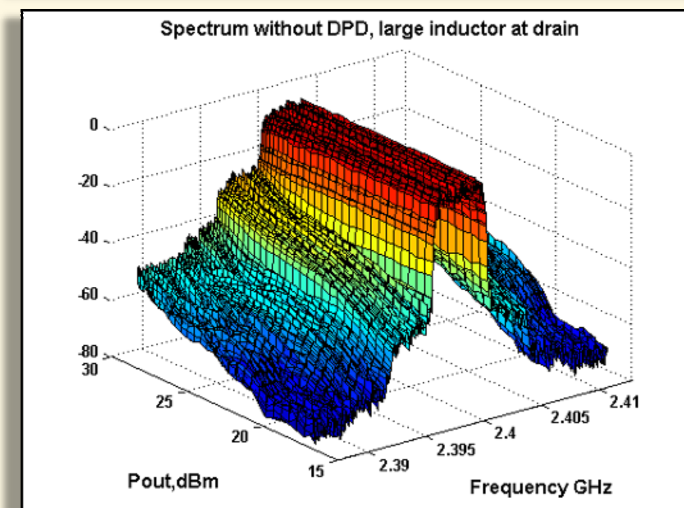


Experimental Results

- Linearity measurements with large inductor at drain
  - ACPR degraded
  - DPD not able to compensate due to memory/drain modulation

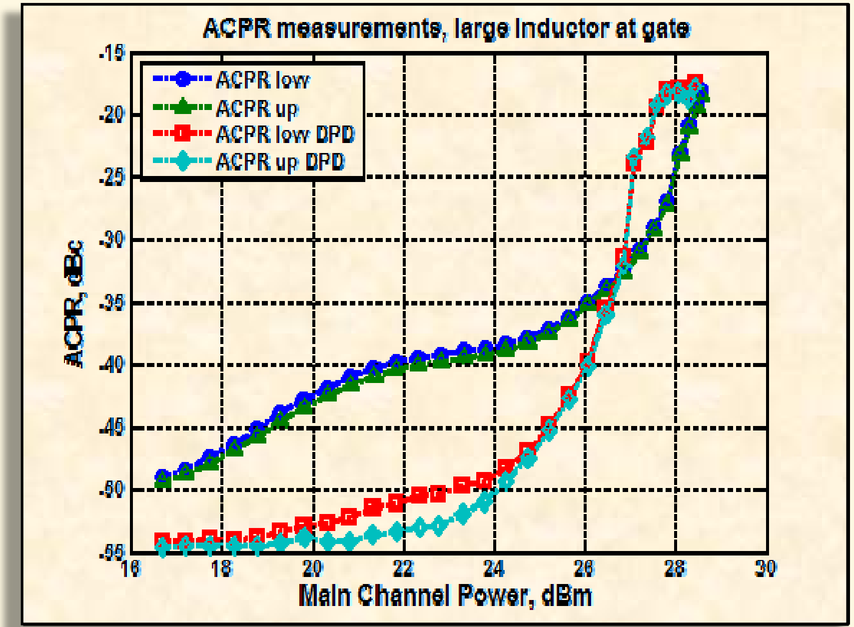


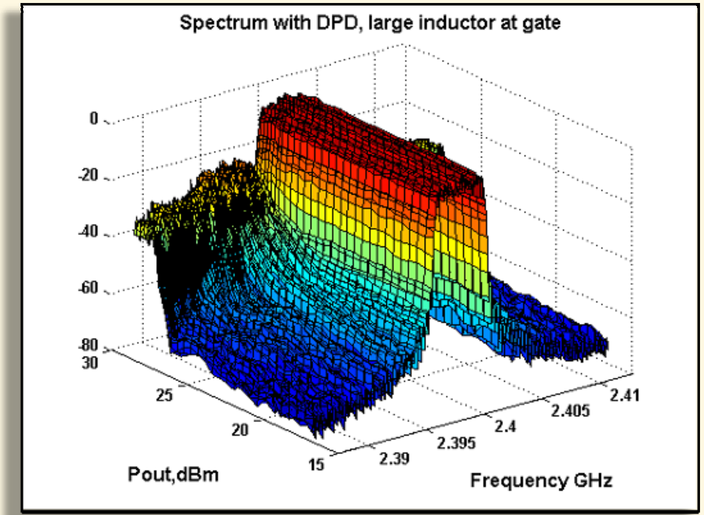


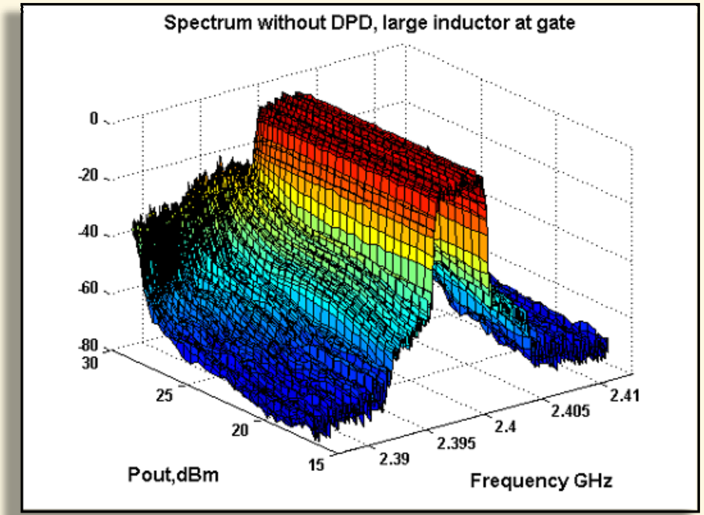


Experimental Results

- Linearity measurements with large inductor at gate
  - ACPR unchanged at low power levels
  - At high output power ACPR is drastically degraded

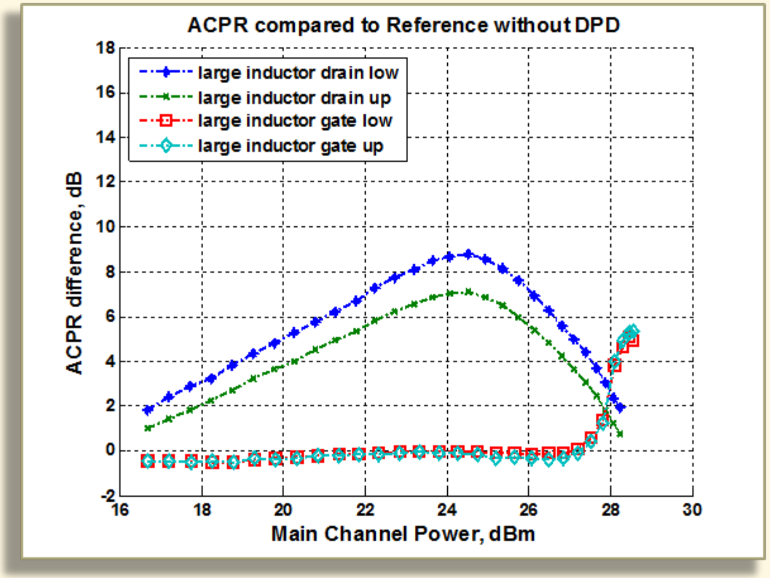


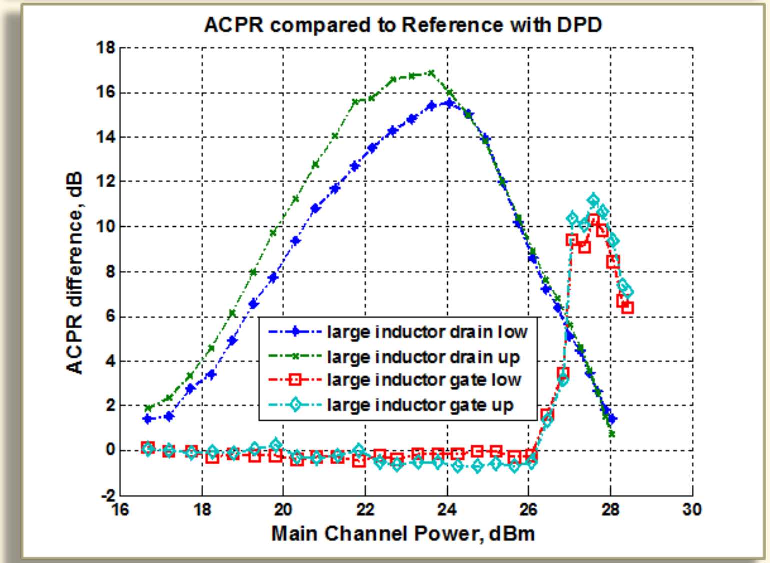




Experimental Results

- A large inductance at drain degrades the linearity, DPD cannot compensate for this
- A large inductance at gate doesn't affect the linearity at low power but has a significant impact at high power, gate modulation?





Conclusions

- A testbench for PA design is presented that includes automized measurements
- In addition to load-pull the effect of the bias network can be easily measured
- To demonstrate the importance of the bias circuits two extreme variants are tested and their effect of the linearity are measured
- Measurements show that large inductance at drain degrades the linearity as expected and that a simple memoryless DPD cannot compensate for this
- A large inductance at gate only affects the linearity at high power levels, gate modulation

Acknowledgement

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Thank you for your attention!