Layout-Optimization of Power-Devices

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imec

Outline

1. Problem + Nomenclature
2. Unit gatewidth
3. Thermal
4. Number of unit cells
5. EM-simulations

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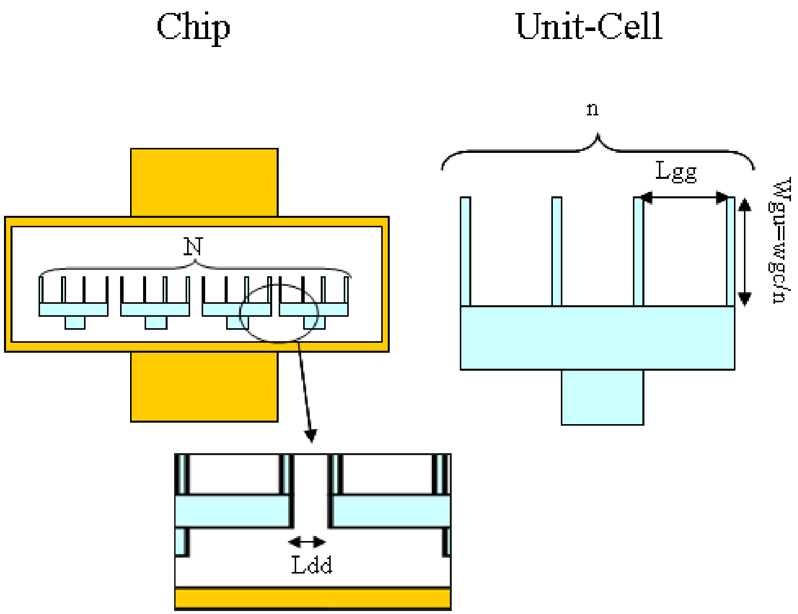
Problem Description + Nomenclature

- A device = N unit cells, each having n gate-fingers of length w_{gu}
- Total gatewidth is $w=N \times n \times w_{gu}$. And w~Pout
- Lgg=finger spacing

?: How to choose N,n,w_{gu},L_{gg},
-> EM effects
-> Thermal effects



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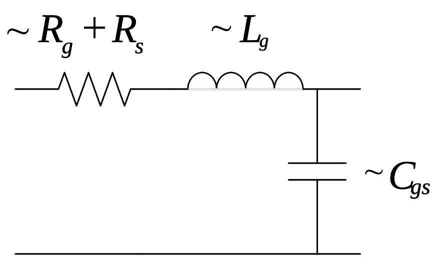
Unit gatewidth w_{gu}

- IDS – modulation: UNIFORM over the gate finger
- => Phase rotation & hence length must be limited.
- Finger ~ transmission line
  - voltage: $v(x,s) = \frac{Z_0(s)E_G(s)}{Z_0(s)+Z_G(s)} \cdot \frac{e^{-\gamma(s)x} + \Gamma_L(s)e^{-\gamma(s)(2L-x)}}{1-\Gamma_L(s)\Gamma_G(s)e^{-\gamma(s)2L}}$
  - difference in phase between $v(0,s)$ and $v(w_{gu},s)$ < $\pi/16$ imposes a limit to w_{gu}
  - γ (complex number):
    - Through simulation
    - By modeling an infinitesimal section of the line

Unit gatewidth w_{gu}

- γ (complex number):
  - Through simulation in Ansoft's HFSS
  - Infinitesimal section of the line; values from transistor extractions



$$\gamma = \alpha + j\beta = \sqrt{(R_g + R_s + j\omega L_g)\, j\omega C_{gs}}$$

- Resulting maximum values for w_{gu} in µm:

	HFSS	Extractions
2GHz	368	298
5GHz	236	188
10GHz	165	130

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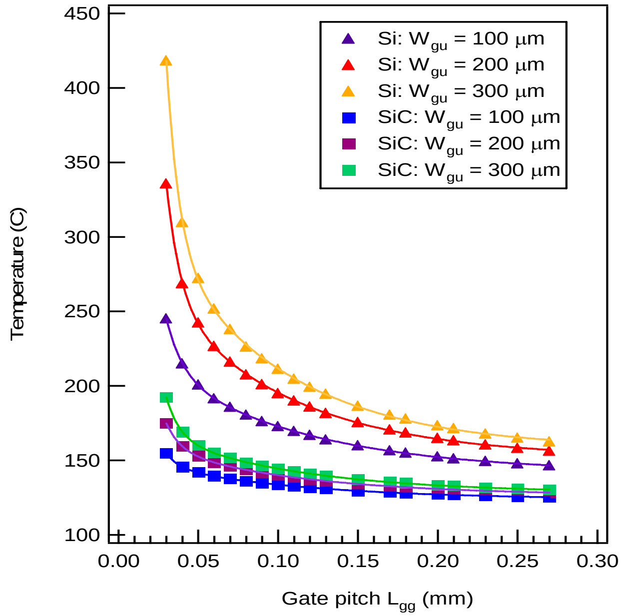
Thermal *Lgg*

- From a previous Imec study
  [J. Das et. Al, IEEE Trans. Electron Devices, 53 (11), pp. 2696-2702,2006]
  Relationship *Lgg*, Temperature and w_{gu} by means of 3D-simulations:



Limiting the temperature to 160 ºC imposes a minimum to L_{gg} for a certain w_{gu}

The longer the finger, the further they have to be separated from each other

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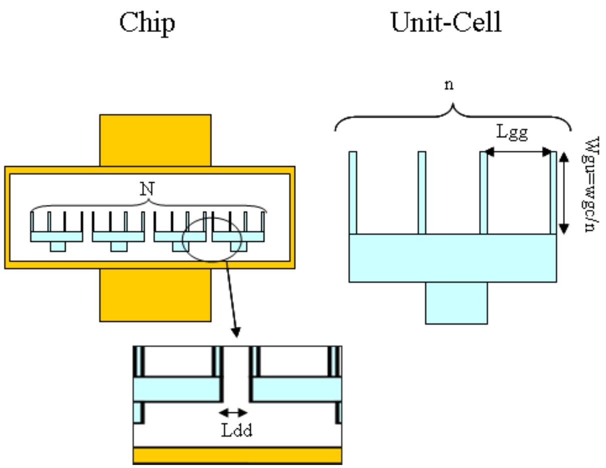
Number of unit cells *N* (and *n*)

- Choose that combination of *N*, *n* and w_{gu} that minimizes the chip area through

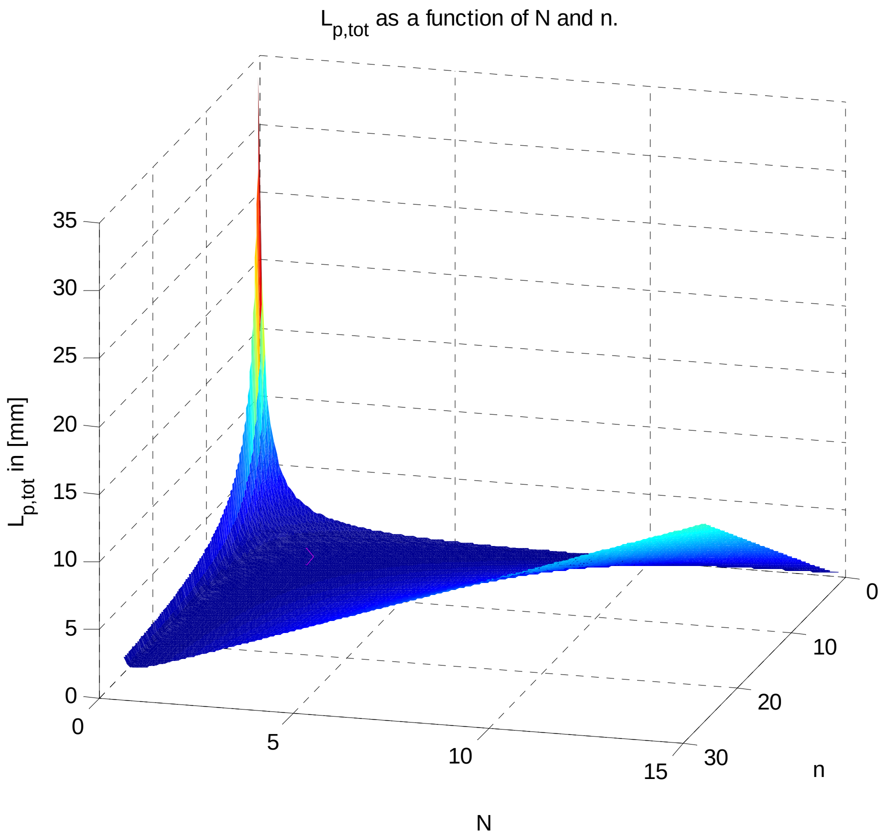
$$L_p = \frac{N}{2}(n-1)L_{gg} + \frac{w_g}{N \cdot n} + \frac{N-1}{2}L_{dd}$$



- … taking into account
  - *N* is integer and *n* is even
  - w_{gu} has a maximum
    => a minimum number of fingers is necessary
    => *N x n* has a minimum value
  - The cells are measurable by probes
    => *N* has a minimum value

- => Graphical method

Number of unit cells *N* (and *n*)



1. Projection of *Lp* on N,n-plane
2. Plot the discrete working grid (cyan diamonds)
3. w_{gu} has maximum
   N x n is minimum~hyperbole
4. On-wafer characterization
   Minimum value for *N*
5. Pick that point in the working area, where L_p is minimal.

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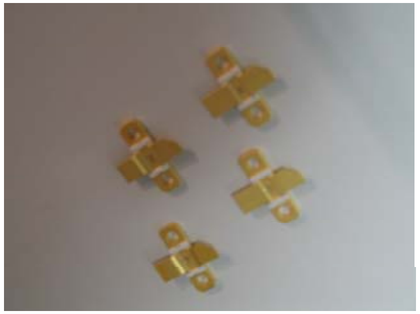
EM-simulations

- Devices in Microstrip Packages



- Gate,Source,Drain on top of die (CPW)
  <->
  Ground=bottom of MS Package

- Source-areas connected to bottom of MS Package:
  - Wirebonds
  - Via’s

- Source-Inductance kills performance

EM-simulations

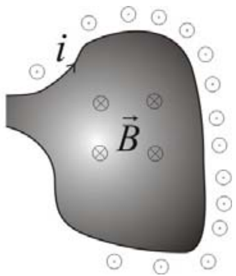
- Approximation of MAG:

$$G_{a\max} \cong \frac{\left(\frac{f_T}{f}\right)^2}{4G_{ds}\left(R_{gs} + R_s + R_g + \frac{\omega_T L_s}{2}\right) + 2\omega_T C_{gd}\left(R_{gs} + R_s + 2R_g + \omega_T L_s\right)}$$

L_s should be minimized

- L_s doesn't scale and is not predictable
  - Any L is proportional with area of membrane of mag flux
  - *Surface* is difficult to determine because
    - *More* than 1 via's or WB's (+ coupling)
    - *Common* for the gate-source path and drain-source path
    - *Airbridges*

$$L \sim \Phi \sim \iint \vec{B} \cdot d\vec{s}$$



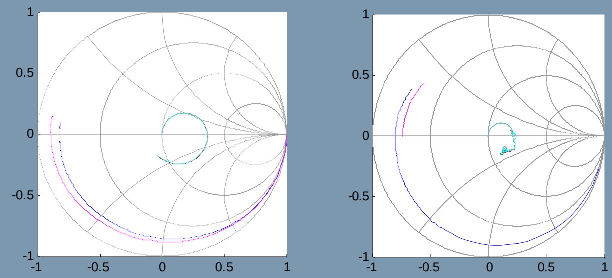
=> EM-simulations

EM-simulations

S-PARAMETERS

VG<VT

zero

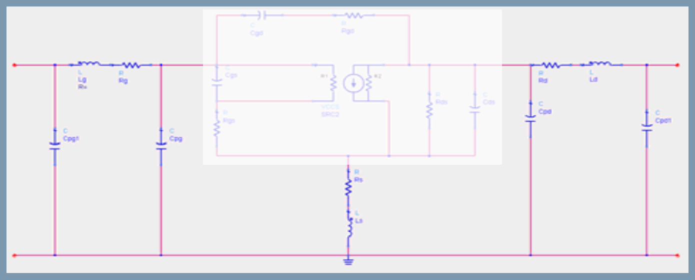


Measurements

3D Simulations (HFSS)

Extraction Procedure

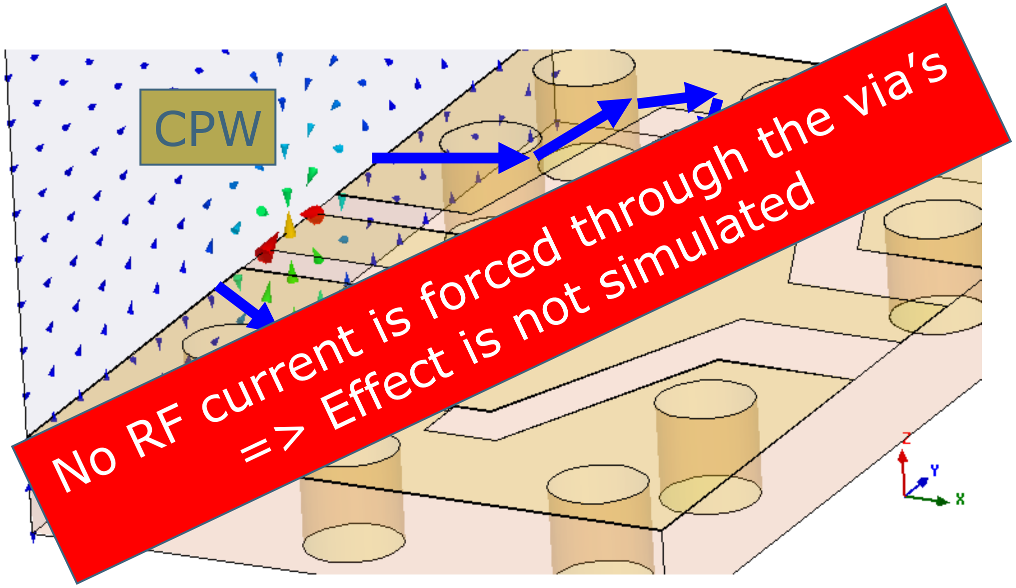
EQUIV. CIRCUIT



Extrinsics (ao L_s)

EM-simulations

- Effect of via’s <=> they conduct RF Current
  Excitation of waveports is key



EM-simulations

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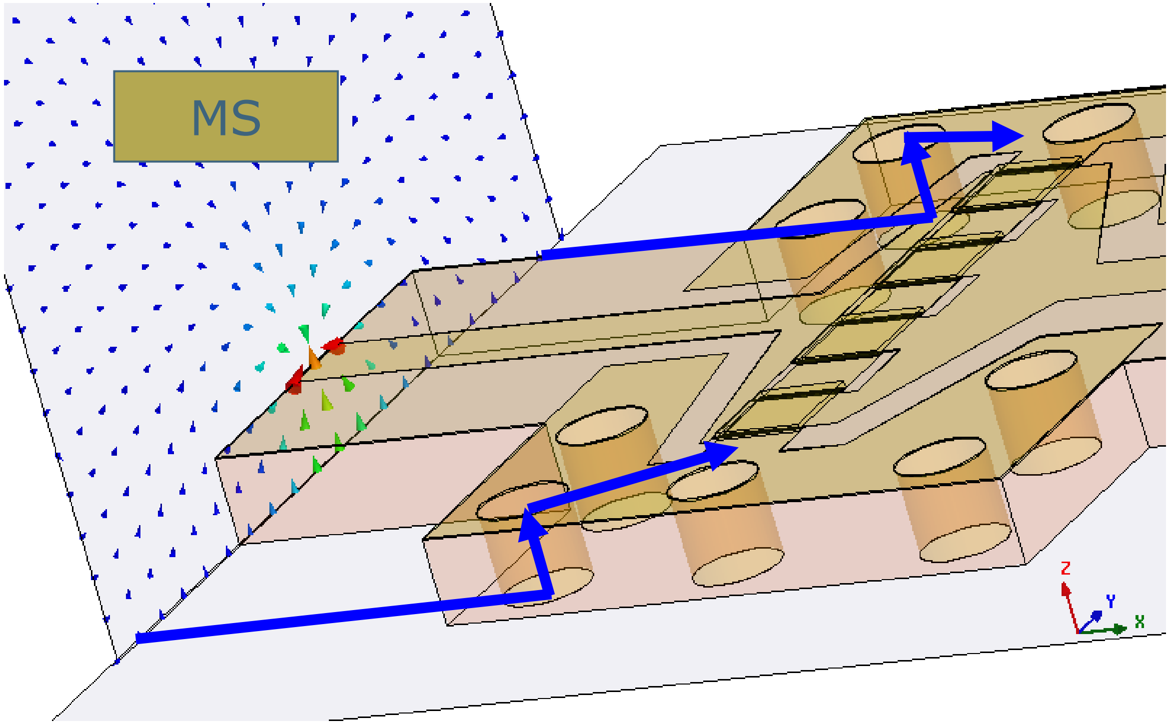
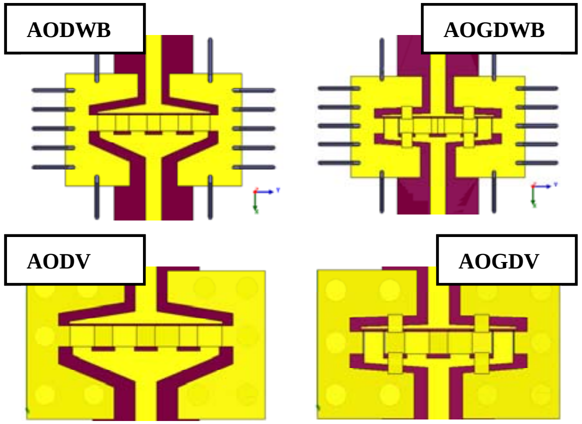
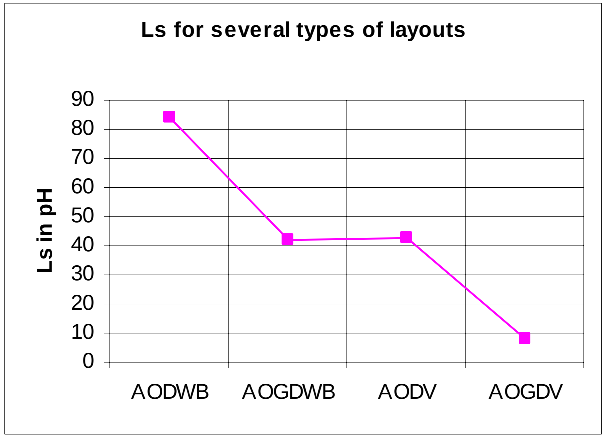
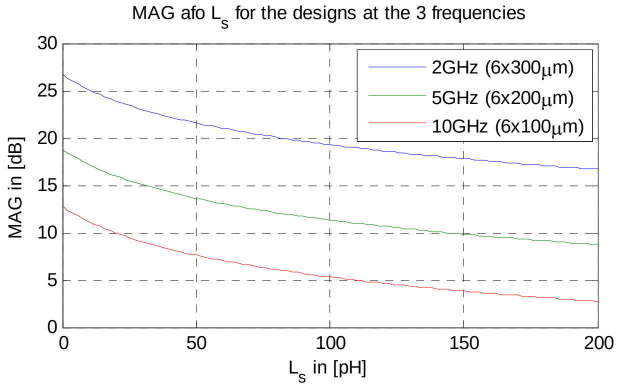


EM-simulations

- Applied to 4 configurations







$$G_{a\,max} \cong \frac{\left(\frac{f_T}{f}\right)^2}{4G_{ds}\left(R_{gs}+R_s+R_g+\frac{\omega_T L_s}{2}\right)+2\omega_T C_{gd}\left(R_{gs}+R_s+2R_g+\omega_T L_s\right)}$$

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