Monolithic lumped-element unequal branch-line coupler for the use in asymmetrical Doherty amplifiers

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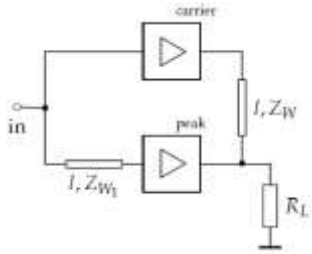
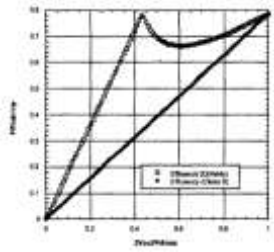
Agenda

- Introduction
  - Doherty amplifiers
  - Active load-pull principle
- Unequal lumped element power splitter design
- Simulation and measurement results
- Summary
- Outlook

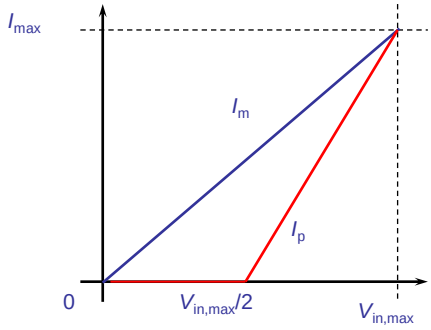
Doherty amplifiers

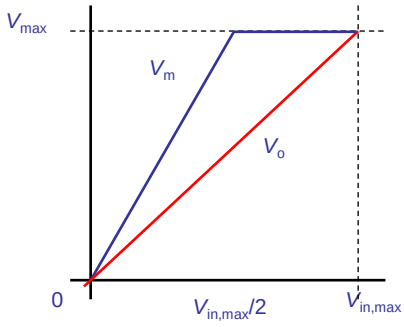




- Doherty amplifiers provide good efficiency for envelope modulated signals
- High efficiency in back-off
- State-of-the-art amplifier for wireless communication infrastructure
- Size constrains for monolithic integration

Active load-pull principle



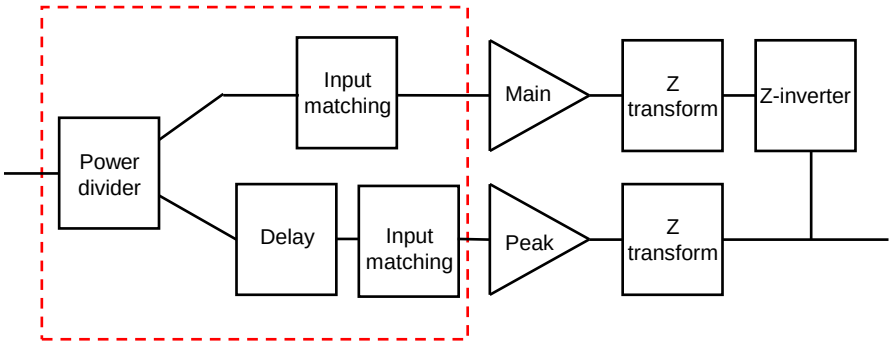


- Peaking device has to deliver the same current as the main device
- With half of input drive level

Implementation issues

- Different device peripheries
  - Size ratio is factor 2 or greater
  - Acceptable for MMICs
  - Different impedance level
- Bias control of peaking amplifier
  - Identical devices
  - Bias adaptation according to instantaneous input drive amplitude
  - Use digital signal processing unit
- Unequal input power splitting
  - Identical devices
  - Similar matching networks
  - Performance tuning with splitting ratio
  - Reduced gain

MMIC input circuitry

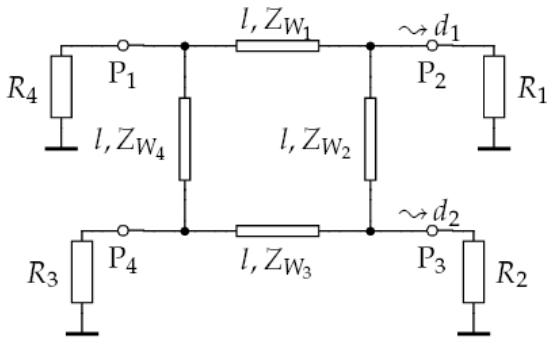


DPA input circuitry tasks

- Splitting of the input signal
  - Equal splitting
  - Unequal splitting
- Phase compensation for output impedance inverter
- Impedance matching
- Individual biasing of the two transistors

Modified branch-line hybrid coupler

Unequal power splitting



$$Z_{W1} = \sqrt{\frac{R_1 R_2 d_1^2}{d_1^2 + d_2^2}}$$

$$Z_{W2} = \sqrt{R_2 R_3}\frac{d_1}{d_2}$$

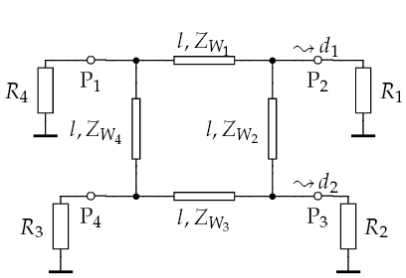
$$Z_{W3} = \sqrt{\frac{R_3 R_4 d_1^2}{d_1^2 + d_2^2}}$$

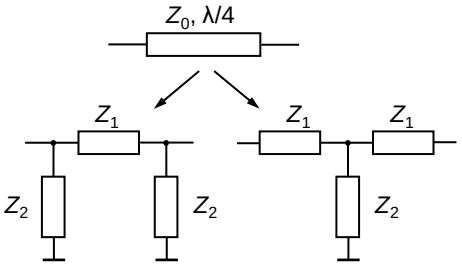
$$Z_{W4} = \sqrt{R_4 R_1}\frac{d_1}{d_2}$$

$d_1 = 10^{P/20}$ fraction of input power available at port 2

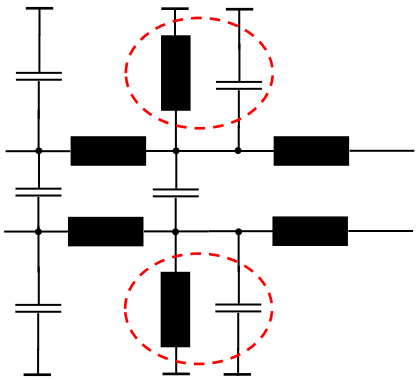
Lumped element approach

- Shrink the size of the coupler
  - Replacement of transmission lines with lumped elements
  - Minimise number of inductors
  - Provide two independent DC paths



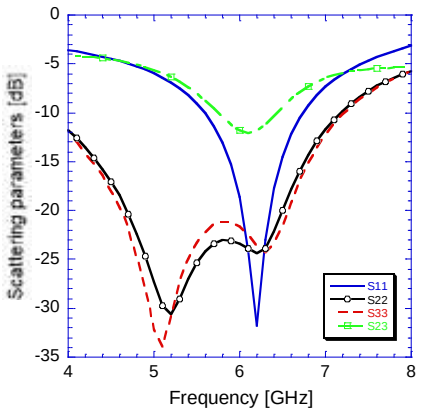


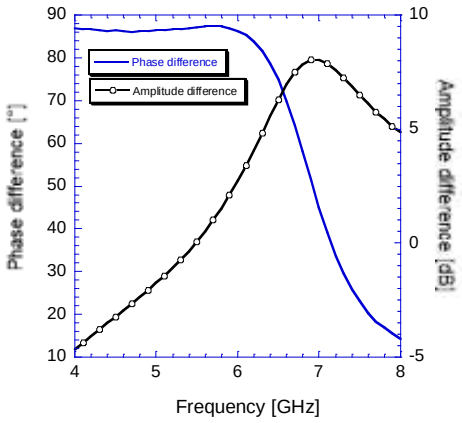
Topology used



- Minimum number of inductors
  - Small size
  - Low loss
- Independent biasing of both transistors
  - External biasing

Simulation results



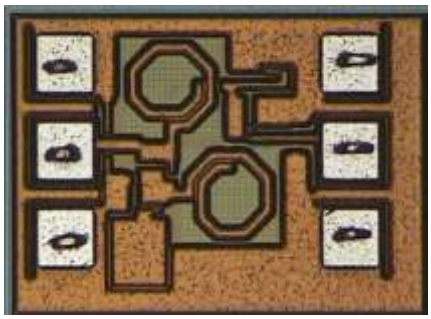


- **Design freq.: 5.8 GHz**
- **Isolation: 10.4 dB**

- **Amplitude diff.: 1.5 dB**
- **Phase diff.: 85.3°**

Implementation at 5.8 GHz

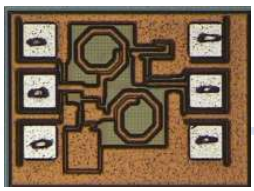
IBM BiCMOS 6HP

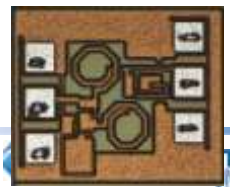


- SiGe HBT f_t = 47GHz
- 0.18 µm CMOS
- 4 µm-thick top metallization
- 10 µm dielectric stack
- 300 mm Si wafer

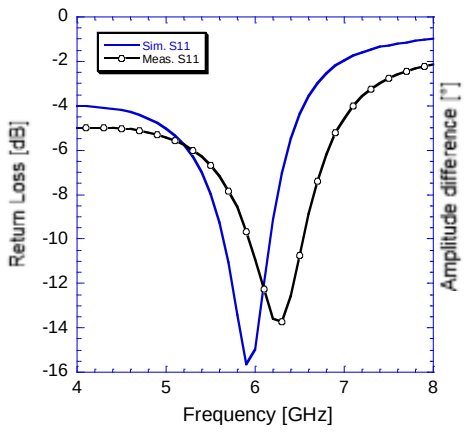
Characterisation issues

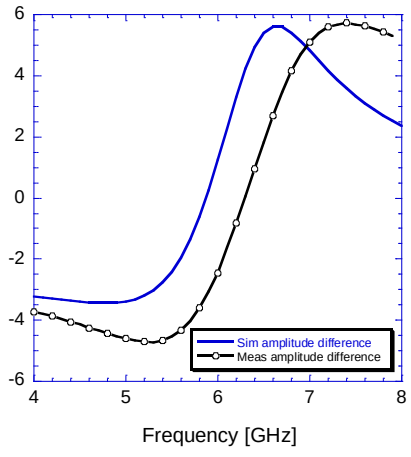
- Complex impedances
  - Performance comparison with simulation results in the same test set up
- Only two probes available
- Four terminal device
  - Two terminals terminated in 50 Ω on chip
  - Two chips required
    - Slight difference in performance





Measurement results





Summary

- Unequal lumped element hybrid coupler
  - Arbitrary output resistance
- Combination of power divider and input matching for DPA input circuitry
  - Complex output impedances
  - Reduction of component count
  - Size reduction
  - Cost efficient implementation
- Simulation and measurement results