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57-65GHz CMOS Power Amplifier Using Transformer-Coupling and Artificial Dielectric for Compact Design

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PA Symposium
1/20/09

Overview

- Introduction
- Design Overview
- Differential Design
  - Transmission Line Technology
  - Artificial Dielectric and Output Matching
  - Differential and Common-Mode Stability
- Transformer
  - Basics
  - Combine Matching, Bias and Stability Networks
- RF Performance
- Layout

60GHz Motivation

- Released standards for unlicensed 57-65GHz spectrum:
  - IEEE 802.15.3c, ECMA, WirelessHD, IEEE 802.11VHT
  - Very limited success: “Last-mile” efforts, LMDS, 77GHz Automotive, 71-76GHz and 81-86GHz point-to-point
  - Military (AEHF cross-link) and science applications dominate
- New commercial applications
  - Uncompressed wireless video transfer: “in-room”, Wireless HDMI
  - Short distance bulk data transfer: “near-field”, <1m
    - P2P (Portable-to-Portable), M2M (Machine-to-machine), Proximity Communication, Wireless hard drive backup
- Availability of standard digital CMOS process
  - High f_t (>120GHz) for 90nm gate length
  - Silicon roadmap http://www.itrs.net predicts 37nm f_t > 360GHz
  - Passive element Q’s are reasonable
  - Do not have to rely on expensive, but high-performance GaAs or InP

Power Amplifier

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- Typical millimeter-wave power amplifiers
  - Expensive, but high-performance GaAs/InP
  - Single-ended
  - Transmission line based with $\lambda/4$ structures, such as Lange or Wilkinson couplers.
  - Difficult matching impedances, extremely low.
- Millimeter-wave CMOS PAs
  - Limited publications.
  - Similar architecture to GaAs design; same disadvantages
  - Low 1.2V supply voltage (knee voltage problematic)
  - Low f_t
  - Lossy substrate, low-Q passive elements
  - Single-digit efficiencies
- Goals and Achievements
  - Double-digit efficiencies above 15% and Pout > 12dbm
  - Compact design: 80% percent reduction from standard design

Schematic

1. Transformer interstage and input matching

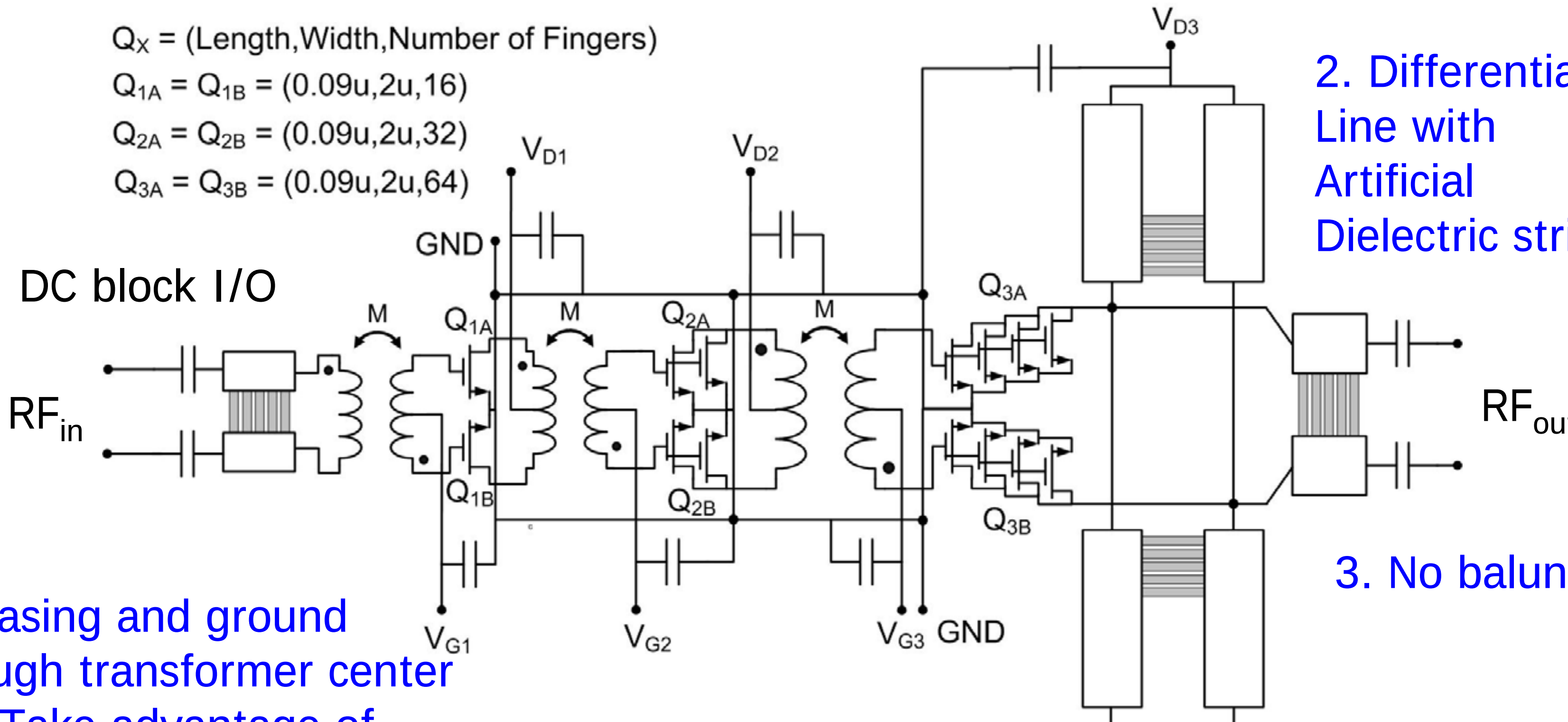
2. Differential Line with Artificial Dielectric strips

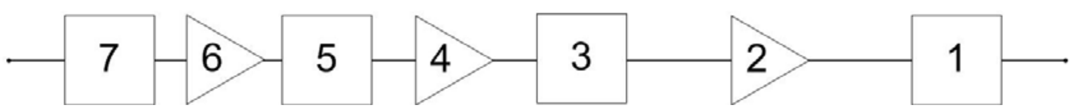
3. No balun

4. Low loss output match network

5. Biasing and ground through transformer center tap. Take advantage of virtual grounds.

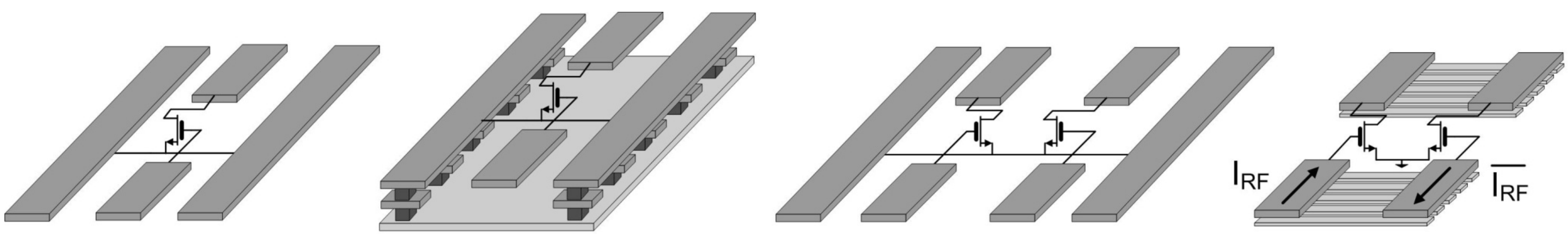
6. DC block I/O





Differential Transmission Line

- CPW (a) and Shield Microstrip (b) are single-ended.
- GSSG (c) is pseudo-differential
  - Need 4-port network analyzer
  - Large Signal testing difficult: magic-T, transitions, amps, etc.
  - Need off or on-chip balun which is lossy
- GS (d)
  - True differential
  - Compact , 3dB more power with negligible area increase
  - Artificial dielectric strips



(a) CPW (b) Shielded μ-strip (c) GSSG (d) GS [Differential] with Artificial Dielectric

CMOS Artificial Dielectric

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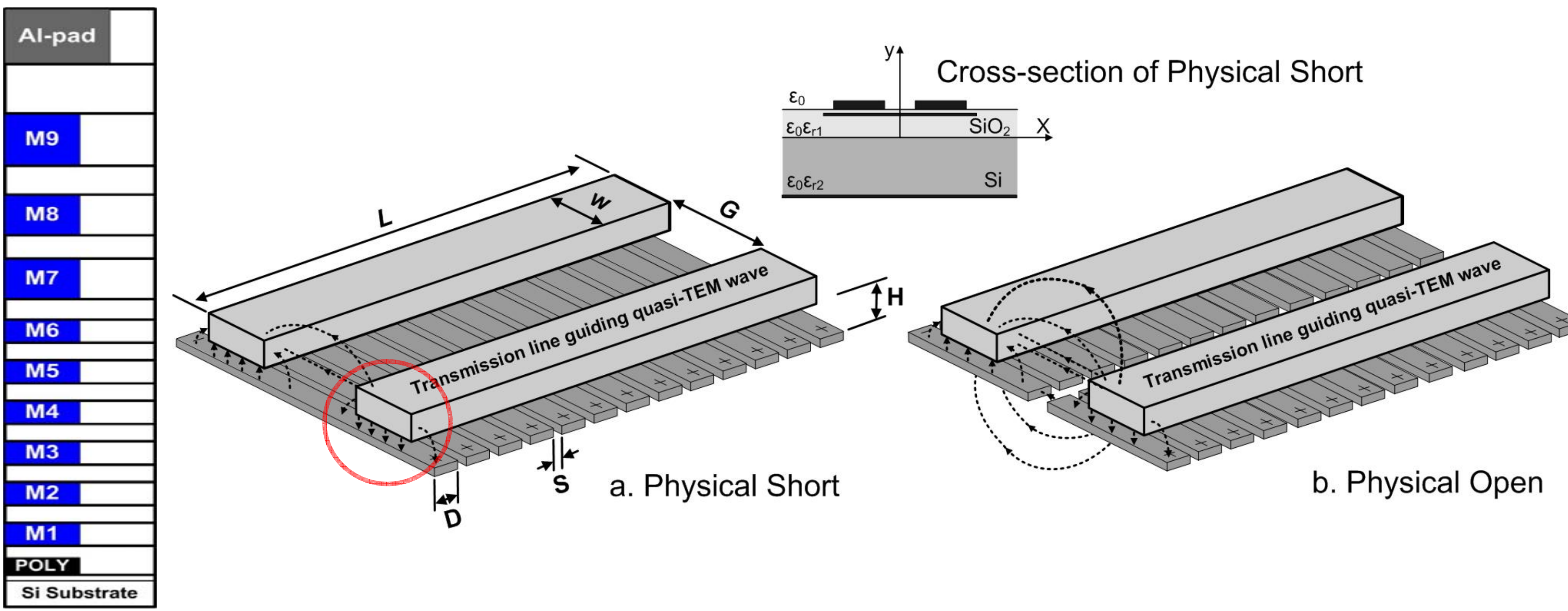
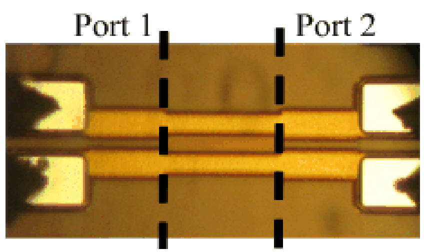
- Method to artificially increase the dielectric constant, and reduce the wavelength. (1948 for antenna lenses, Dr. Kock)
- CMOS is a mutiple metal interconnect process (UMC 1P9M 90nm is a 9 metal layer process)
- Insert floating metal strips directly underneath **differential** transmission line (DTL) to reduce length by increasing $\varepsilon_{r,eff}$

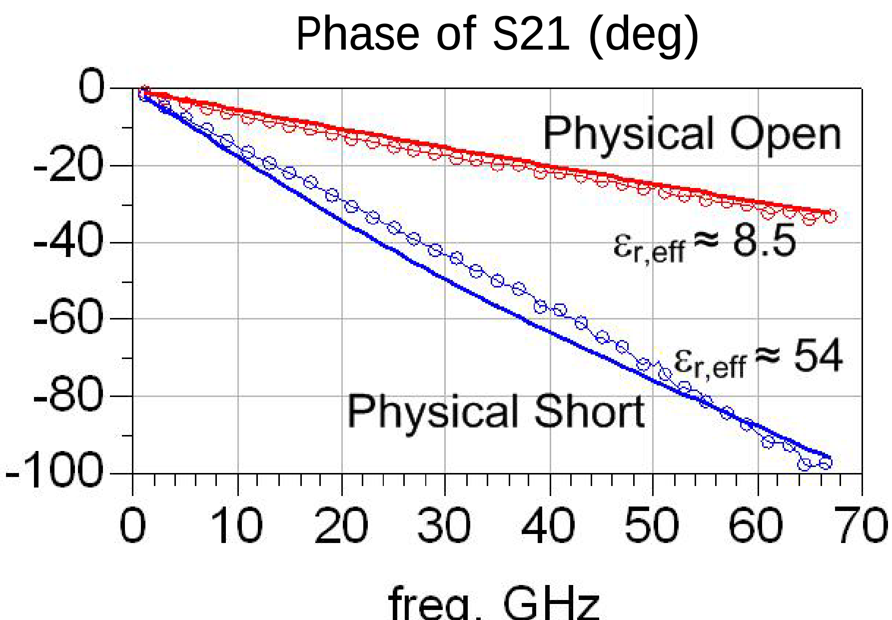


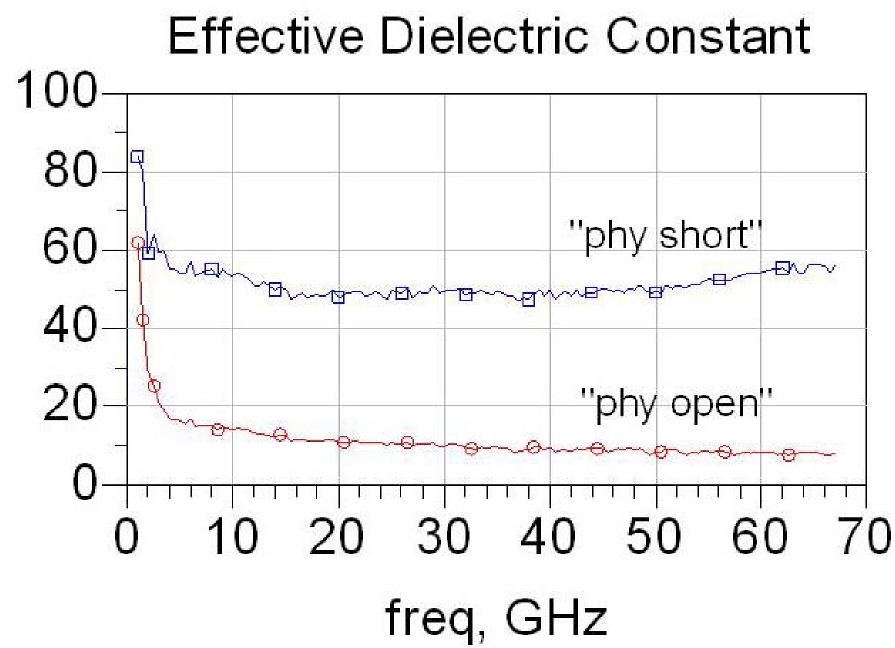
Phase Shift

- Large phase shift versus “physical short” and “physical open” differential transmission lines.
- Result is a 6X increase in the effective dielectric constant.



L	152μm	D	3μm
W	24μm	S	0.5μm
G	20μm	H	0.5μm

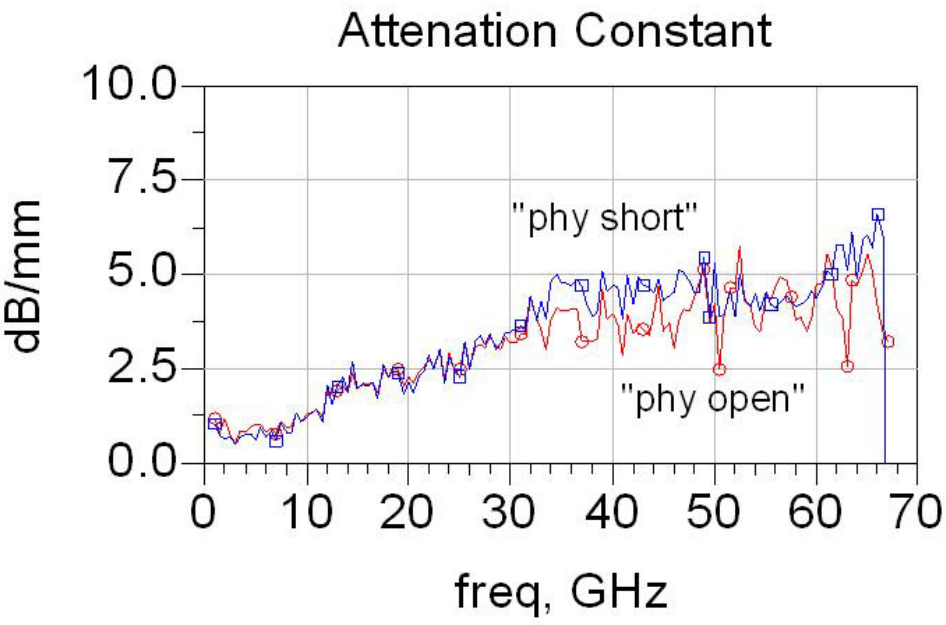


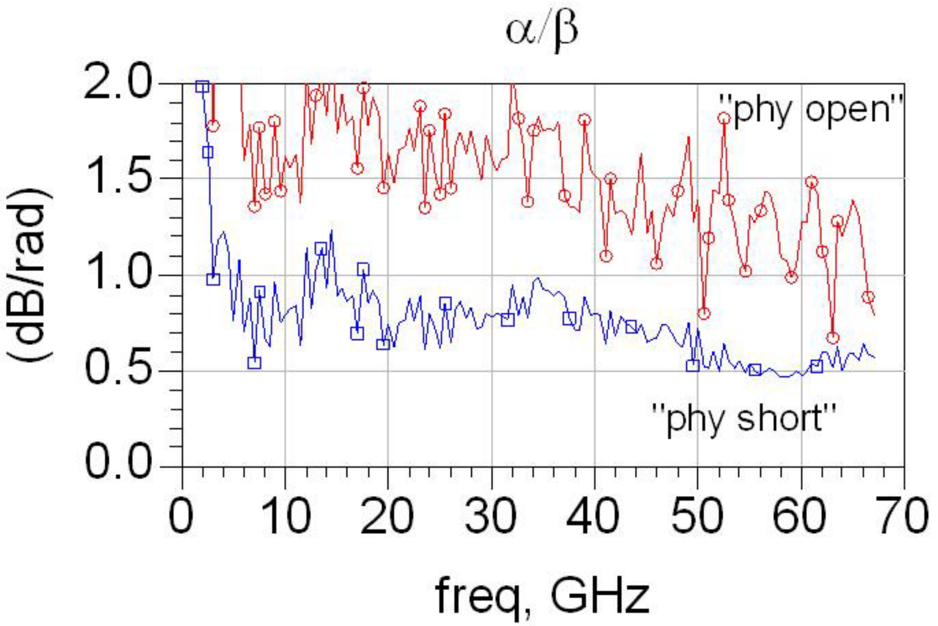


Simulation (SONNET) is solid line and measurement indicated by circles

Attenuation

- Measured attenuation is similar
- Greater than 2X benefit in α/β when compared with $\varepsilon_{r,eff}$

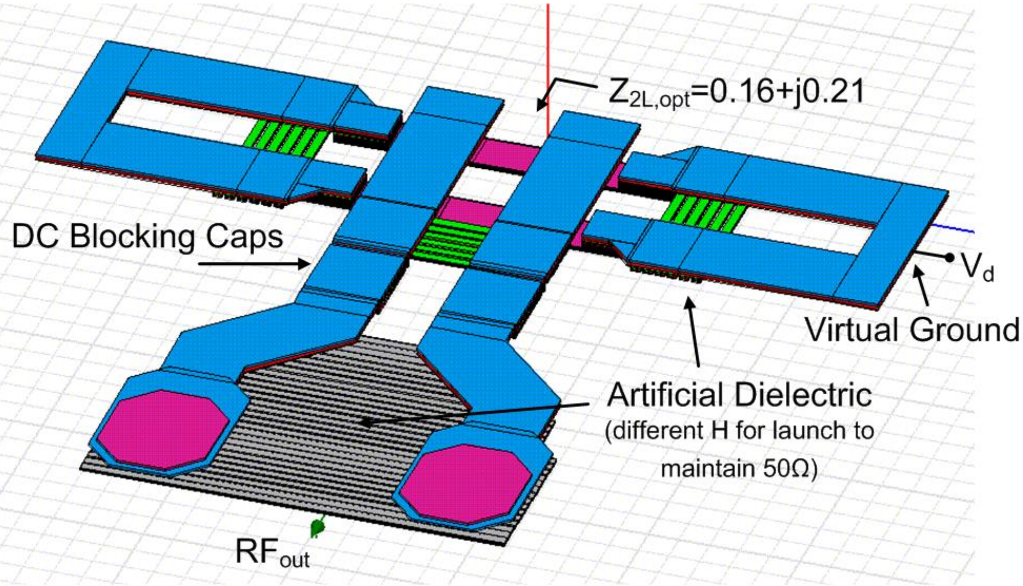


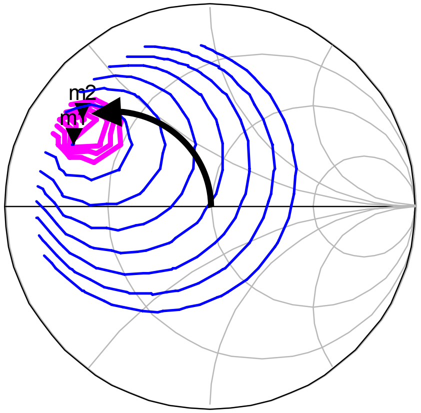


Artificial Dielectric Output Match

- Symmetric short-circuited stub output match.
- Artificial dielectric used for design and further compact layout
- DTL offers less loss than transformer

Output Match Layout





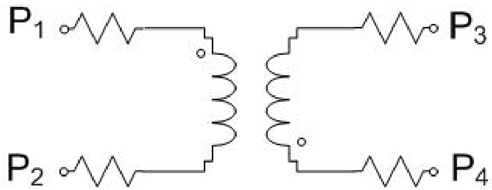
indep(PAE_contours_p) (0.000 to 15.000)
indep(Pdel_contours_p) (0.000 to 55.000)

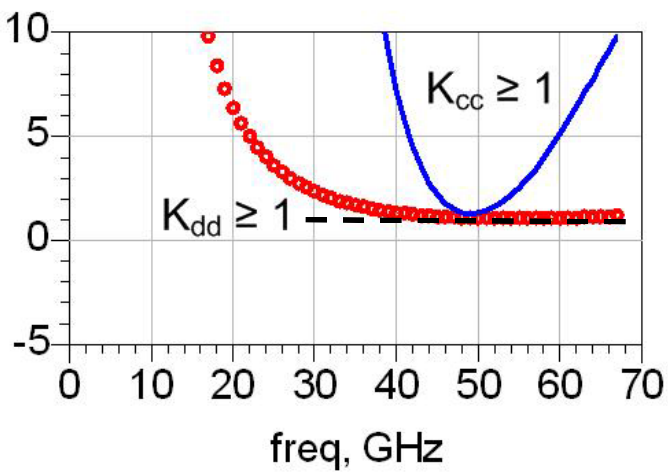
Artificial dielectric strips are further from S.C. end. ~15% size reduction.

Differential and Common-Mode Stability

- Difference between GSSG and GS approach.

GS Transformer





Stable

Stability Factor, K

$$K_{cc} = \frac{1 - |S_{c1c1}|^2 - |S_{c2c2}|^2 + |\Delta_{cc}|^2}{2|S_{c2c1}S_{c1c2}|}$$

$$K_{dd} = \frac{1 - |S_{d1d1}|^2 - |S_{d2d2}|^2 + |\Delta_{dd}|^2}{2|S_{d2d1}S_{d1d2}|}$$

$$\Delta_{xx} = S_{x1x1}S_{x2x2} - S_{1x2x}S_{2x1x}$$

$$S_{d1d1} = \frac{1}{2}(S_{11} - S_{21} - S_{12} + S_{22})$$

$$S_{d1d2} = \frac{1}{2}(S_{13} - S_{23} - S_{14} + S_{24})$$

$$S_{d2d1} = \frac{1}{2}(S_{31} - S_{41} - S_{32} + S_{42})$$

$$S_{d2d2} = \frac{1}{2}(S_{33} - S_{43} - S_{34} + S_{44})$$

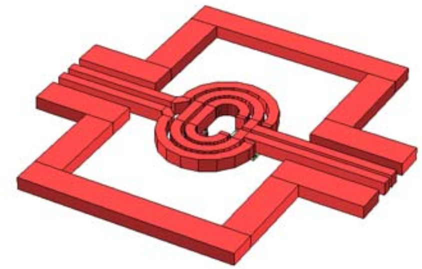
$$S_{c1c1} = \frac{1}{2}(S_{11} + S_{21} + S_{12} + S_{22})$$

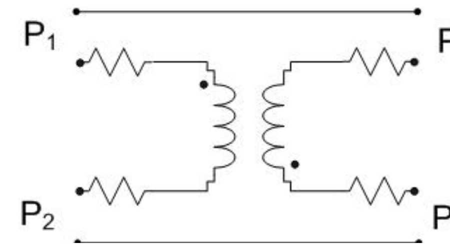
$$S_{c1c2} = \frac{1}{2}(S_{13} + S_{23} + S_{14} + S_{24})$$

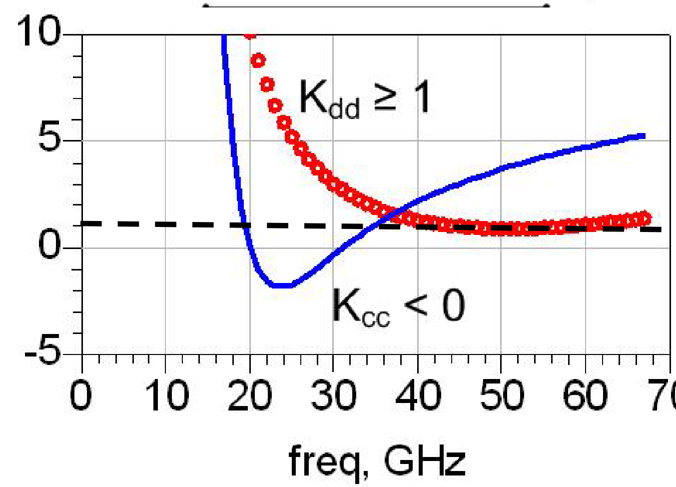
$$S_{c2c1} = \frac{1}{2}(S_{31} + S_{41} + S_{32} + S_{42})$$

$$S_{c2c2} = \frac{1}{2}(S_{33} + S_{43} + S_{34} + S_{44})$$

GSSG Transformer (Gnd ring)







Unstable

Device

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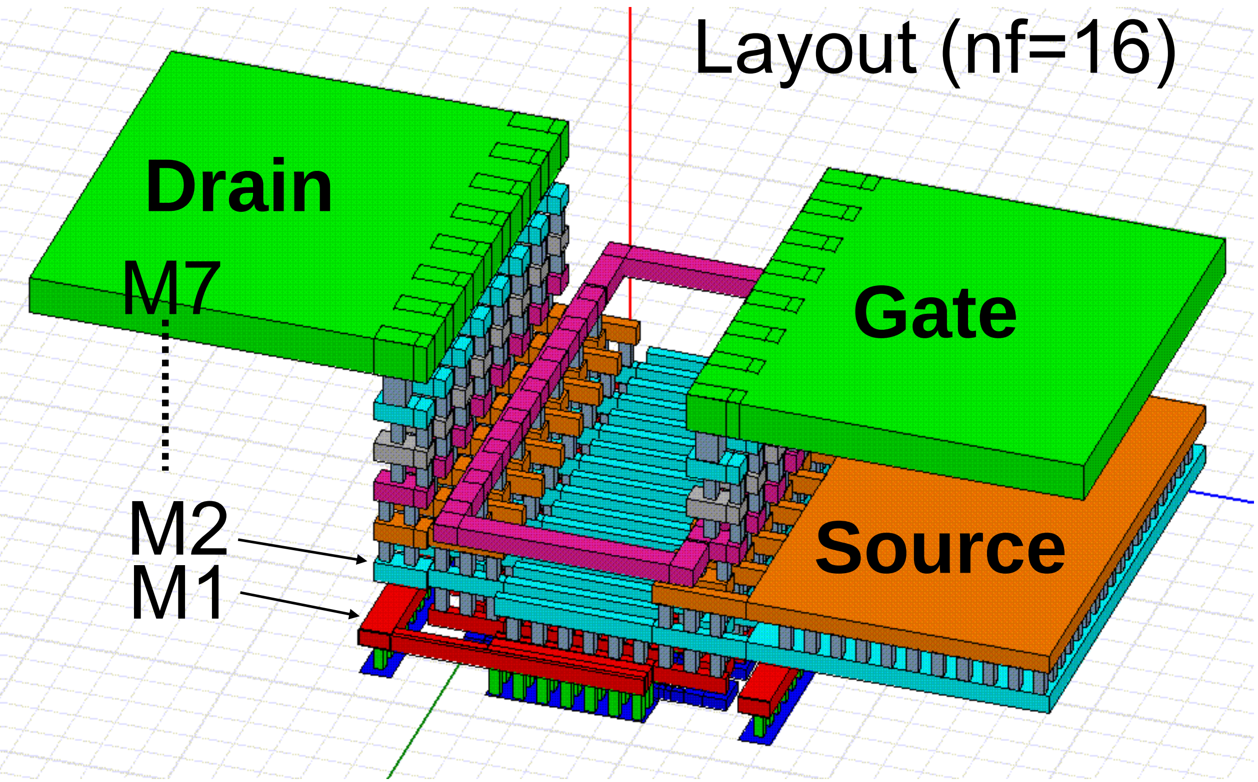
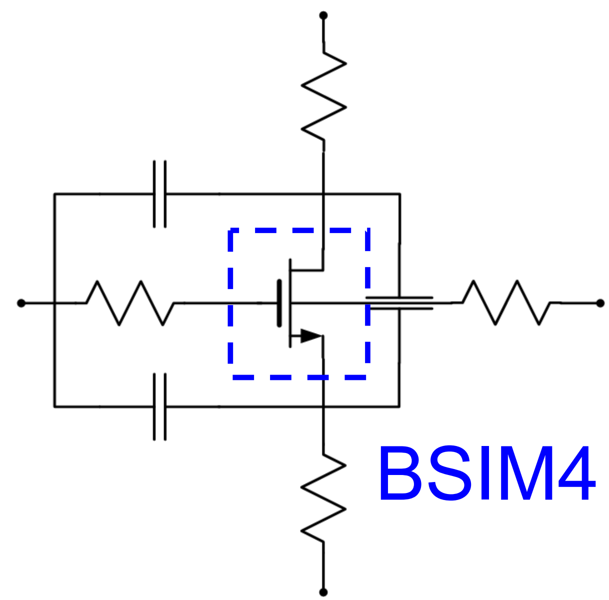
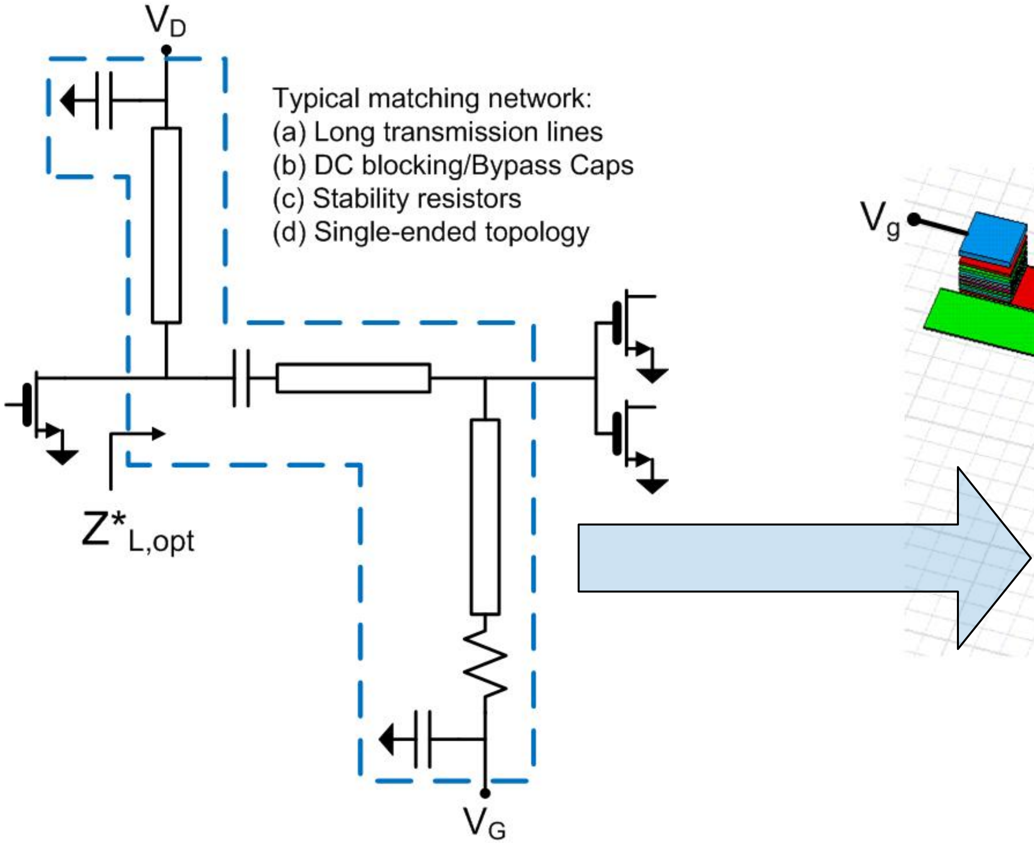
- W_g = 2um (nf=16,32,64) for Max. Stable Gain.
- Source and drain fingers are layered from M1-M2.
- BSIM4 overlaid with RF layout model (R_g, C_{ext} …)
- Be careful of gate resistance in foundry BSIM models

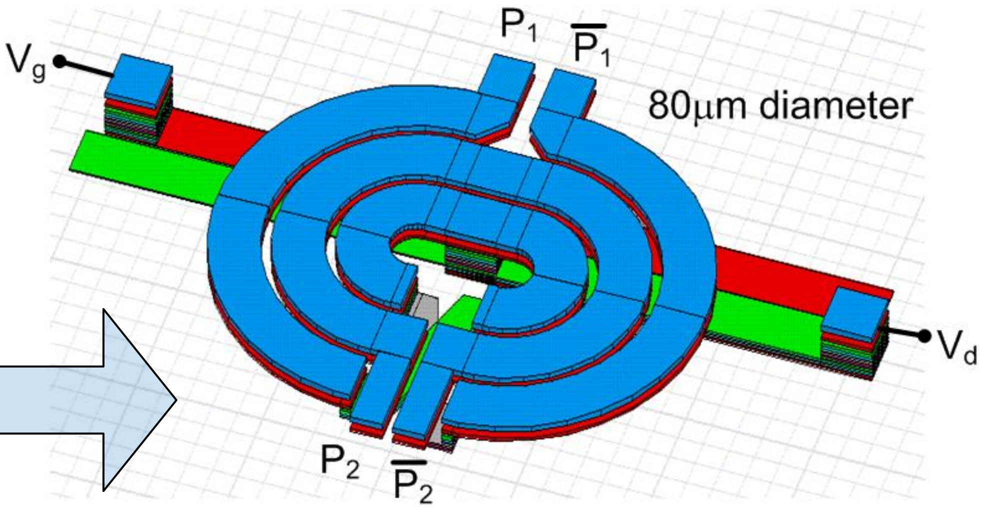




Transformer Element

- Transformer replaces typical matching network.
  - Inter-stage impedance matching
  - Biasing through virtual ground taps
  - Stability (K-factor)
  - Compact Layout (no lengthy chokes or matching elements)

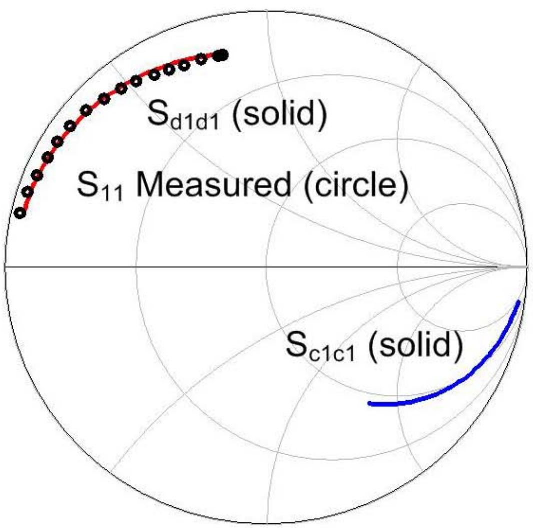




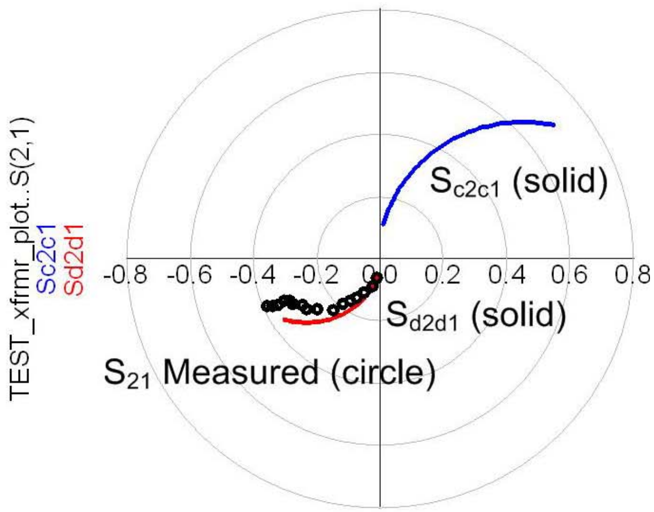
Transformer: S-parameters

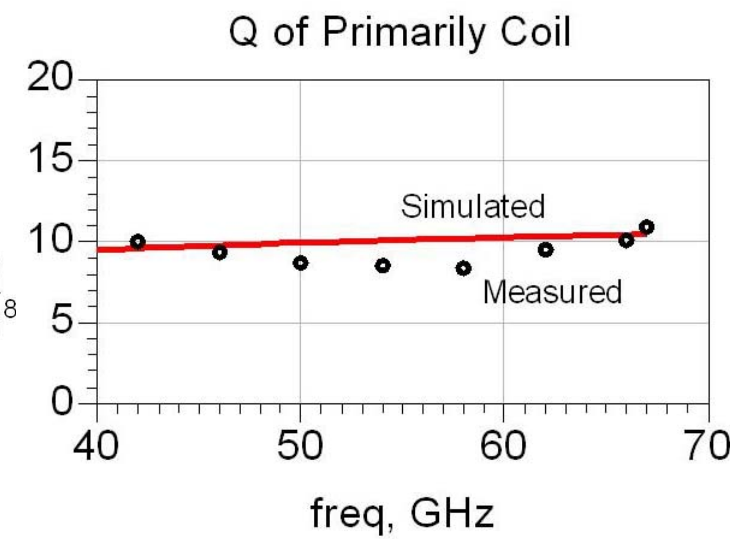
- Good agreement between simulation and test differential S-parameters.
- $Q_{primary} \approx 10$ and k (coupling factor) ≈ 0.6

S11



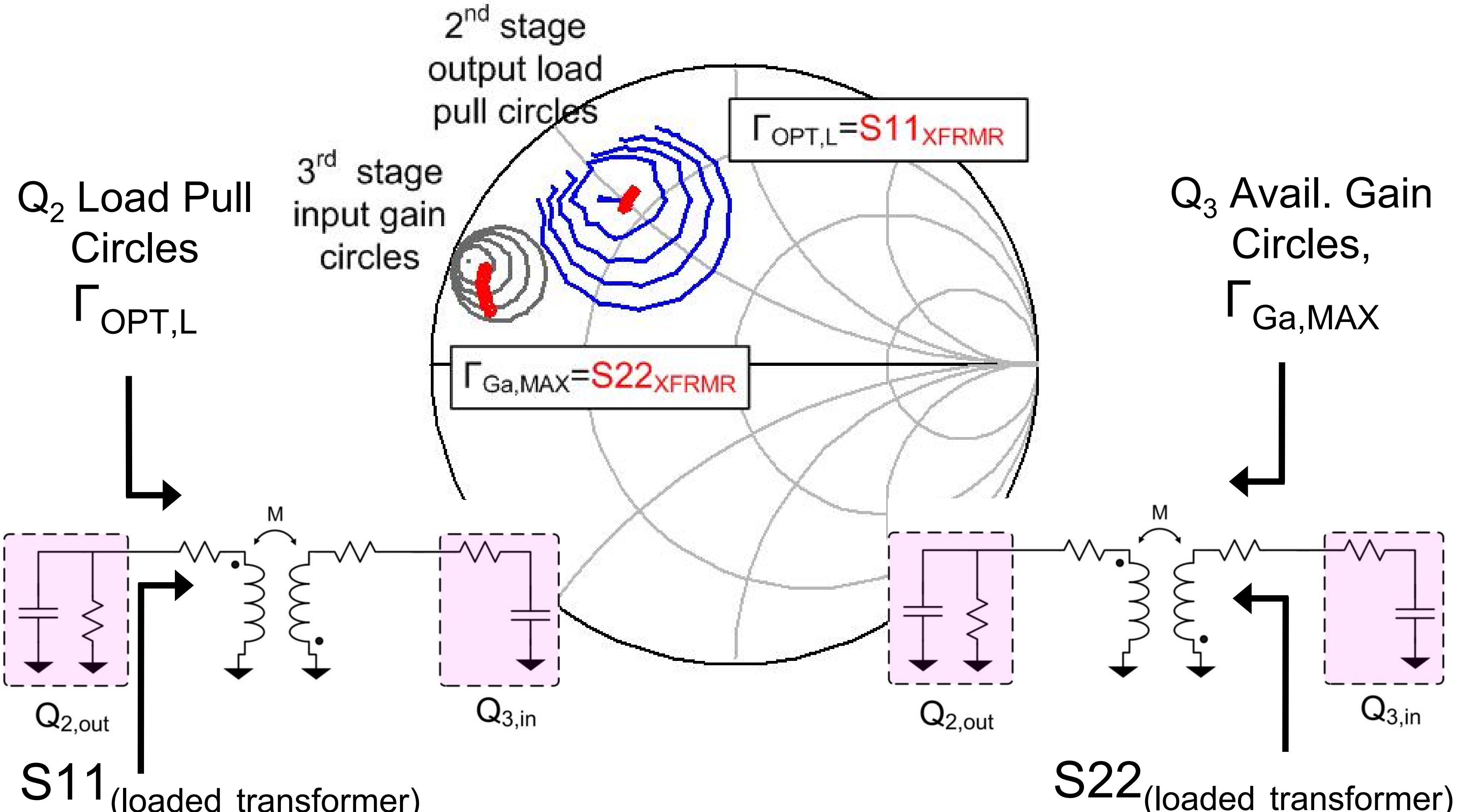
S21



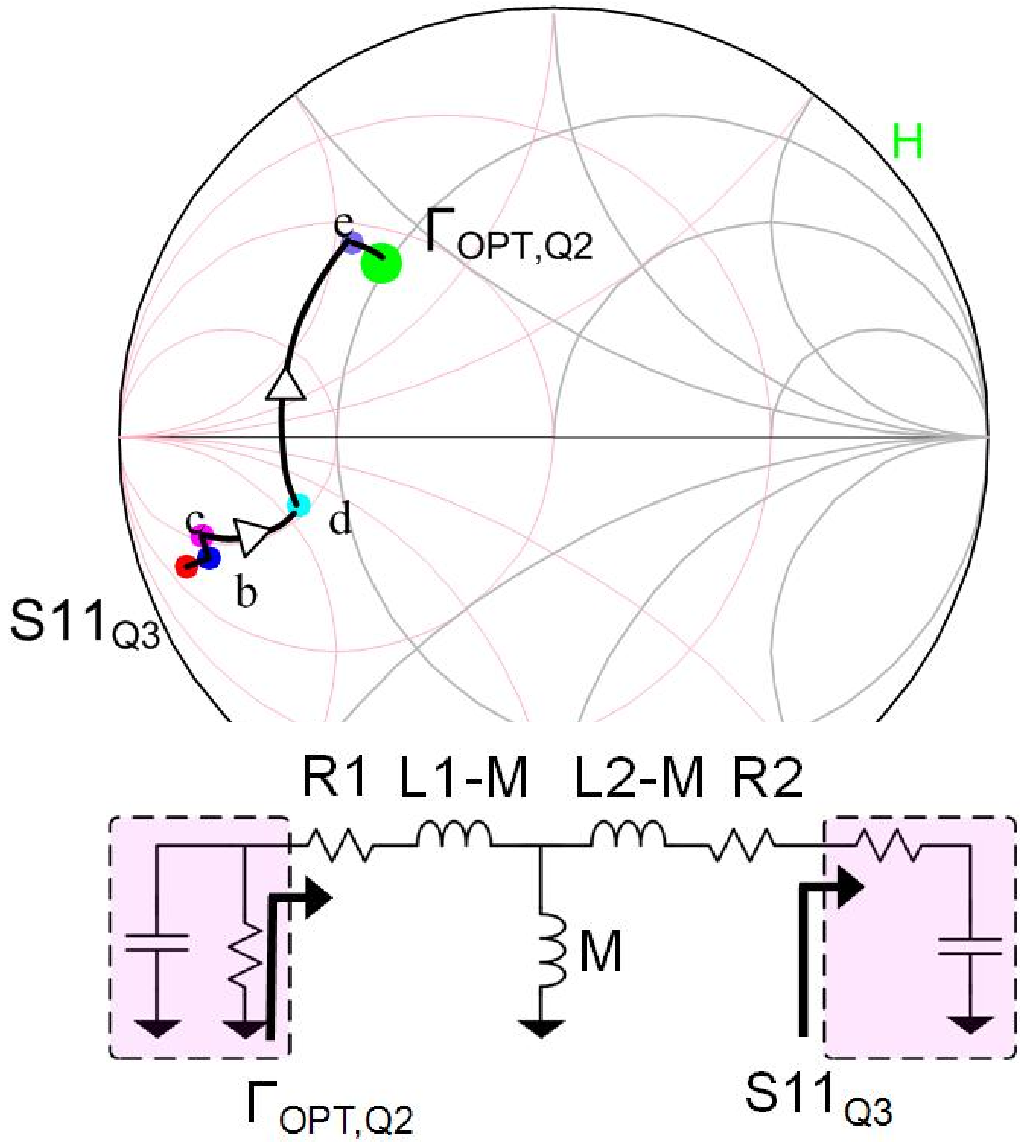


Transformer: Matching

- Simultaneous impedance matching transformation between the output of the n^{th}-1 stage to the n^{th} stage.



Transformer: Matching Path



L1=imag(Z11)/w

L2=imag(Z22)/w

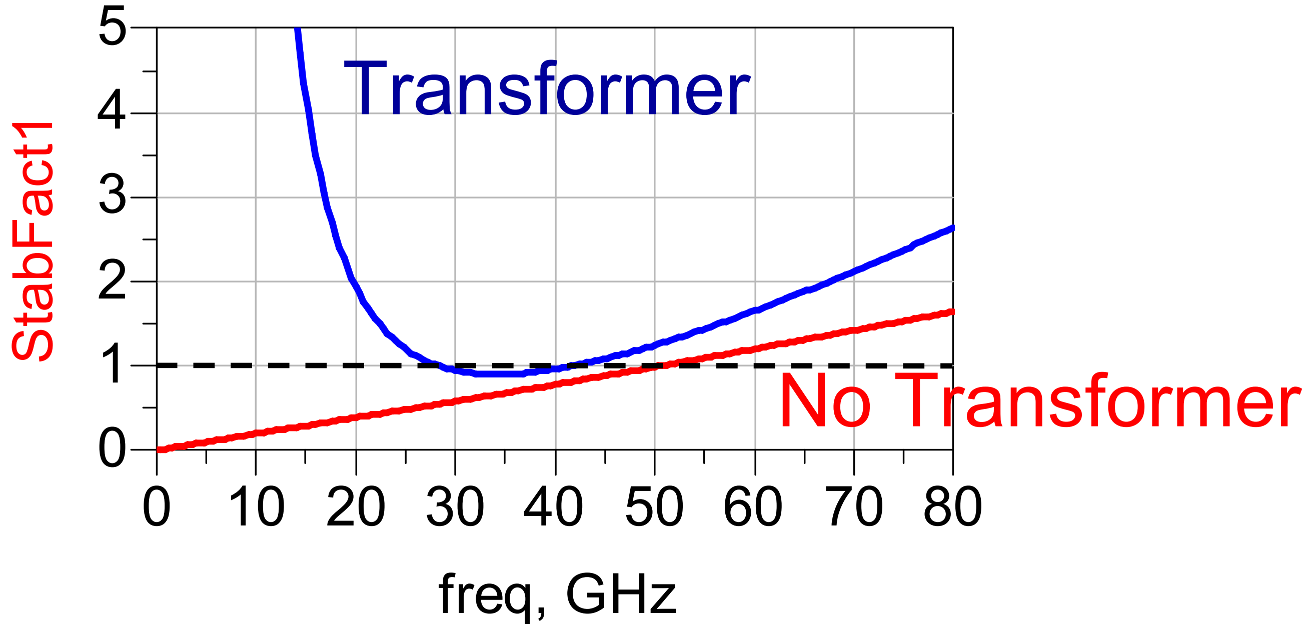
M=imag(Z12)/w

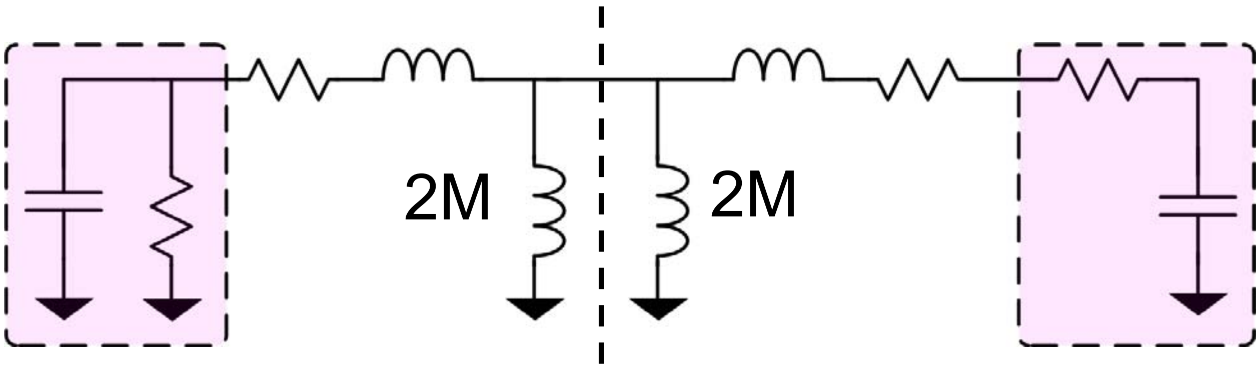
R1=imag(Z11)

R2=imag(Z22)

Transformer: Stability

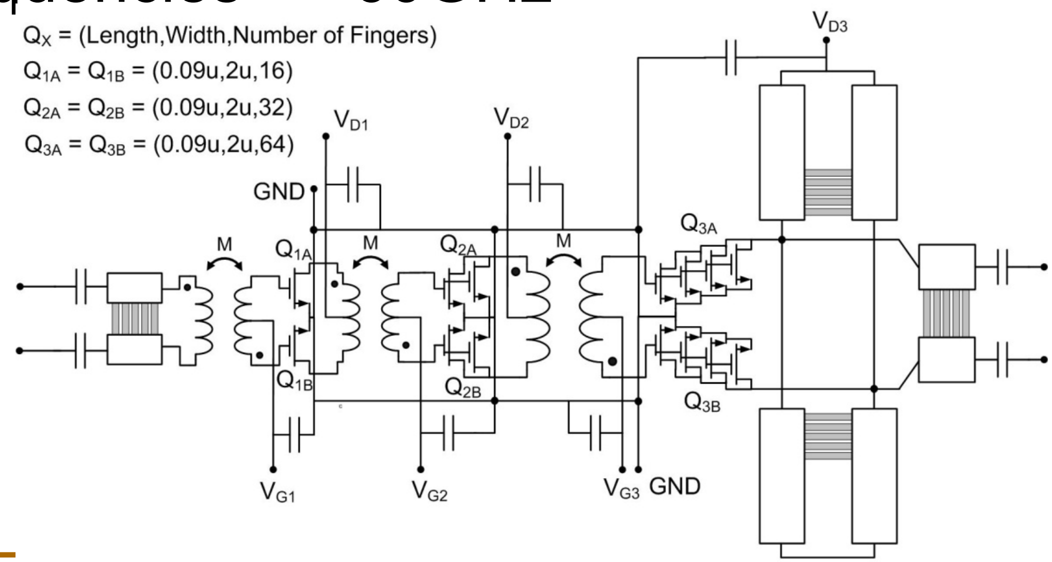
- Q and inductive high-pass network provided by the transformer stabilizes large device peripheries





Transformer Requirments

- Width determined by power handling capability (RMS current), and low loss [5um and 10um]
- Turn ratio is determined ~ device periphery ratio (2).
- Load-pull and S11 determine L_1 and L_2 (self-inductances)
- Metal thickness increased by combining M8-M9.
- Minimum spacing for max. coupling
- Self-resonance frequencies >> 60GHz
- $Q_{1,2}$ >10-12



Small-Signal Performance

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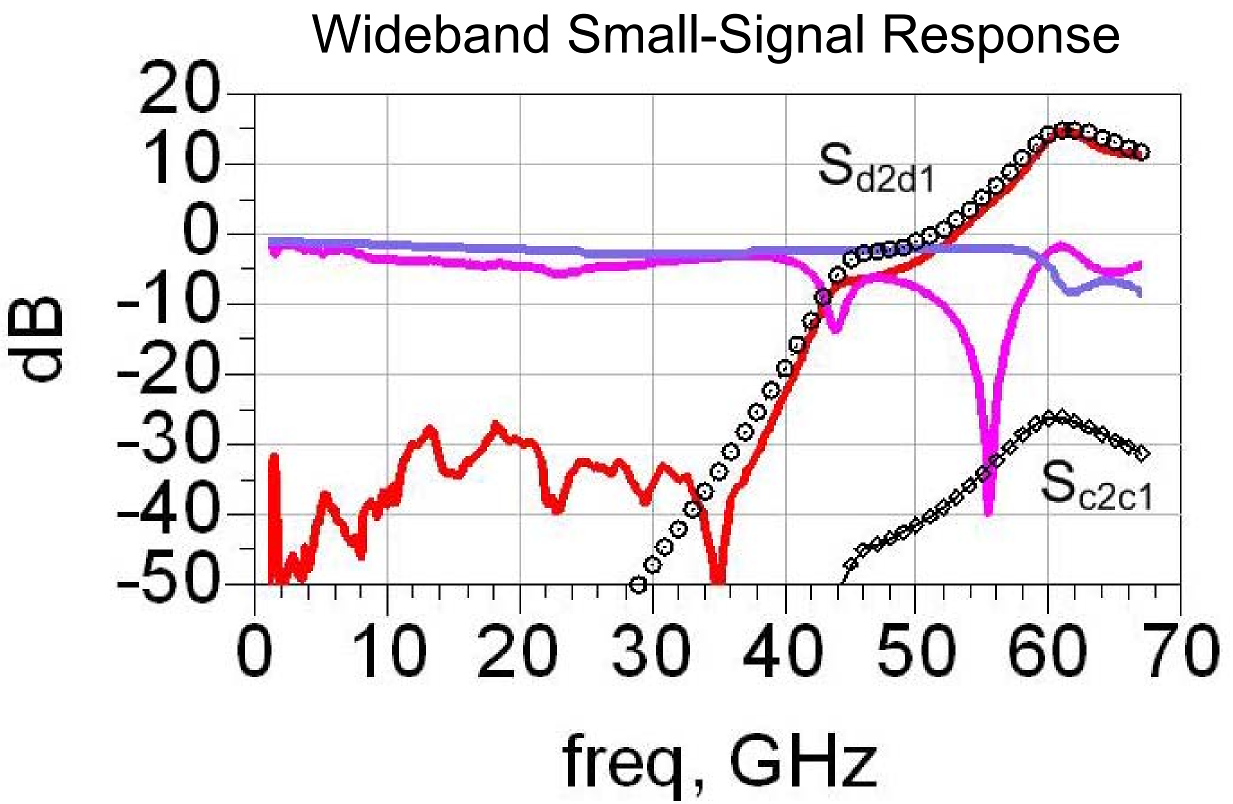
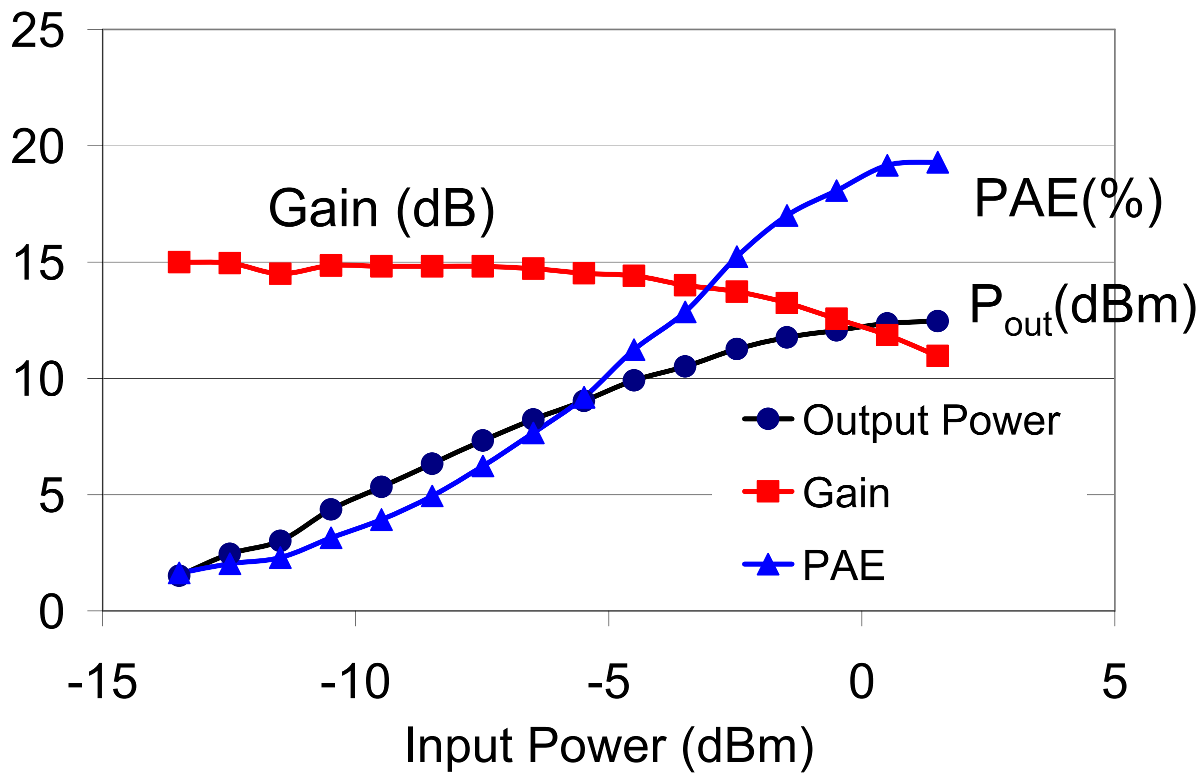
- Gain centered at 61GHz.
- Good agreement between simulation and test.
- Gain greater than 15dB



Sim = circle
Test = solid

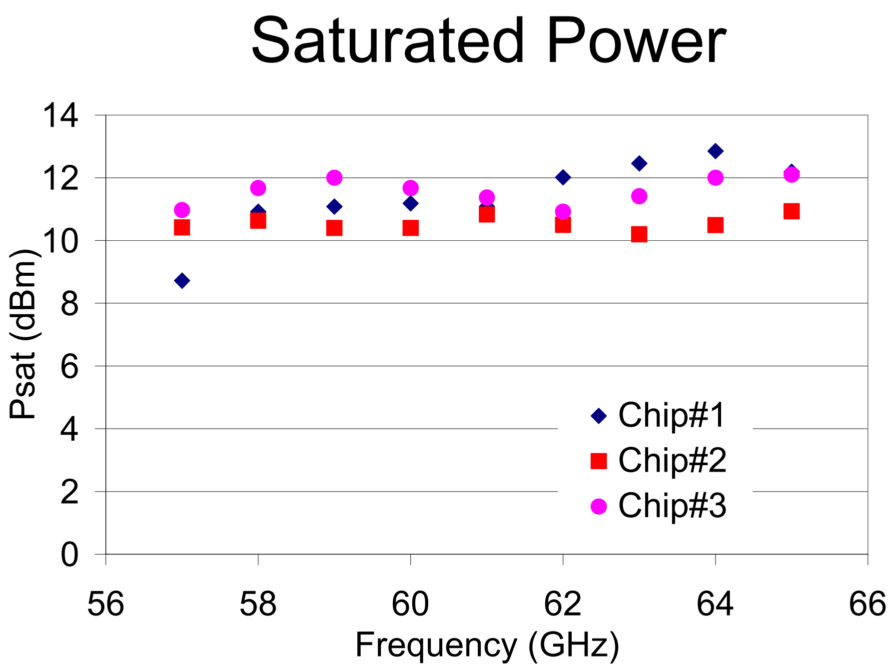
Swept Power Performance

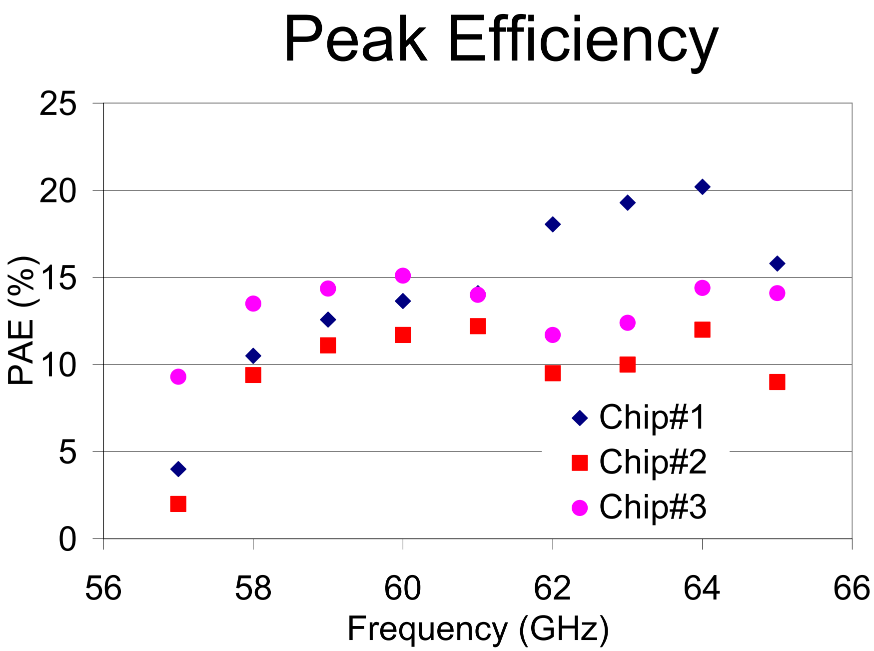
- Saturated Power above 12dBm
- Efficiency greater than 19%.



Large Signal Performance across Band

- 57-65GHz PAE and P_{sat} performance
- Three different chips





Comparison to Prior Art

- Highest reported efficiency and power to-date.

Reference	**This Work**	*[13]*	*[11]*	*[16]*	*[15]*
Technology	90nm	90nm CMOS	90nm	90nm CMOS	90nm CMOS
P_{SAT} (dBm)	**12.5**	8.4	12.3	10.6	8.4
PAE_{SAT} (%)	**19.3**	7	8.8	~1	5.8
$Gain_{SAT}$ (dB)	**11**	10.3	2.3	1	8.4
$Gain_{LIN}$ (dB)	**15**	15.2	5.5	8	17
V_D (volt)	**1.2**	0.7	1.0	1.2	na
P_{DC}(mW)	**84**	89	87	228.6	54
Area (mm^2)	**0.15**	0.18	0.26*	0.97*	0.99*

Layout

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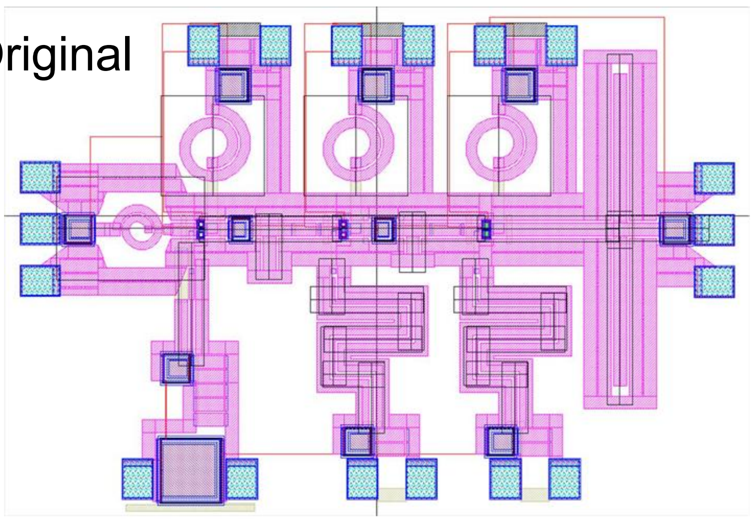
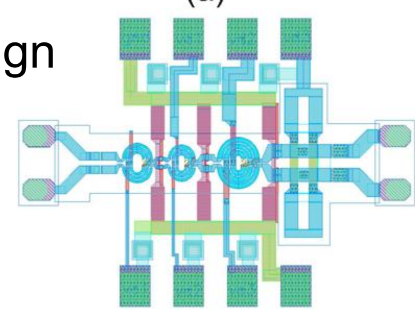
- Compact layout with core area 0.15mm^2
- 16.7% the area of original single ended version.
  - 7-8dB higher gain, and 3.5dBm higher output power

Original

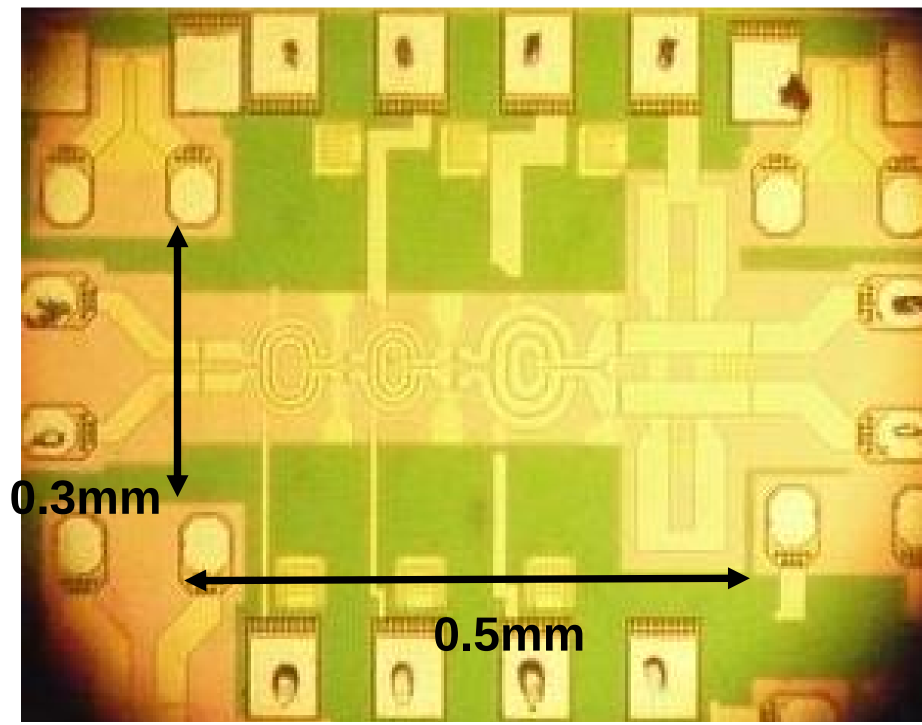


(a)

New Design

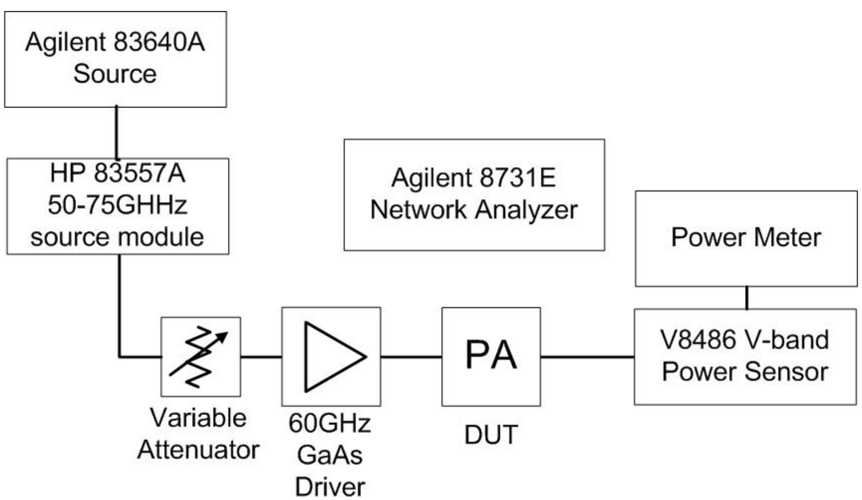


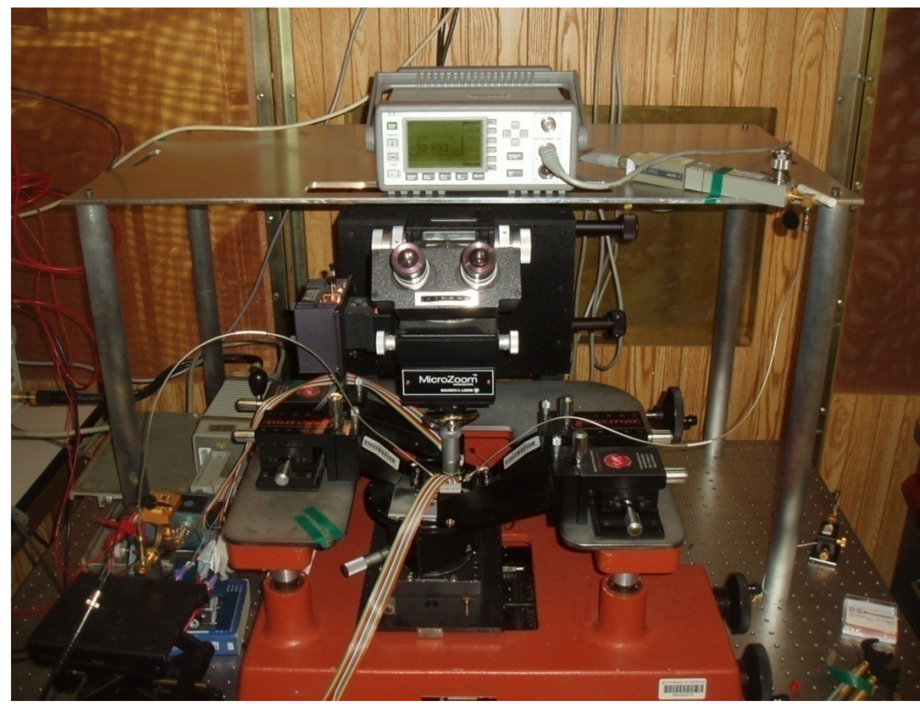
(b)



Test Set-up

- Agilent 8731E Network Analyzer, SOLT calibration
- Agilent 83640A synthesized sweeper, 83557A 50-75GHz source module, NGC GaAs MMIC amp
- Power measurements calibrated and tested to standard





Conclusion

- 60GHz differential CMOS transformer-based power amplifier design validated.
- Highest reported efficiency and saturated power to date.
- Compact size achieved
- Acknowledgements
  - UMC Foundry
  - Northrop-Grumman Corp.

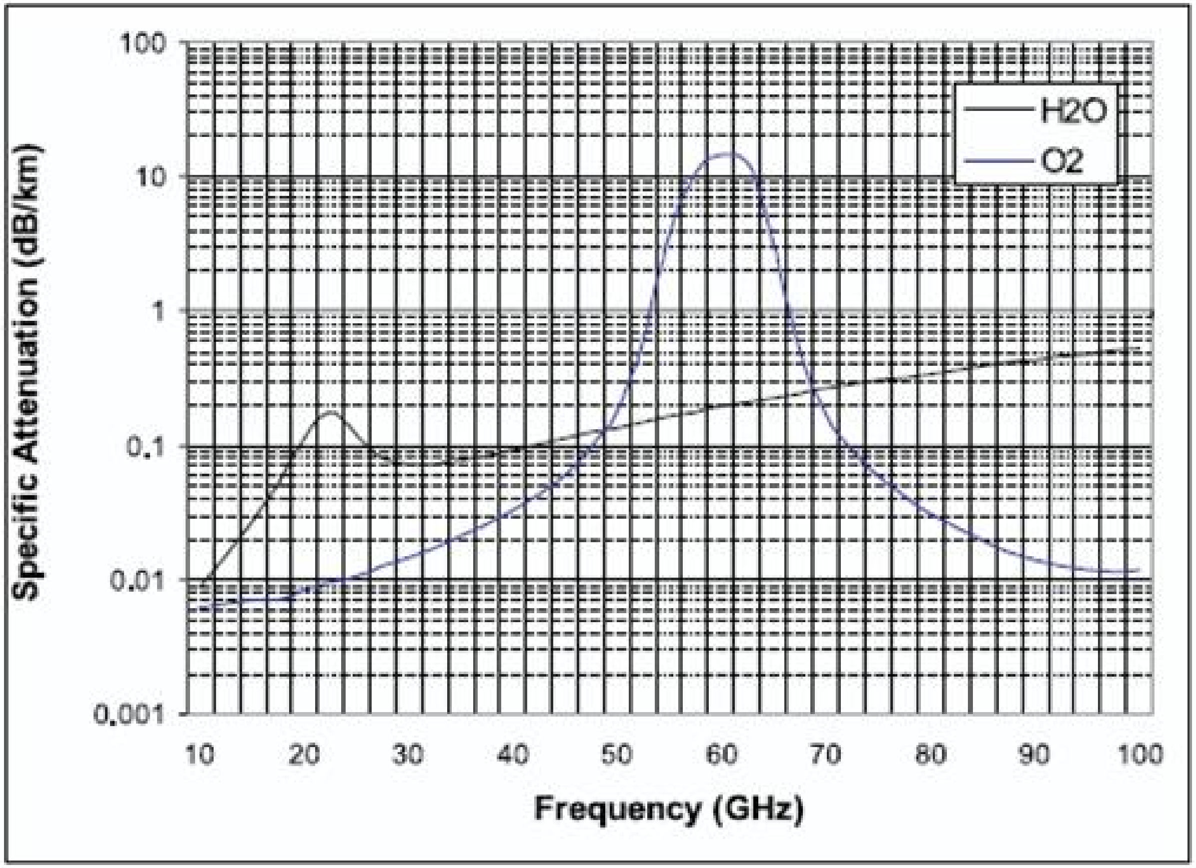
Process Variation

- TT,FF,SS corners for BSIM4 Model
  - F = Low Threshold, high leakage and driving current
- 20% Capacitive Variation

BSIM4 Model Parameter Corner Variation	tt	ss	ff	delta	%
Physical gate oxide thickness	1.82E-09	-1.00E-10	1.00E-10	2.00E-10	10.98
Width reduction parameter	2.02E-08	0	2.00E-09	2.00E-09	9.90
Length dependence of lpe0	3.89E-08	-1.55E-09	1.40E-09	2.95E-09	7.58
L offset for channel width due to mask/etch effect	-1.00E-08	-1.00E-10	1.30E-09	1.40E-09	14.02
Source-drain resistance per width	50	-1.00E+01	1.70E+01	2.70E+01	54.00
Gate-drain overlap capacitance per width	5.00E-11	5.00E-12	-5.00E-12	1.00E-11	20.00
New C-V model parameter	2.20E-10	2.20E-11	-2.20E-11	4.40E-11	20.00
Fringe capacitance parameter	9.26E-11	9.26E-12	-9.26E-12	1.85E-11	20.00
Source bottom junction capacitance	1.07E-03	-1.07E-04	1.07E-04	2.14E-04	20.00
Source sidewall junction capacitance	1.26E-10	-1.26E-11	1.26E-11	2.52E-11	20.00
Source (gate) sidewall junction capacitance	2.31E-10	-2.31E-11	2.31E-11	4.62E-11	20.00
Electrical gate oxide thickness	2.25E-09	-1.00E-10	1.00E-10	2.00E-10	8.89
Threshold voltage	2.00E-01	-3.30E-02	3.30E-02	6.60E-02	33.00
Gate-source overlap capacitance per width	5.00E-11	5.00E-12	-5.00E-12	1.00E-11	20.00
Length dependence parameter for Vth offset	-4.93E-09	-1.05E-09	4.50E-10	1.50E-09	30.51
New C-V model parameter	2.20E-10	2.20E-11	-2.20E-11	4.40E-11	20.00
Equivalent length of pocket region at 0V	1.00E-10	0.00E+00	0.00E+00	0.00E+00	0.00
W offset for channel width due to mask/etch effect	0.00E+00	1.80E-09	-5.00E-09	6.80E-09	
Narrow width effect	-1.288	-2.51E+00	2.20E+00	4.71E+00	365.68
Width reduction parameter	1.78E-22	-1.20E-23	4.00E-23	5.20E-23	29.18

Atmospheric Absorption

- O^2 resonance

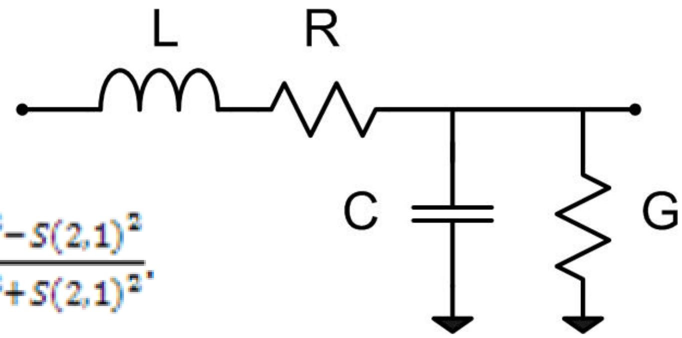


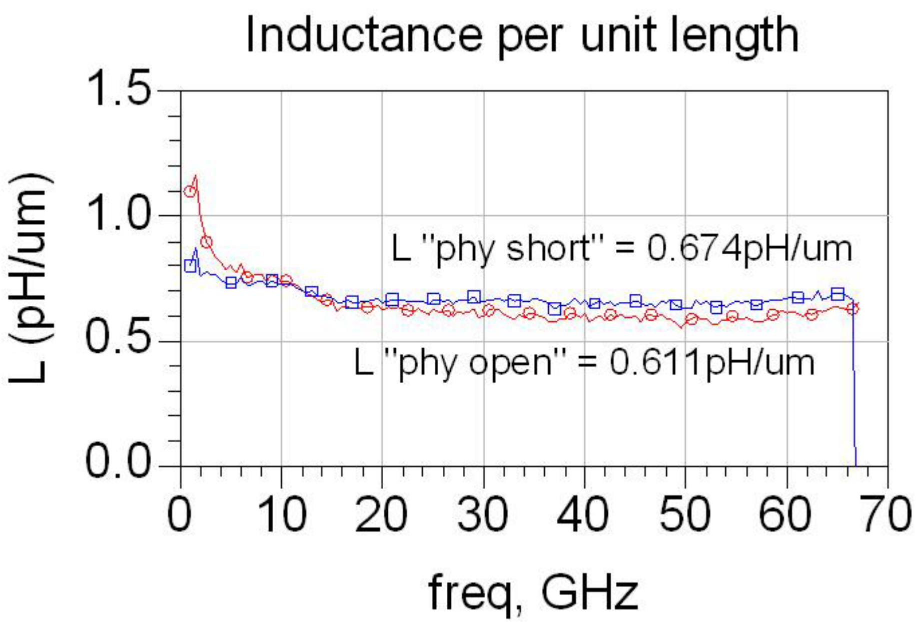
RLC Model for Artificial Dielectric

$$R = Re\{\gamma Z\} \qquad C = \frac{Im\left\{\frac{\gamma}{Z}\right\}}{\omega}$$

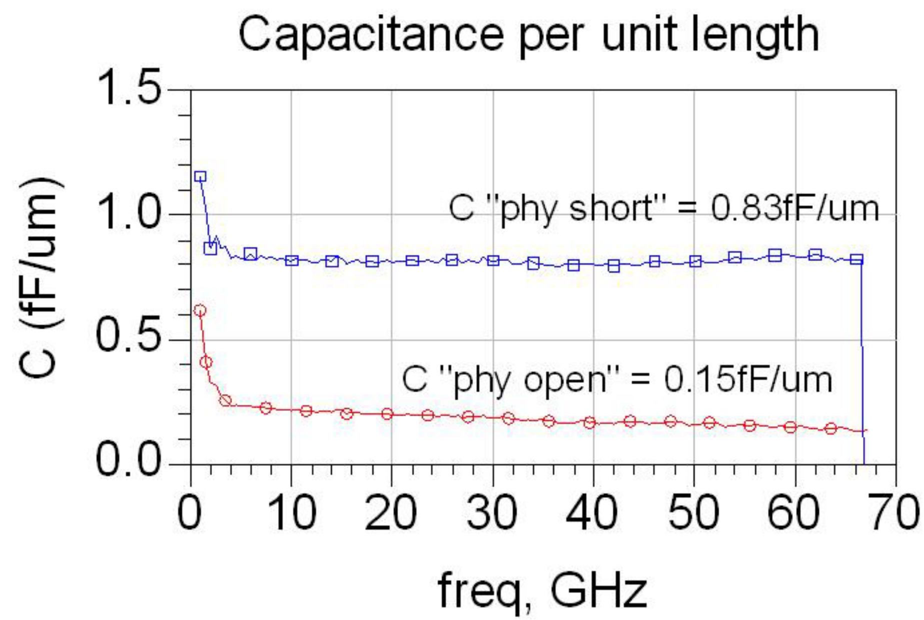
$$L = \frac{Im\{\gamma Z\}}{\omega} \qquad \gamma = \alpha + j\beta$$

$$G = Re\left\{\frac{\gamma}{Z}\right\} \qquad Z = \mp\sqrt{\frac{Z(1,1)}{Y(1,1)}} = {Z_0}^2\,\frac{(1+S(1,1))^2 - S(2,1)^2}{(1+S(1,1))^2 + S(2,1)^2}.$$





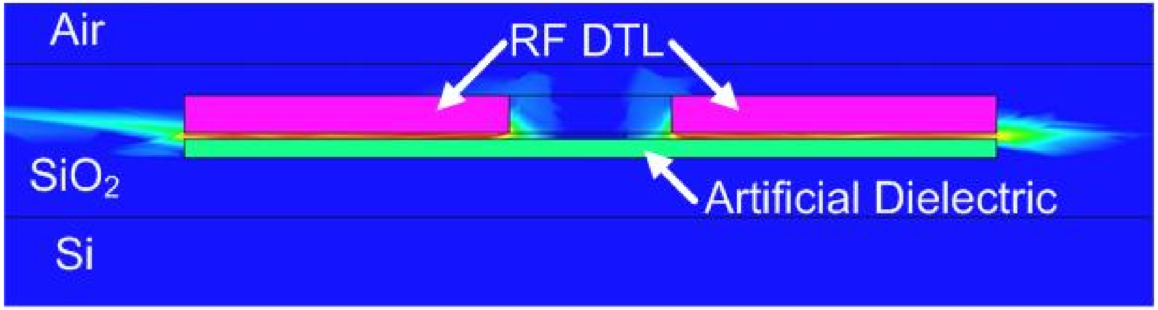
No effect on Inductance

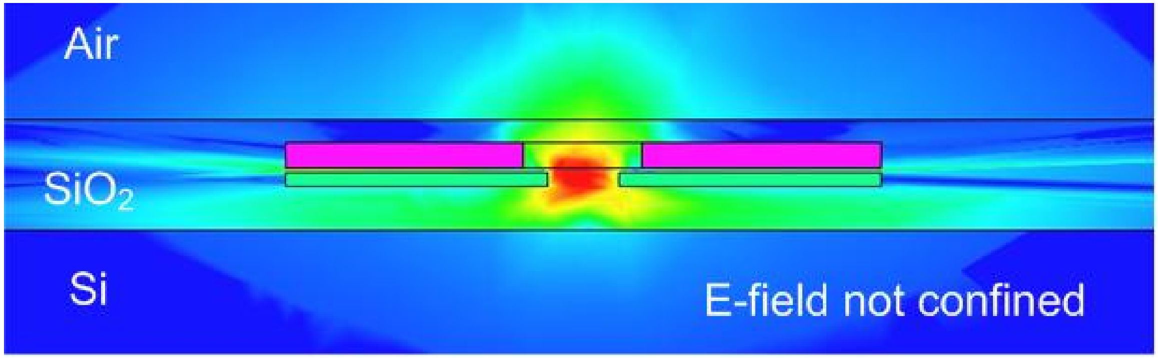


Factor 5-6 for capacitance

Electric Field

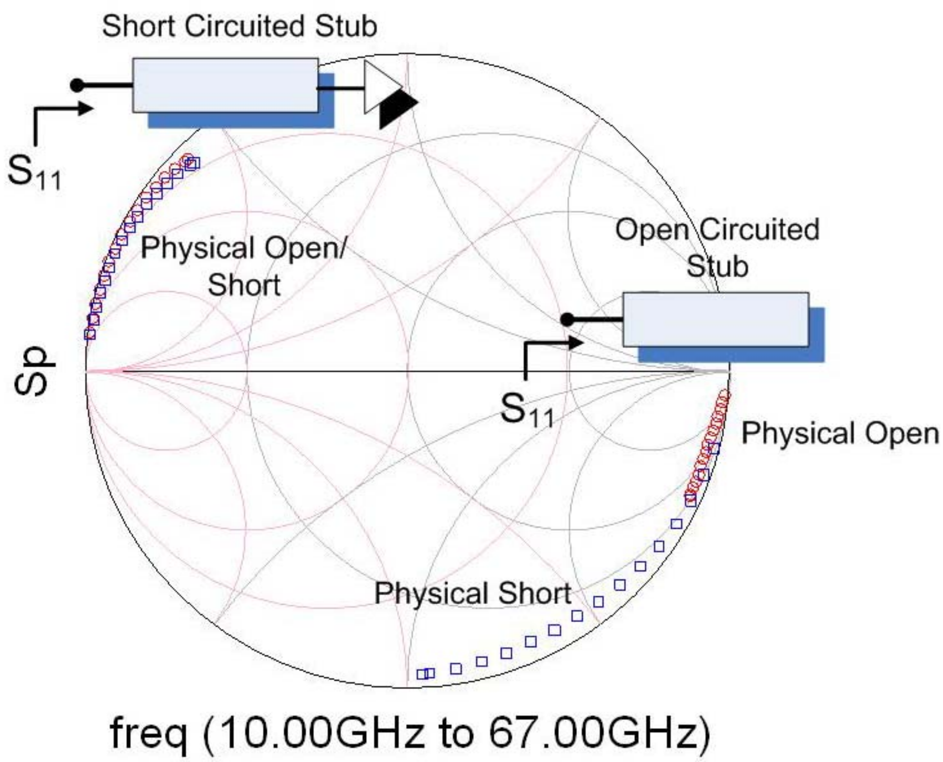
- E-field confined between artificial dielectric strips and DTL (does not shield H-field)





Short-Circuited Stub Effect

- No difference between "physical short" and "physical open" S.C. stub elements



Characteristic Impedance

$$Z_{in} = Z_0 \frac{Z_L + jZ_{0,X}\tan(\beta\ell)}{Z_{0,X} + jZ_L\tan(\beta\ell)}$$

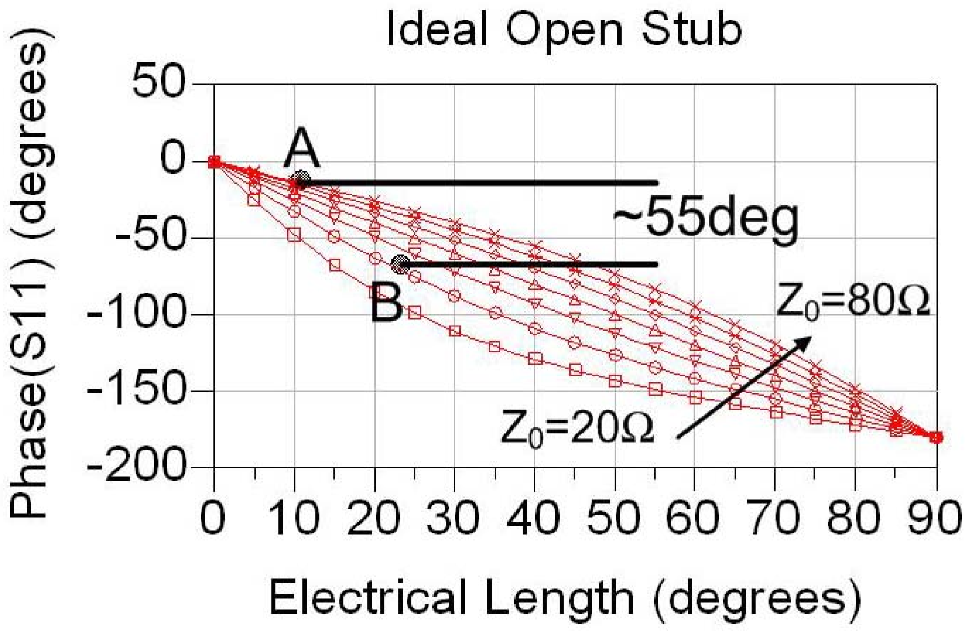
$$Z_{in\_SHORT} = jZ_{0,X}\tan(\beta\ell)$$

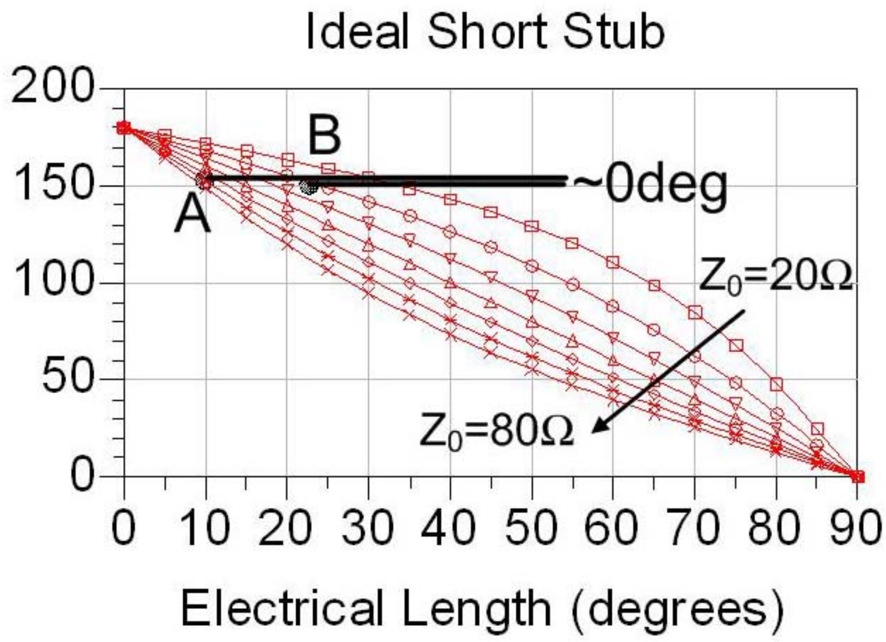
$$Z_{in\_OPEN} = -jZ_{0,X}\cot(\beta\ell)$$

$$S_{11} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0}$$

Case A. "Physical Open" Differential Line: $Z_{0,\ PhyOpen} = 65\Omega,\ \beta\ell = 10^o$

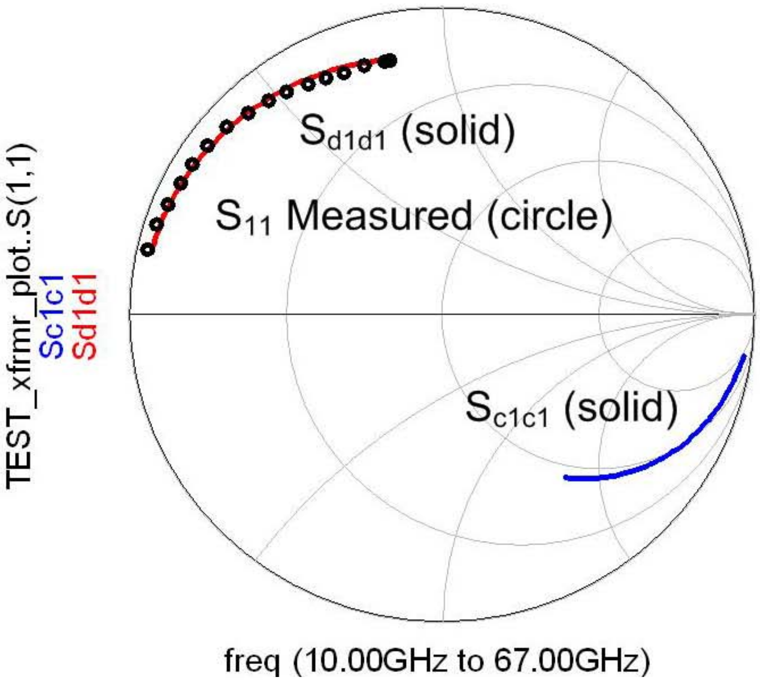
Case B. "Physical Short" Differential Line: $Z_{0,\ PhyShort} = 30\Omega,\ \beta\ell = 22.5^o$

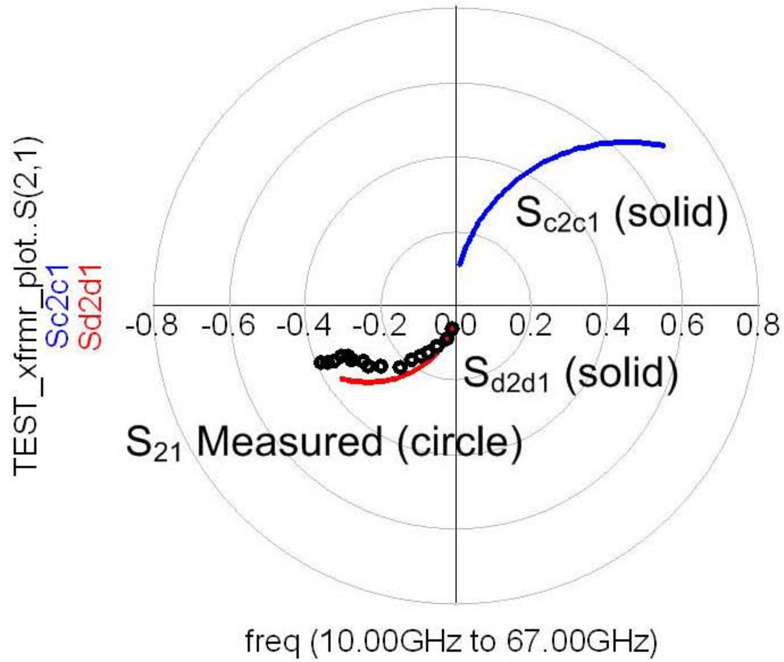


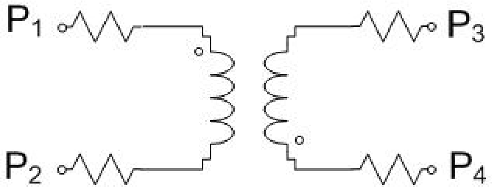


Transformer: Differential Mode

- Extract differential and common mode S-parameters from electromagnetic simulation
- Measurements match Differential Mode Simulation







Effective Dielectric Constant

- Short/Open Stub

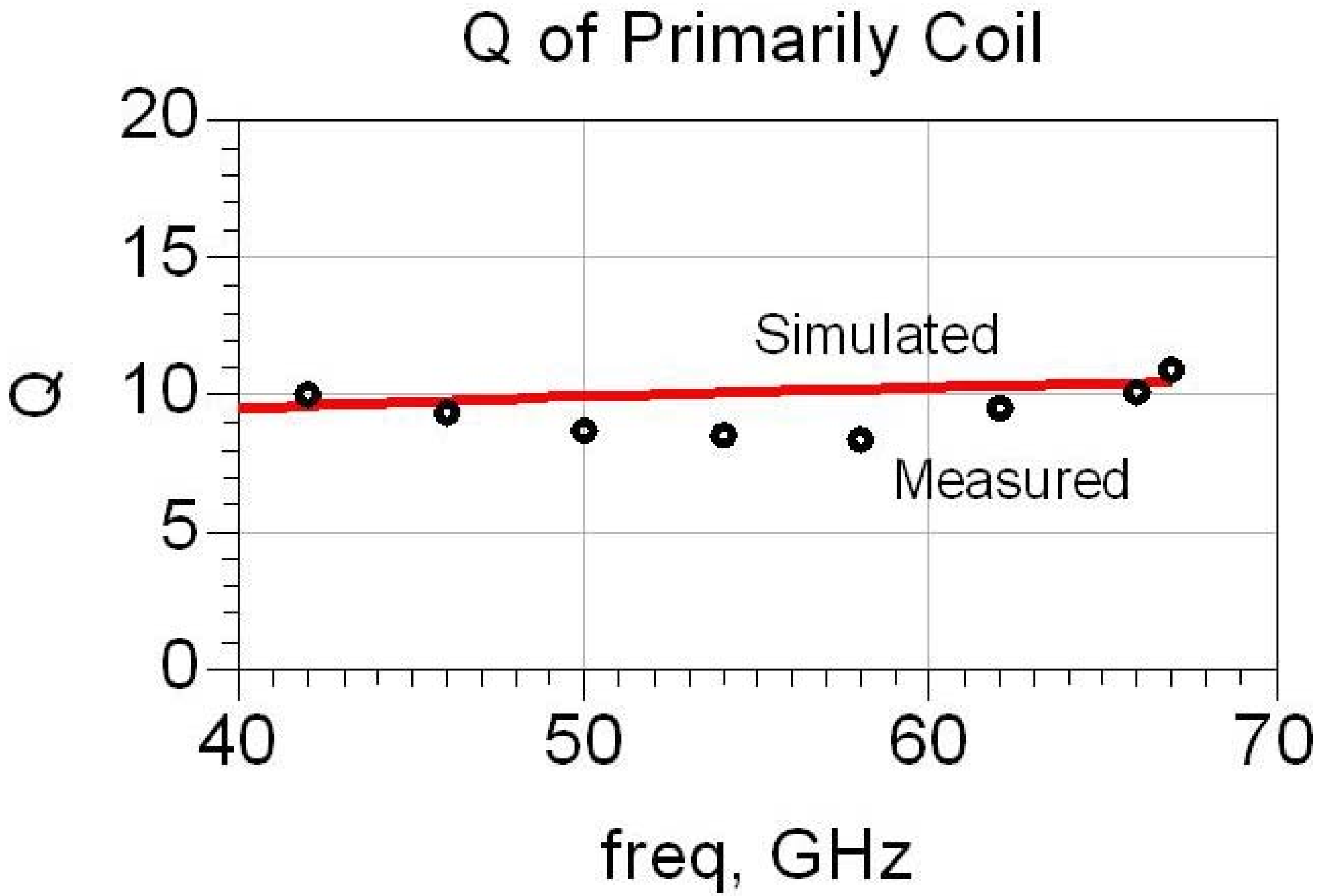
$$\beta_{open} = \frac{1}{\ell} imag\left(\coth^{-1}\left(\frac{Z_{in}}{Z_o} \right) \right)$$

$$\beta_{short} = \frac{1}{\ell} imag\left(\tanh^{-1}\left(\frac{Z_{in}}{Z_o} \right) \right)$$

$$\varepsilon_{eff} = \left(\frac{\beta_{op/sh} c}{\omega} \right)^2$$

Q Transformer

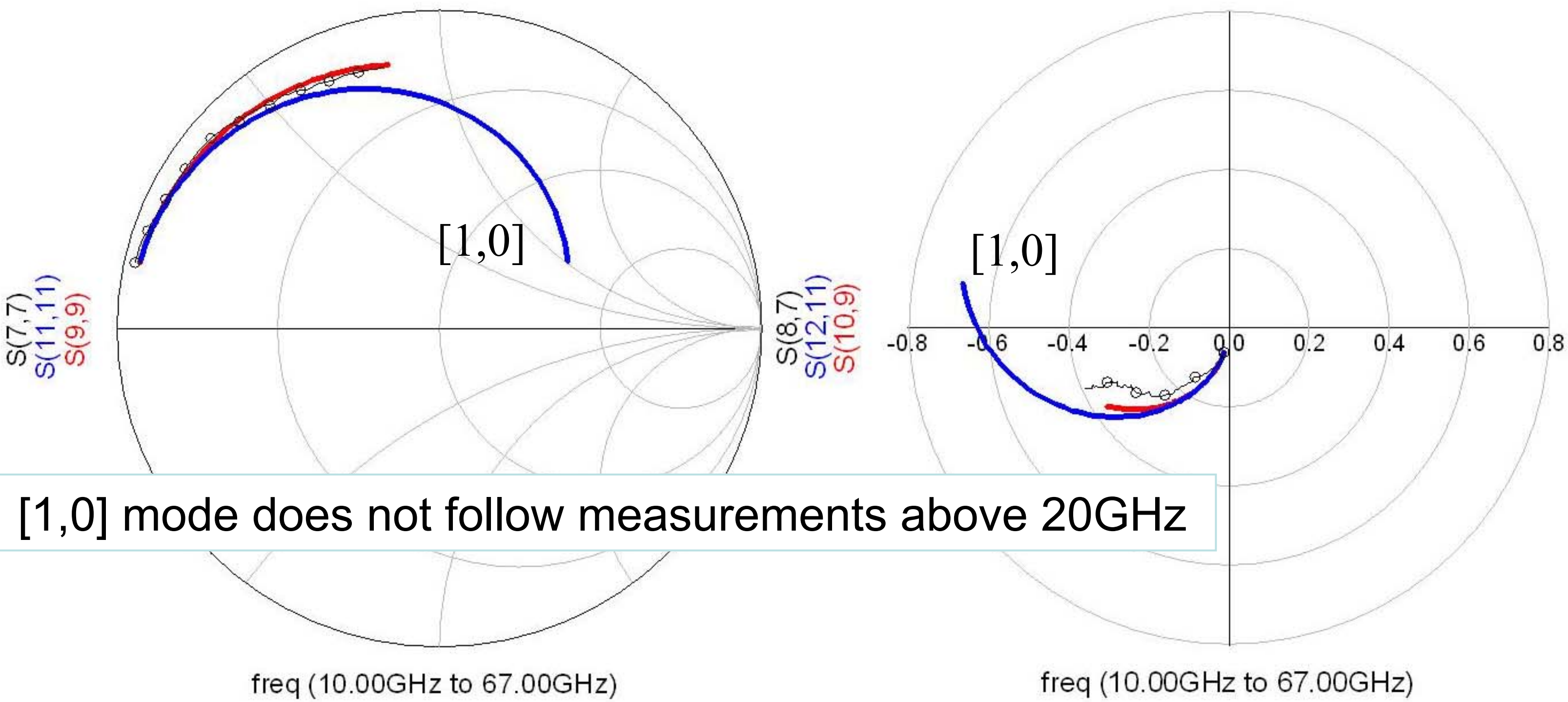
- Q is approximately 10



Transformer: Differential Mode

- [1,0] mode, or ±1V and 0V consists of both even and odd mode.

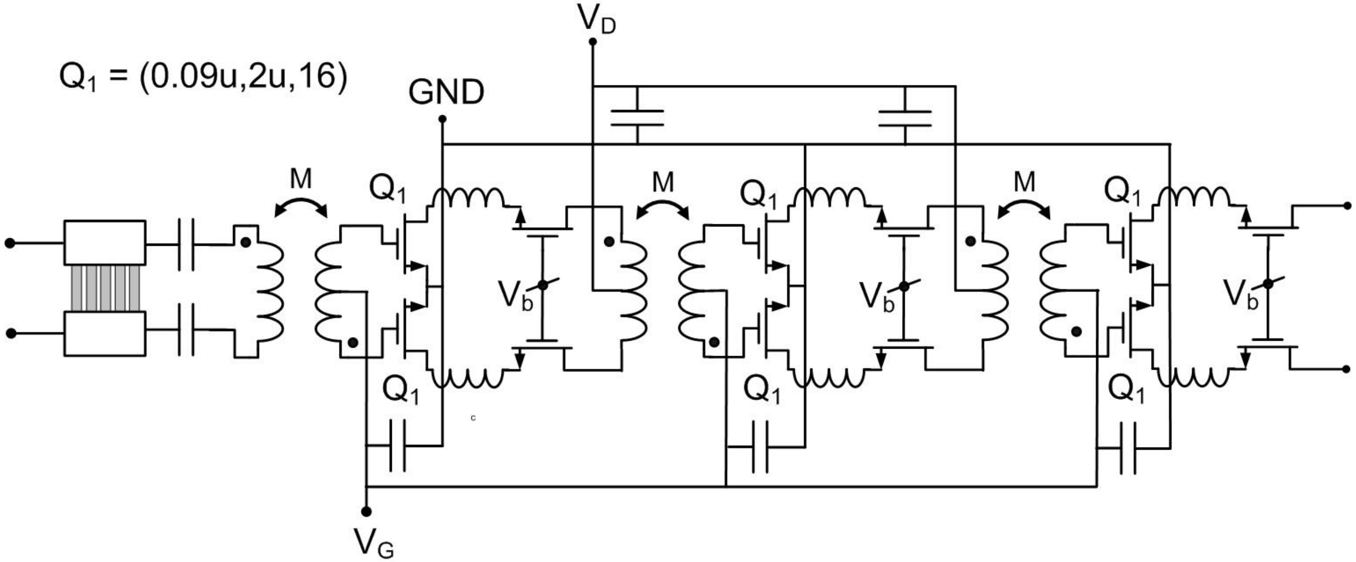
	+½	-½	:Odd Mode
+	+½	+½	:Even Mode
	1	0	

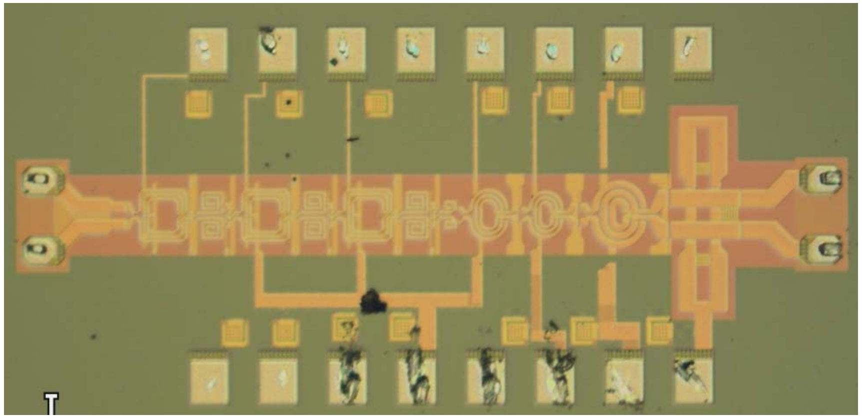


[1,0] mode does not follow measurements above 20GHz

VGA Schematic

- Cascode, Transformer-Coupled
- Layout is VGA + PA (0.95mm x 0.3mm)

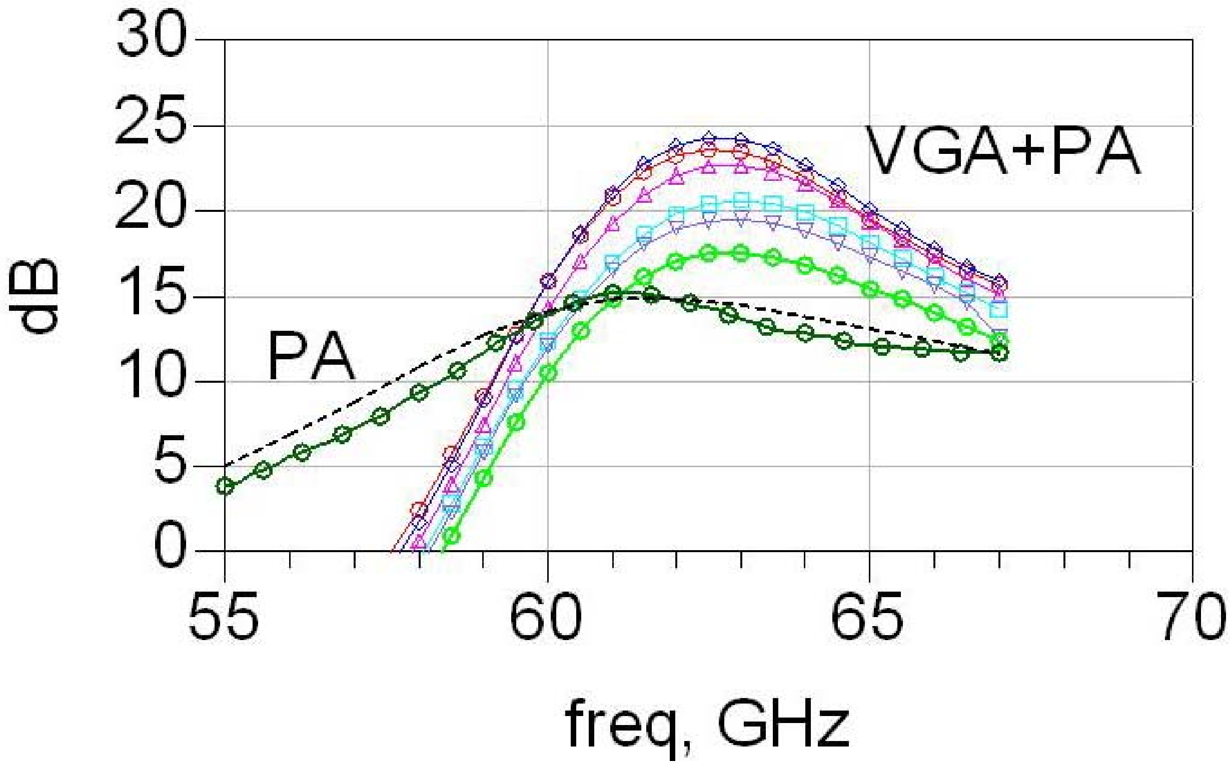




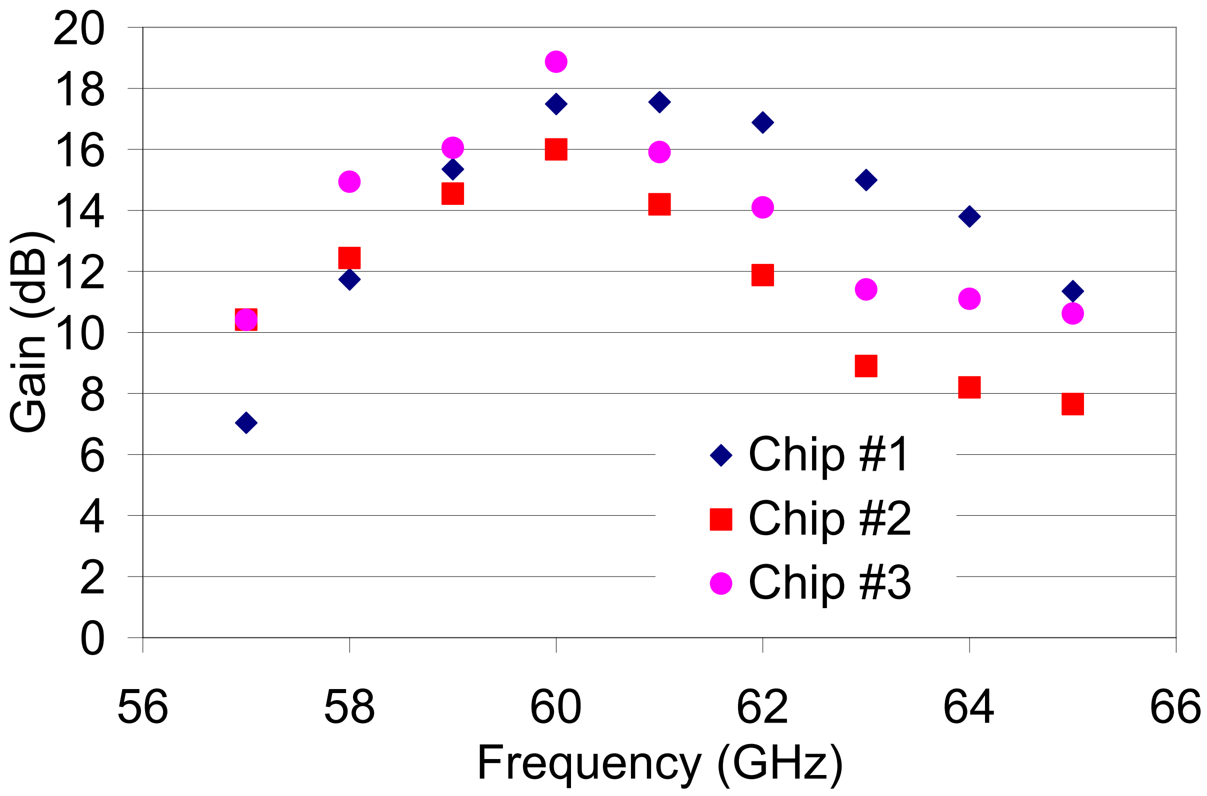
VGA Test Results

UCLA

- 24dB Peak Gain
- 8dB Variation; 7-22mA

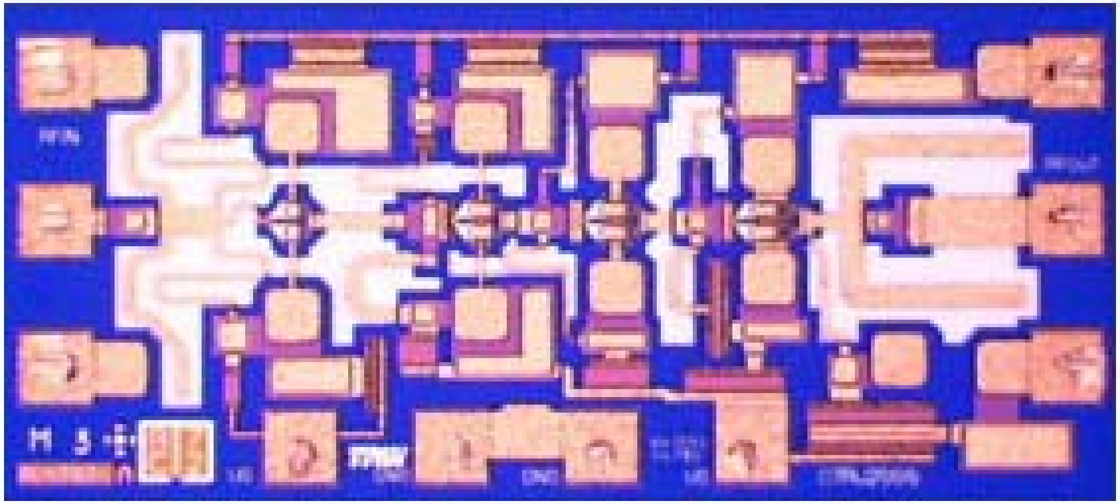


PA Gain



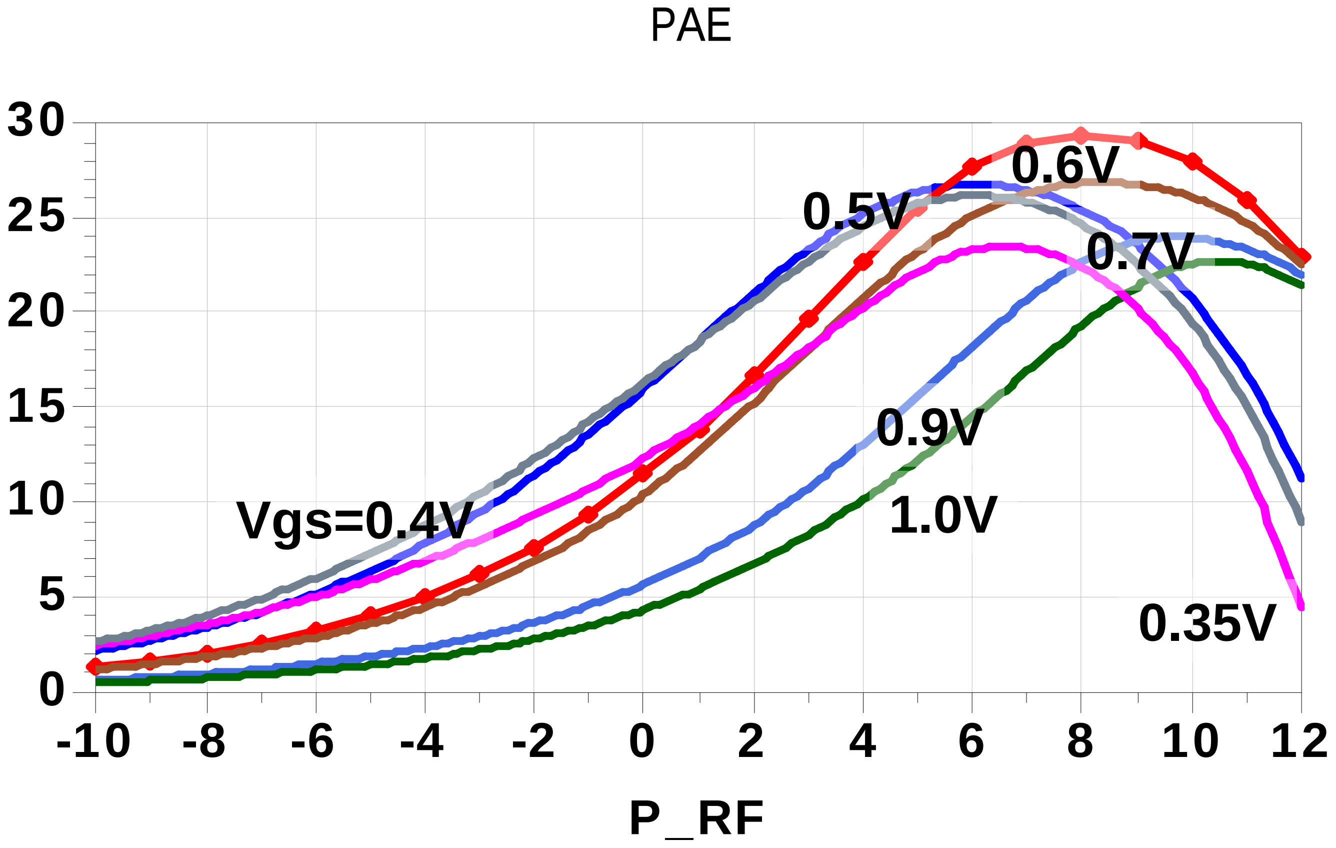
Gain (dB)
0
2
4
6
8
10
12
14
16
18
20
56
58
60
62
64
66
Frequency (GHz)
Chip #1
Chip #2
Chip #3

GaAs MMIC (ALH382)

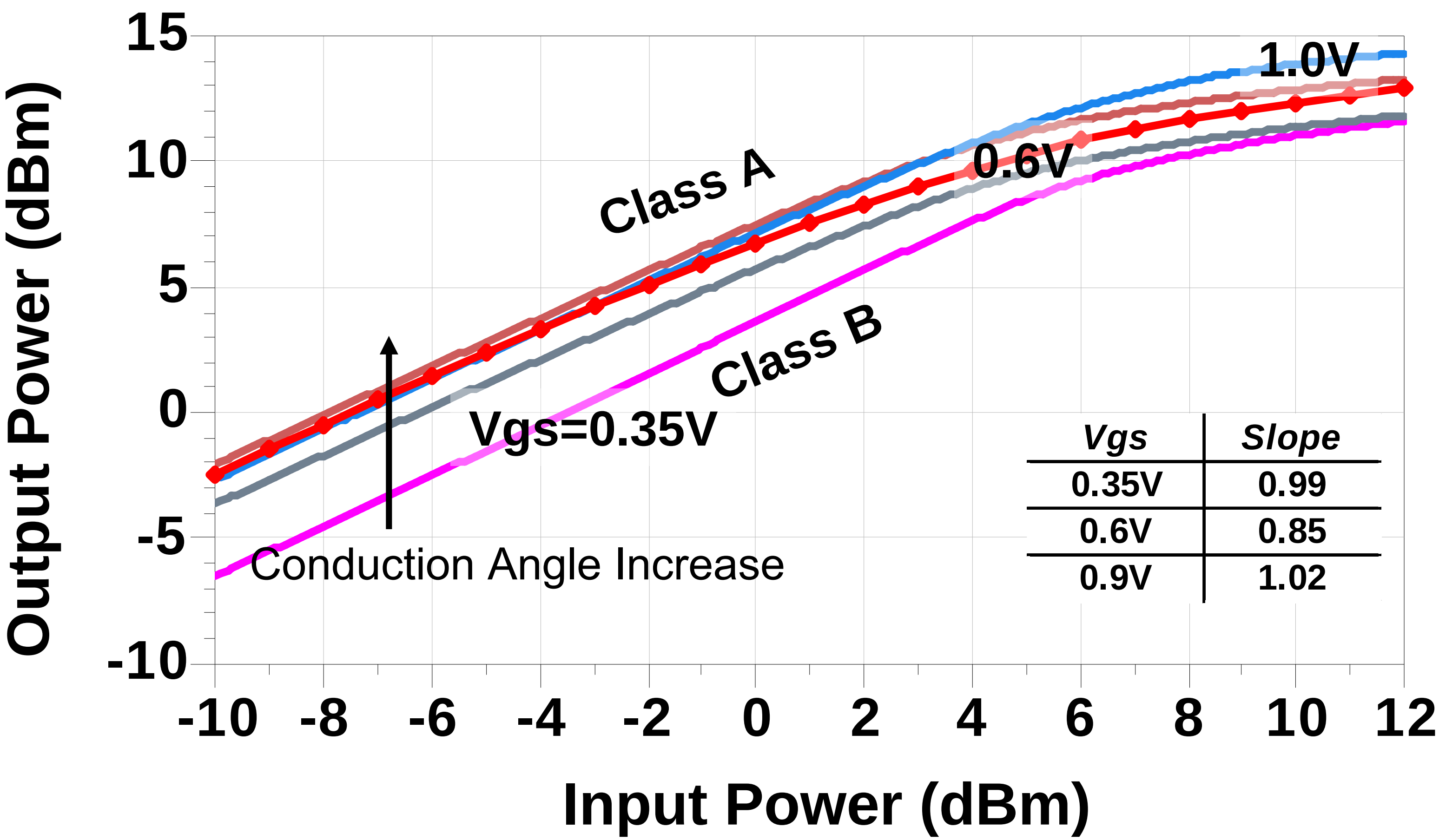


X=1550 µm Y=730 µm

PA


PAE
30
25
20
15
10
5
0
-10
-8
-6
-4
-2
0
2
4
6
8
10
12
P_RF
Vgs=0.4V
0.5V
0.6V
0.7V
0.9V
1.0V
0.35V

PA Output Power



Vgs	Slope
0.35V	0.99
0.6V	0.85
0.9V	1.02

PA Test Set-up