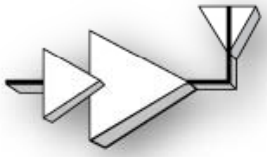

Evaluation of High Efficiency PAs for use in Supply- and Load-Modulation Transmitters

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Outline

- Motivation
  - PA efficiency for modulated signals
  - Efficiency enhancement techniques
- Supply modulation transmitters
  - General polar architectures
  - Static polar characterization of LDMOS class D^{-1} PA
  - Optimum operation for maximized efficiency
- Load modulation transmitters
  - Load impedance tuning
  - Static load modulation characterization of LDMOS class D^{-1} PA
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- Summary and conclusions
  - Summary of efficiency predictions with modulated signal statistics
  - Comparison between supply- and load modulation results
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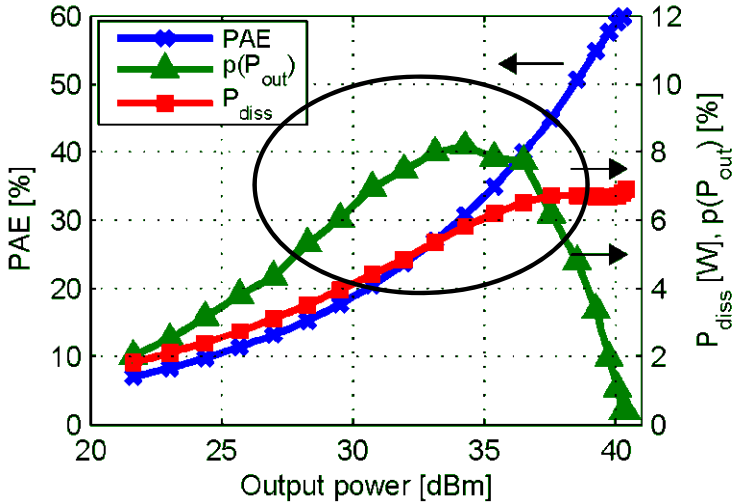
PA efficiency for modulated signals

- Typical high efficiency power amplifier characteristics



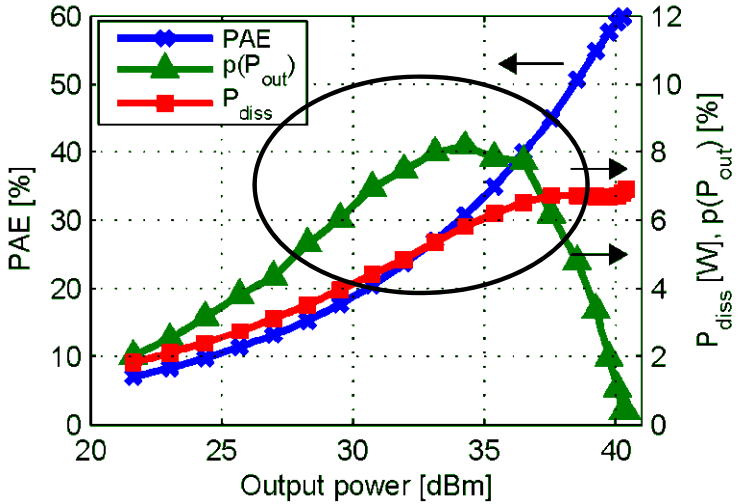
- Overall efficiency is maximized by minimizing the dissipated power, P_{diss}

$$P_{diss} = \left(P_{out} - P_{in}\right)\left(1/PAE - 1\right)$$

- Average PAE is determined by the probability: $p(P_{out}) \times P_{diss}$
  - To improve efficiency, PAE must be increased at intermediate P_{out}, where the signal spends most of its time

PA efficiency for modulated signals

- Typical high efficiency power amplifier characteristics



- Different efficiency enhancement techniques have been proposed
  - **Dynamic supply modulation (EER / envelope tracking / hybrid EER)**
  - **Dynamic load modulation**
  - Outphasing (Chireix / LINC)
  - Doherty
  - Pulse-width modulation (RF-PWM, bandpass $\Delta\Sigma$)
  - …

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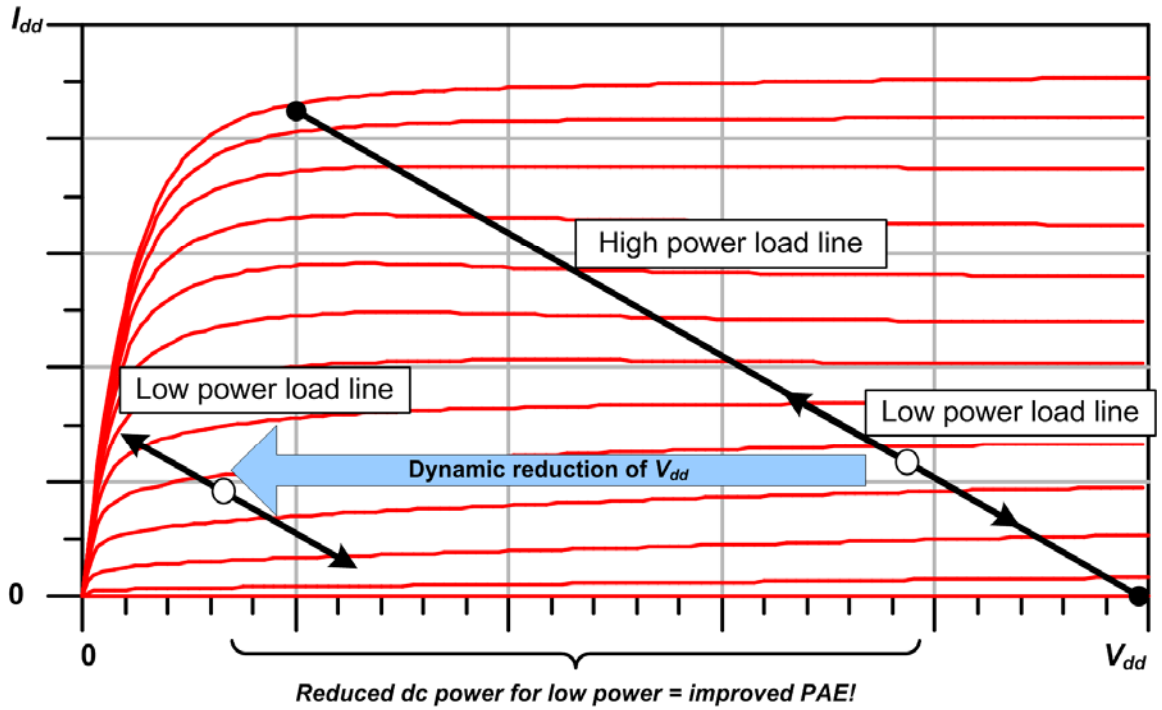
Dynamic supply modulation principle

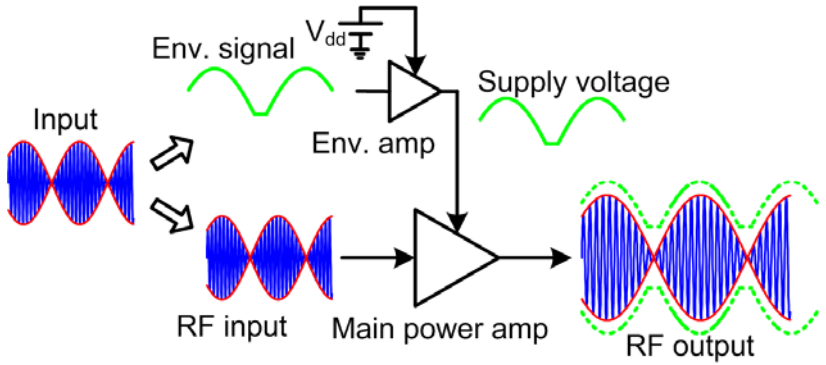
- PA efficiency can be improved if the supply voltage is decreased for lower power levels



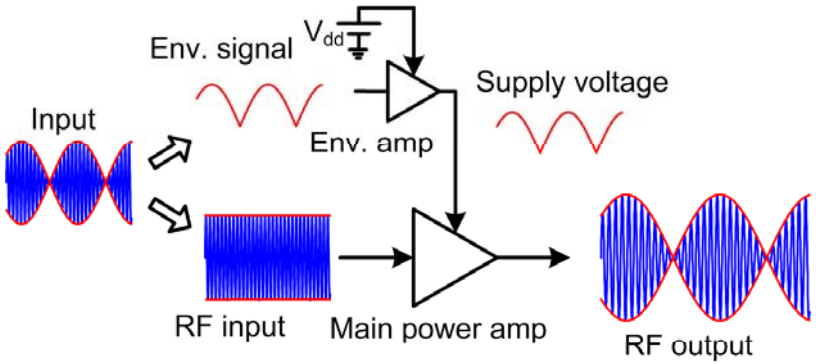
- Different techniques can be defined depending on how the RF input power and V_{dd} are jointly controlled…

Two general categories of dynamic supply modulation

- Envelope tracking (ET)
  - PA supply voltage is always sufficiently high
  - Output power is controlled by input signal, i.e. PA in linear mode
  - Pre-distortion of the RF input only, like in ordinary PA

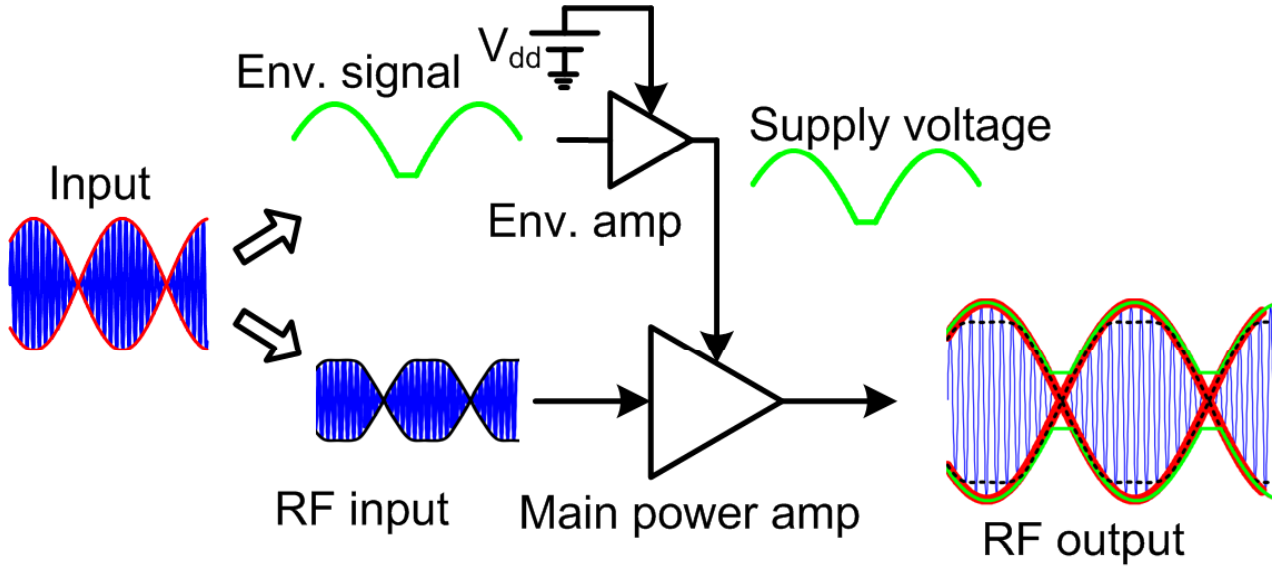


- Envelope elimination and restoration (EER)
  - Output power is controlled only by the PA supply voltage
  - PA operated in saturation
  - Suitable for switched mode PA operation
  - Time alignment between supply voltage and RF signal critical



General polar transmitter architecture

- Neither EER or envelope tracking can give maximum efficiency at all power levels
  - EER: Lower efficiency at low output power
  - ET: Lower efficiency at high output power
- Hybrid EER is considered
  - PAE can be maximized for all power levels by simultaneous control of both RF input power and supply voltage

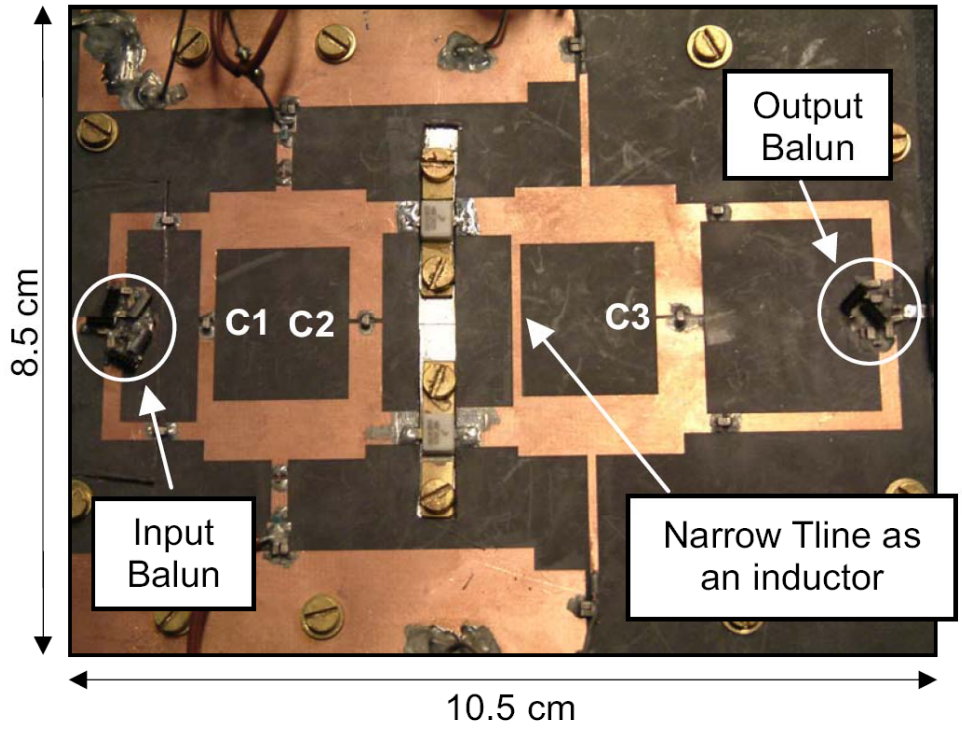


Measurement example: LDMOS class D^{-1} PA

- Static PA characterization of efficiency and P_{out} vs. P_{in} and V_{dd}

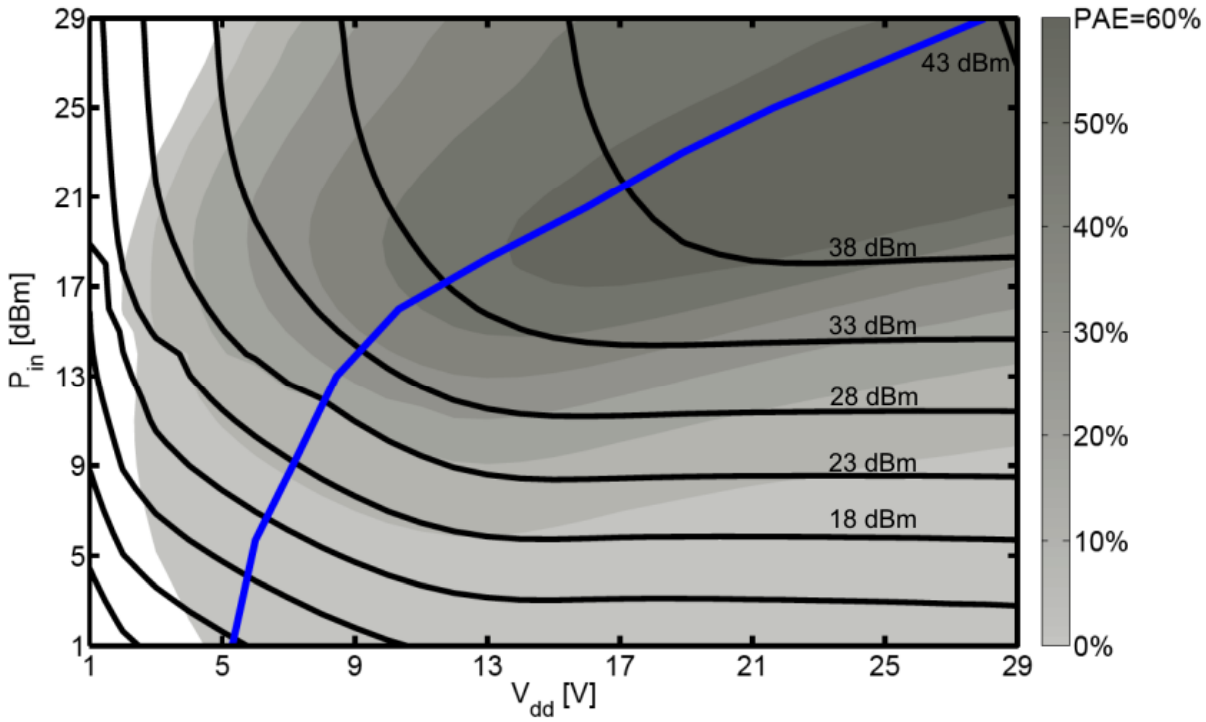
$$PAE_{PA}\left(P_{in},V_{dd}\right)=\frac{P_{out}\left(P_{in},V_{dd}\right)-P_{in}}{P_{dc}\left(P_{in},V_{dd}\right)}$$

- 1 GHz LDMOS class D^{-1} SMPA
  - Devices: 2×Freescale MRF282
- Performance summary
  - V_{DD} = 30 V
  - P_{out} = 20W
  - PAE_{MAX} = 70%
  - Gain = 15 dB
  - Bandwidth (*PAE* >50%): 90 MHz



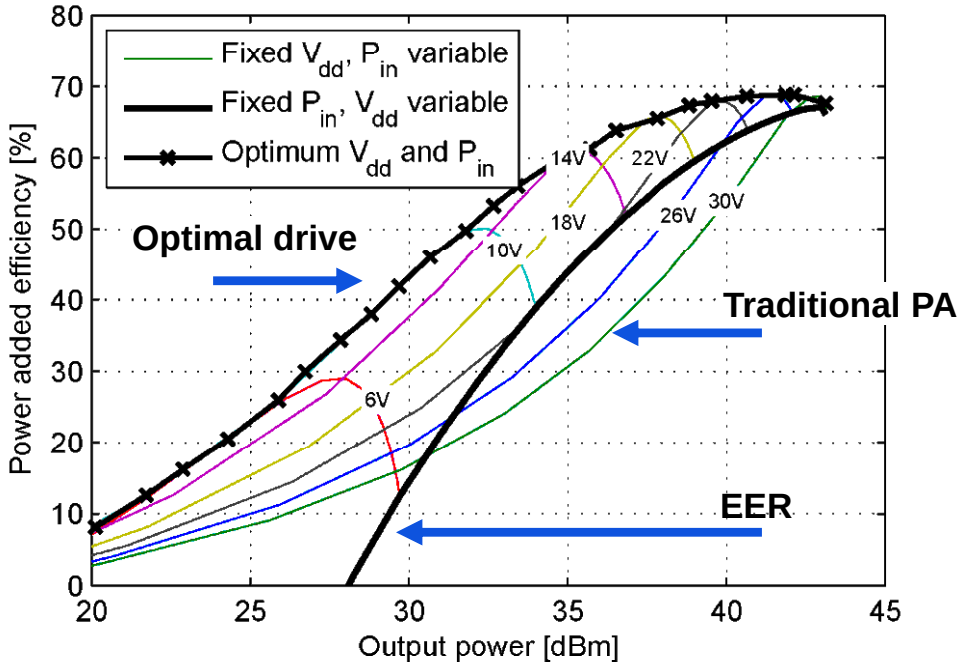
Static polar characterization results

Numbered contours represent output power levels in dBm



- Efficiency and output power have mutual dependence on input power and supply voltage
  - The V_{dd} and P_{in} combination that maximizes efficiency can be determined for every given P_{out}

Optimized polar performance for LDMOS class D^{-1} PA



P_{in} and V_{dd} are independent parameters in the figure

Simulated results with W-CDMA input signal statistics

Drive condition	$\langle\eta_{PA}\rangle$ (%)	
	PAPR 10.3 dB	PAPR 6.6 dB
Traditional (V_{dd} fixed)	24%	36%
EER (P_{in} fixed)	37%	48%
Optimum P_{in}/V_{dd} drive	53%	60%

$$\langle \eta_{PA} \rangle = \frac{\int P_{out} \cdot p(P_{out}) dP_{out}}{\int P_{in} \cdot p(P_{out}) dP_{out} + \int P_{dc} \cdot p(P_{out}) dP_{out}}$$

- Simultaneous P_{in} and V_{dd} control can give a substantial efficiency improvement for the presented LDMOS class D^{-1} PA

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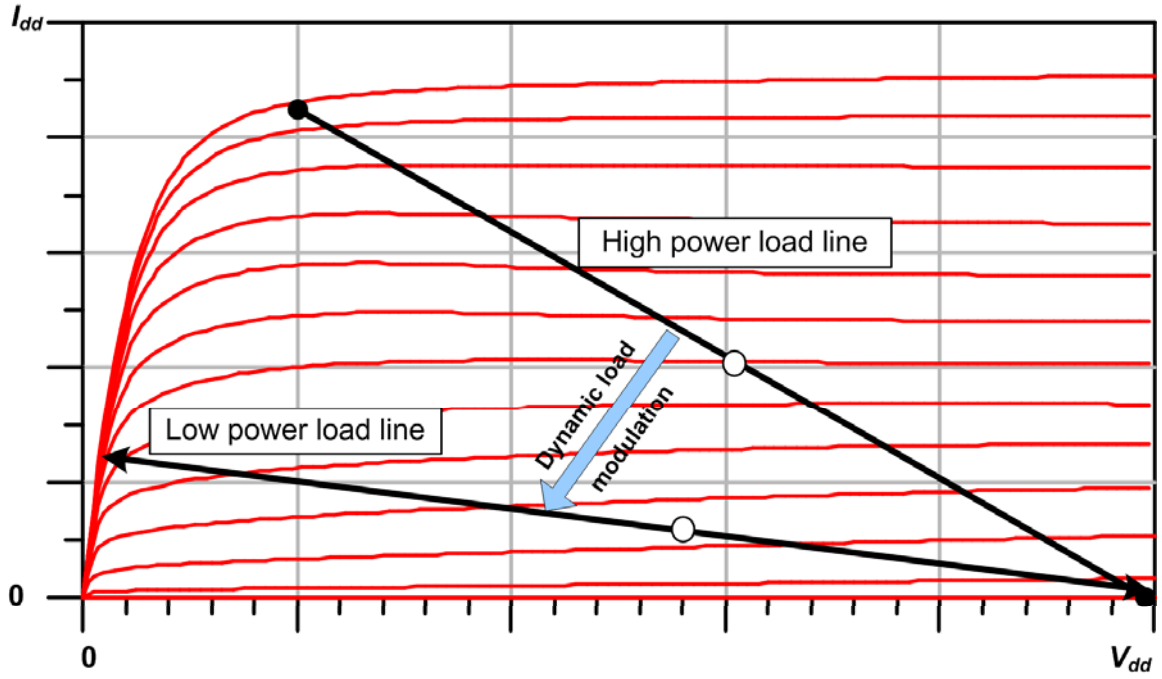
Dynamic load modulation principle

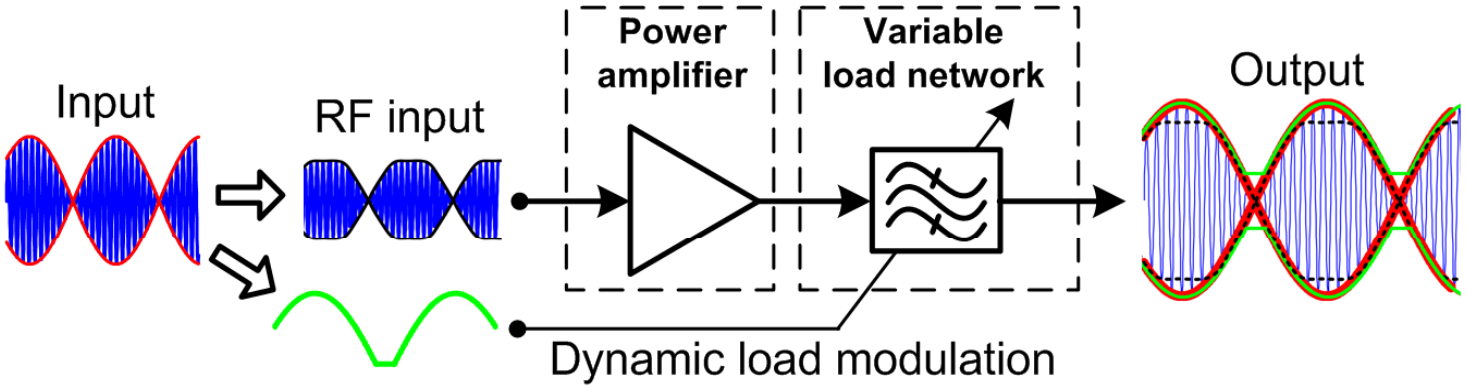
- Efficiency can be improved if the PA load impedance is increased at low power
  - Average dc current is decreased, while maintaining full voltage swing



- Desired load impedance variations can be generated actively
  - E.g. in Doherty amplifiers
- or using a reconfigurable load network…

Dynamic load modulation architecture

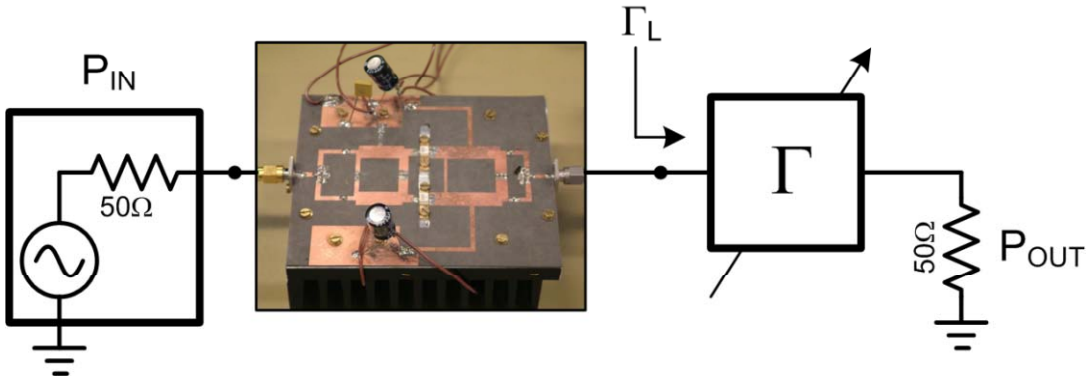
- Variation of output power by dynamically tuning the PA load network



- Varactors typically used as tuneable elements
  - Breakdown voltage > 100V
  - Low series resistance, large tuning range
- Simple and efficient electronics can be used for the control
  - No need for high power dc converters etc.
  - Potentially wideband modulation

Static load modulation measurements

- A passive load-pull tuner is used to realize a statically tunable load impedance

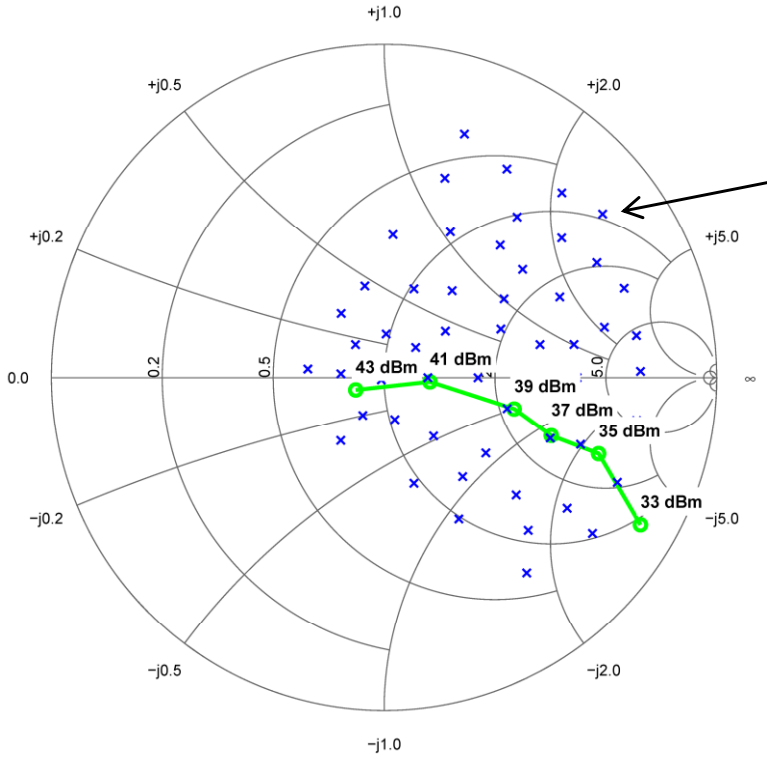


- Static PA characterization of efficiency and P_{out} vs. P_{in} and Γ_L

$$PAE_{PA}\left(P_{in},\Gamma_L\right)=\frac{P_{out}\left(P_{in},\Gamma_L\right)-P_{in}}{P_{dc}\left(P_{in},\Gamma_L\right)}$$

- Similar type of characterization as the supply modulation case

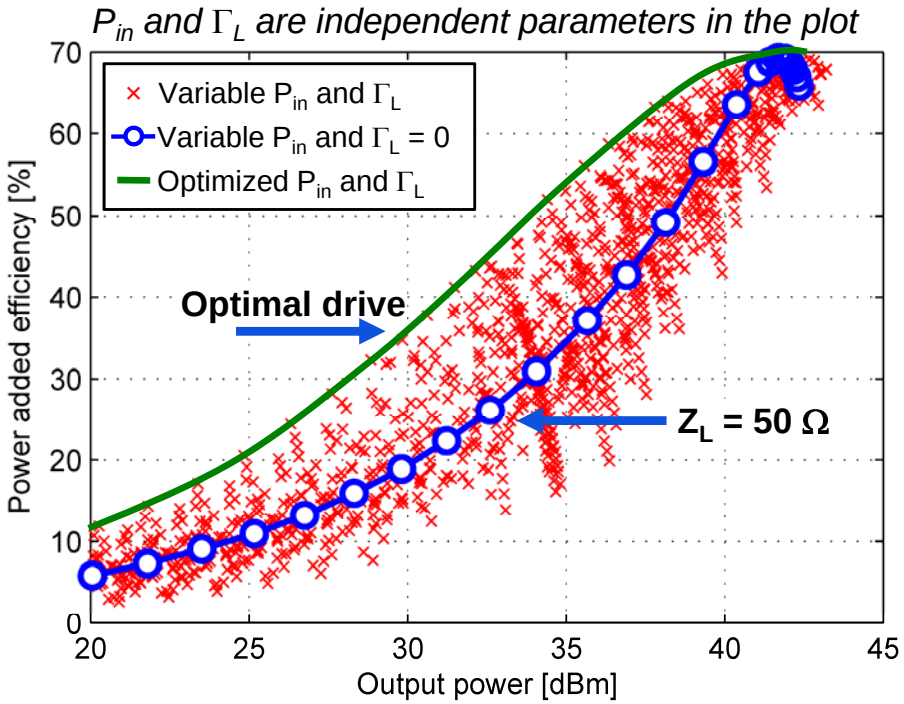
Measured optimum load impedance locus



Load impedance points tested

- The Γ_L and P_{in} combination that maximizes efficiency can be determined for every given P_{out}
  - At max output power, efficiency is maximized for 50Ω
  - A higher impedance is desired at reduced output power

Optimized load modulation performance for LDMOS class D^{-1} PA



Simulated results with W-CDMA input signal statistics

Drive condition	$<\eta_{PA}>$ (%)	
	PAPR 10.3 dB	PAPR 6.6 dB
Traditional (Z_L = 50 Ω)	24%	36%
Optimum P_{in}/Γ_L drive	43%	57%

- Simultaneous P_{in} and Γ_L control can also give a significant efficiency improvement even with an existing PA
  - Design of tunable matching networks for high power applications is still a matter of research

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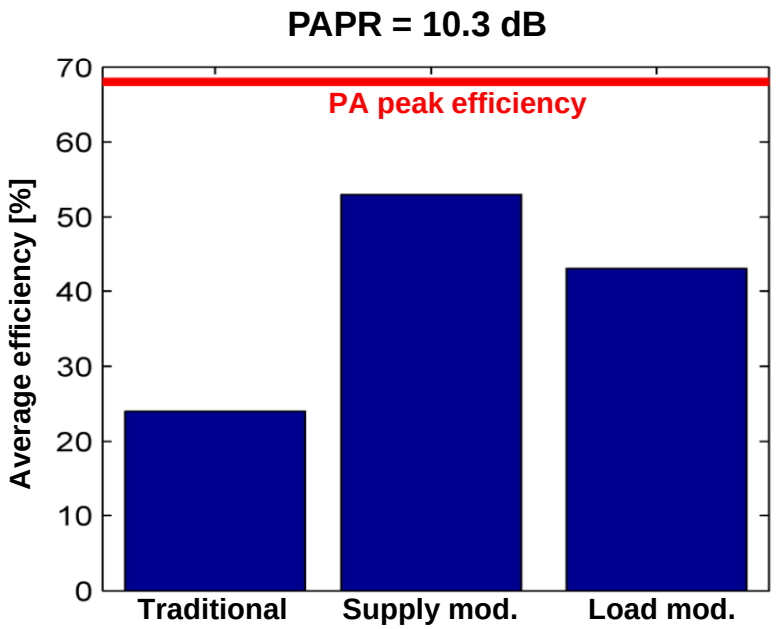
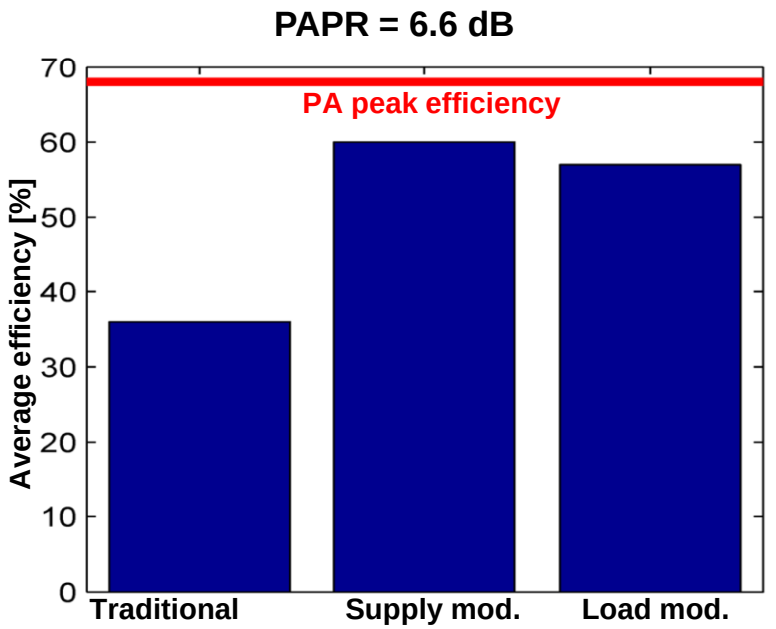
Static supply and load modulation characterization for LDMOS class D^{-1} PA

- Summary of efficiency predictions with WCDMA signal statistics





- Both supply voltage and load impedance modulation show high potential for efficiency enhancement with existing PAs

Conclusions

- Existing LDMOS class D^{-1} PA evaluated in supply and load modulation transmitter architectures
  - Static characterization used
  - Average efficiency estimated using WCDMA signal statistics
- Both architectures show promising results with the PA tested
  - Similar performance enhancement is observed with other transistor technologies and amplifier classes
- Modulator losses are not included
  - Efficiency and bandwidth limitations in envelope modulators for supply modulation
  - Varactor and network losses/limitations in load modulation architectures
- Careful co-control of two input signals needed for maximum efficiency performance
  - New challenges in linearization and behavioural modelling

Thank you for your attention!

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