Quad-band GSM Power Amplifier by optimized BCD RFLDMOS

This work has been supported and founded by the Italian Research and University Ministry (MIUR) throughout the project:

Reduced Electrosmog Society Technology

Andrea Pallotta – FTM Smart Power & HV Tech. Department

IEEE Topical Workshop on Power Amplifiers for Wireless Communications, San Diego 15-17 Jan. 2006

STMicroelectronics

RF-LDMOS Cross-section

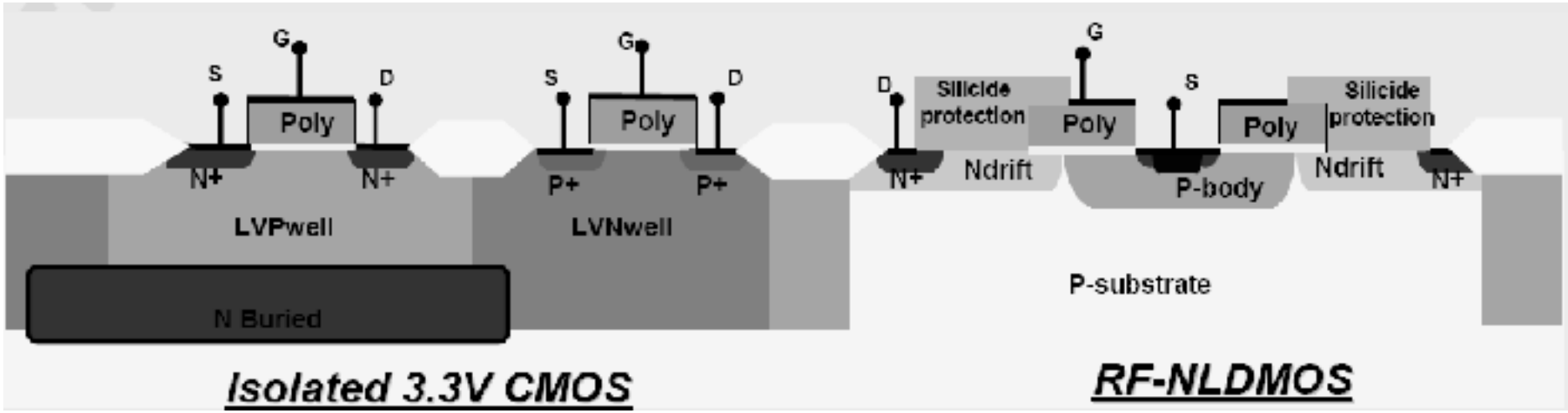
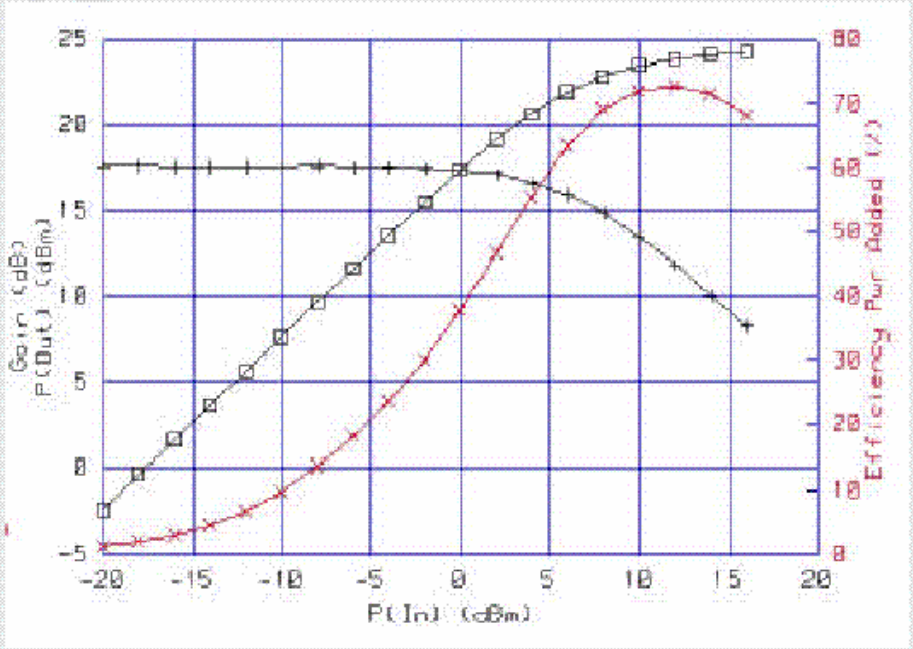


Table I

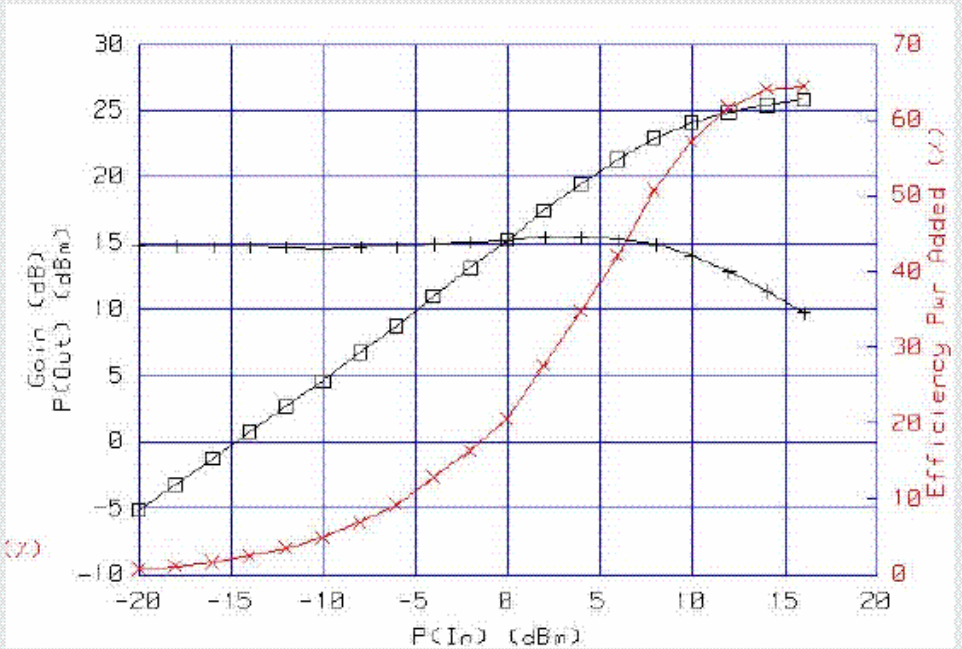
Parameter	Value	Test Condition
BV_{DSS} [V]	16	I_{DS} = 0.01 nA/µm
I_{OFF} [pA/µm]	<1	V_{DS} = 5 V V_{GS} = 0
*Ron*W* [Ω*mm]	2.8	V_{GS} = 3.3 V V_{DS} = 0.1 V
Gm/W [mS/mm]	200	V_{DS} = 3.5 V
I_{SAT}/W [mA/mm]	480	V_{DS} = 3.5 V
F_T [GHz]	18	V_{DS} = 3.5 V

W=2.8mm RF-LDMOS load-pull measurements

Vd = 3.5 V; Vg = 0.7 V



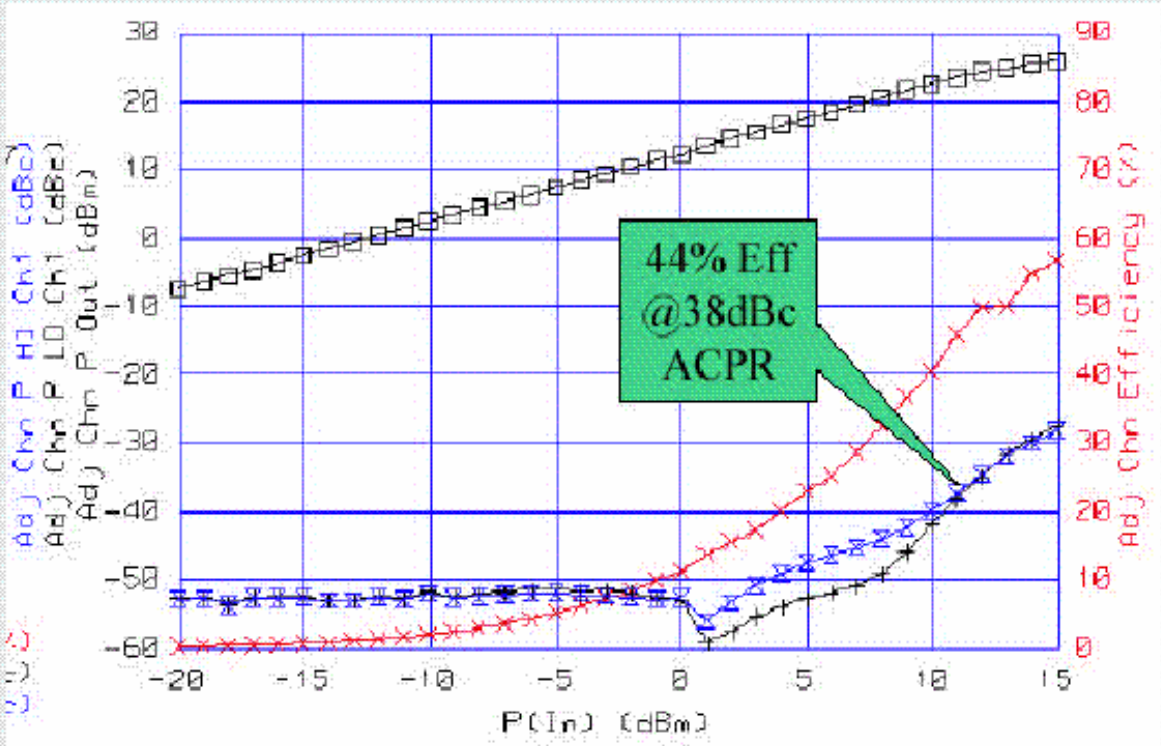
f_0 = 0.9 GHz
Pout $_{max}$ = 24.3 dBm
PAE $_{max}$ = 73 %



f_0 = 1.8 GHz
Pout $_{max}$ = 25.8 dBm
PAE $_{max}$ = 65 %

W=2.8mm RF-LDMOS W-CDMA ACPR measurements

Vd = 3.5V; Vg = 0.7 V

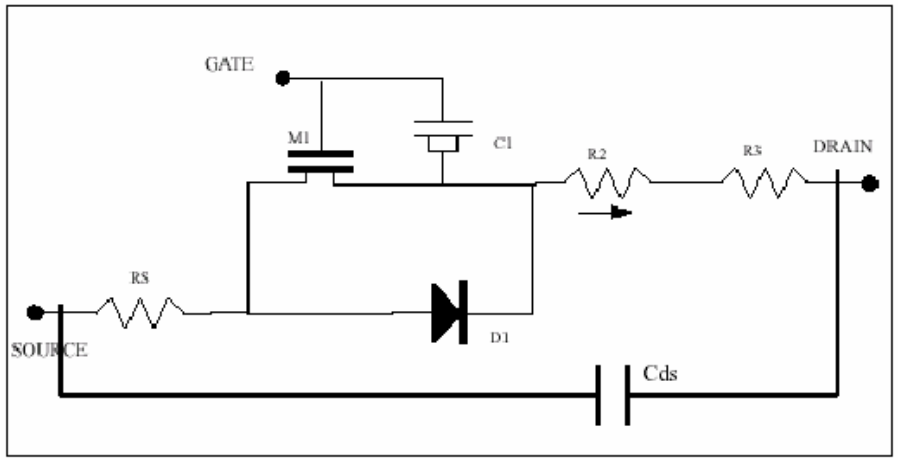


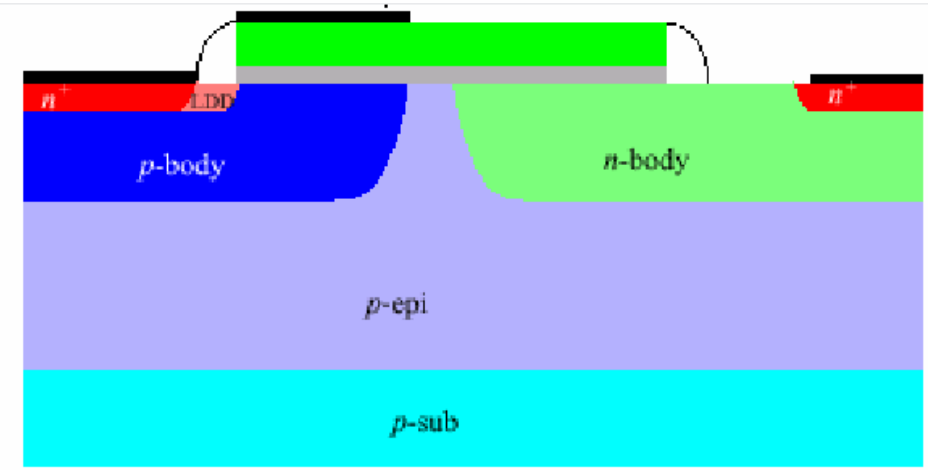
$f_0 = 2$ GHz

$Pout_{max}$ (@ ACPR -38dBc) = 23 dBm

PAE_{max} (@ ACPR -38dBc) = 44 %

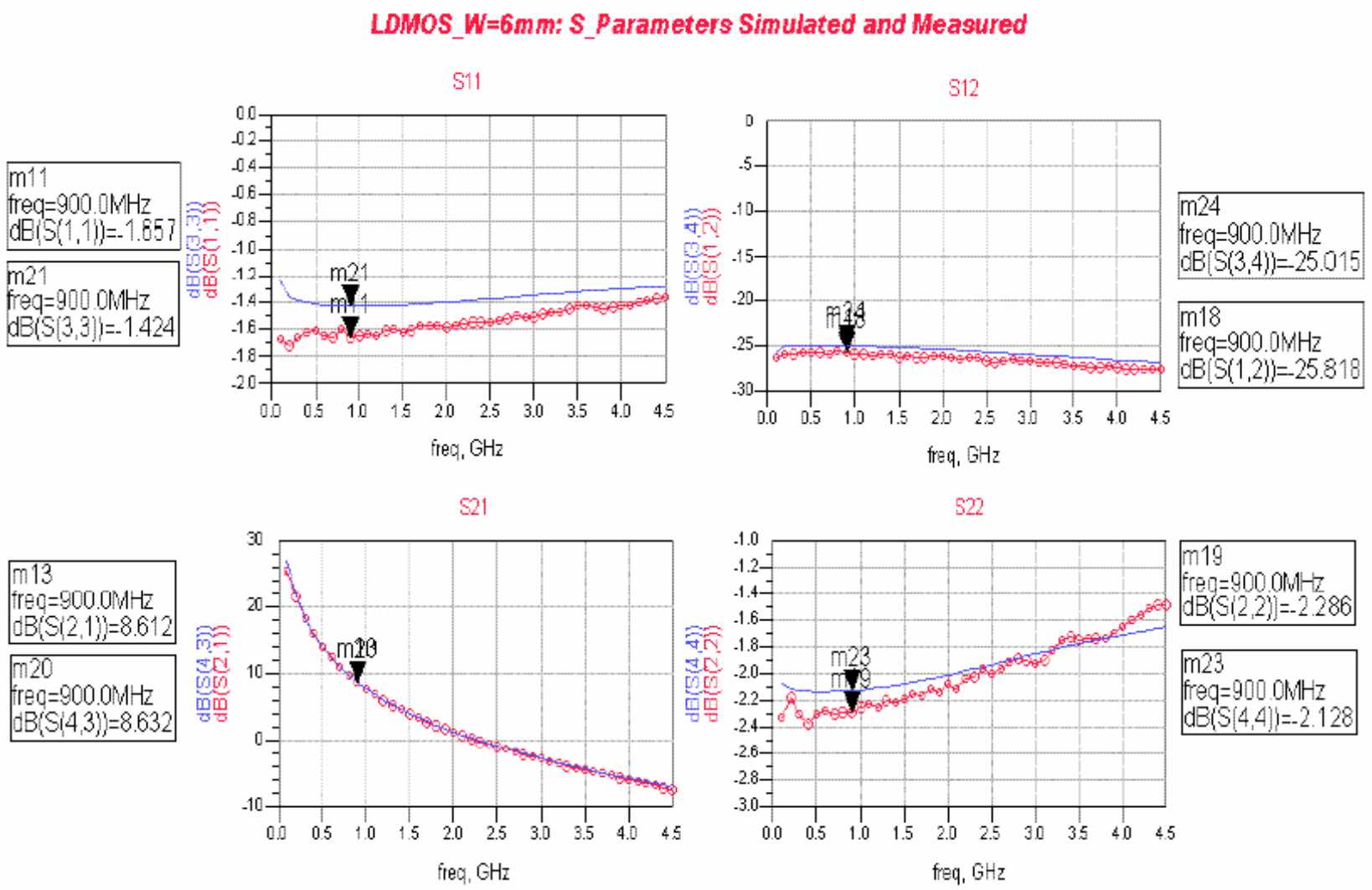
RF-LDMOS sub circuit model



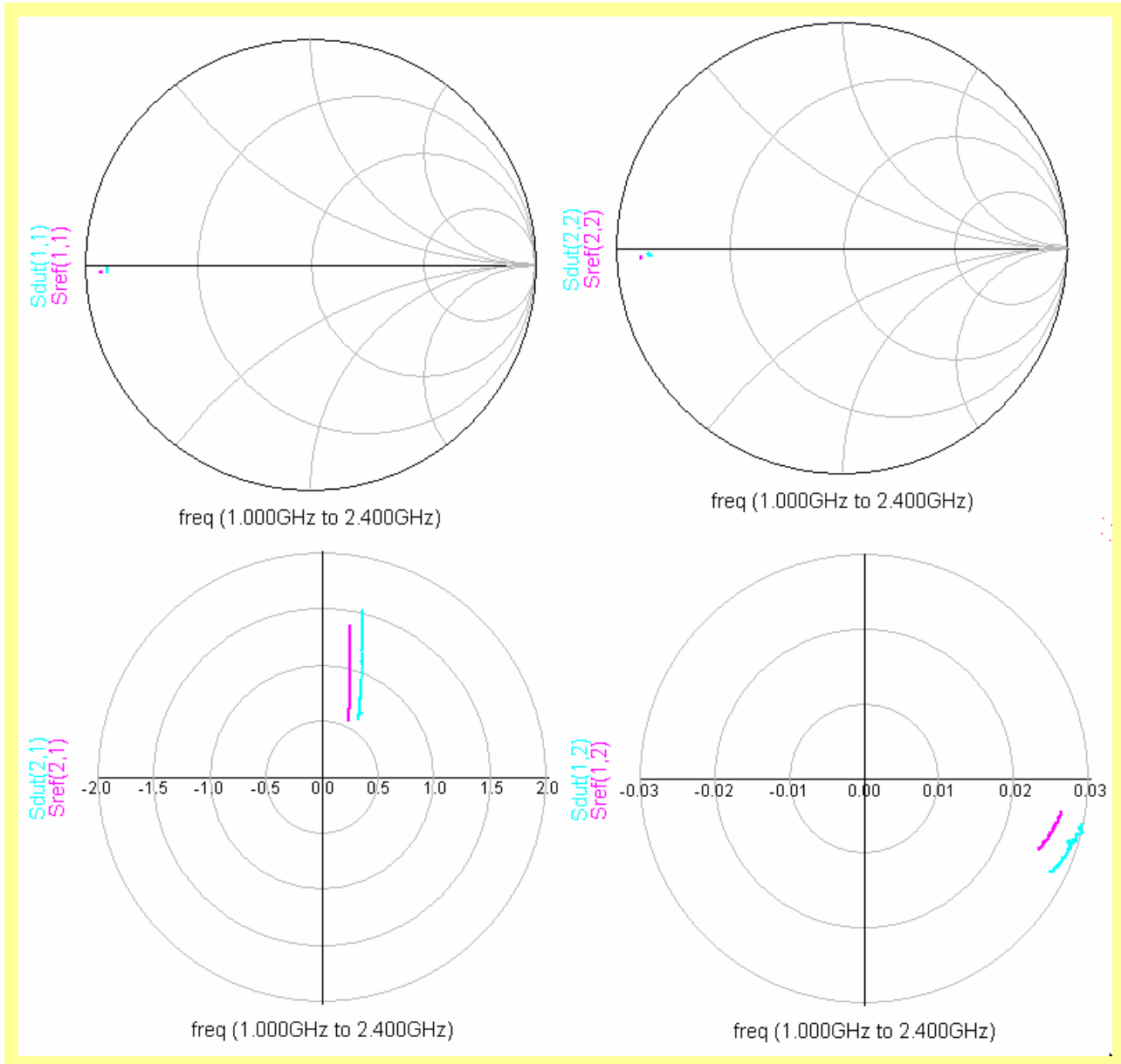


- M1: BSIM3 compact model
- C1: Non linear MOS capacitor included in BSIM3 model
- R2: Non linear resistor modulated by gate Bias
- Rs, R3: Source/drain constant resistor
- D1: p-Epi/n-body diode
- Cds: Parasitic drain/source overlap metal capacitances

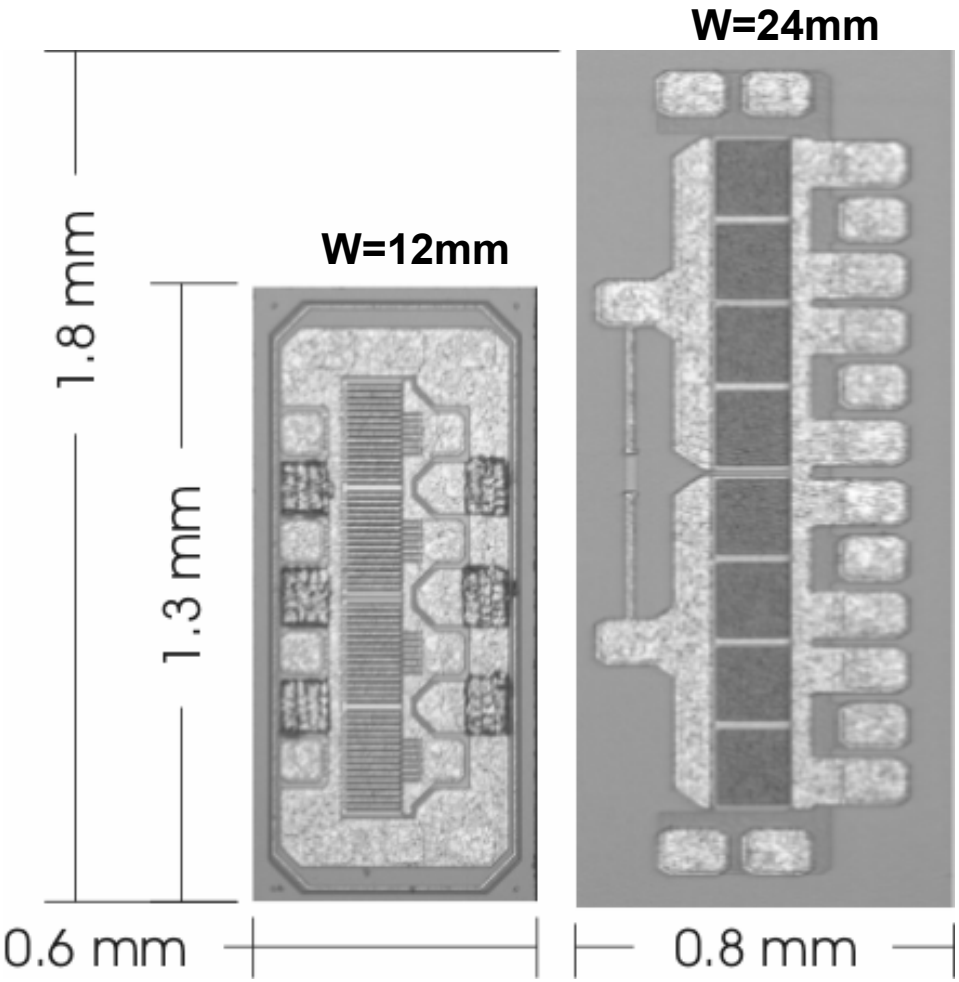
W=6 mm RF-LDMOS model vs. measurements



W=12mm RF-LDMOS model vs. measurements

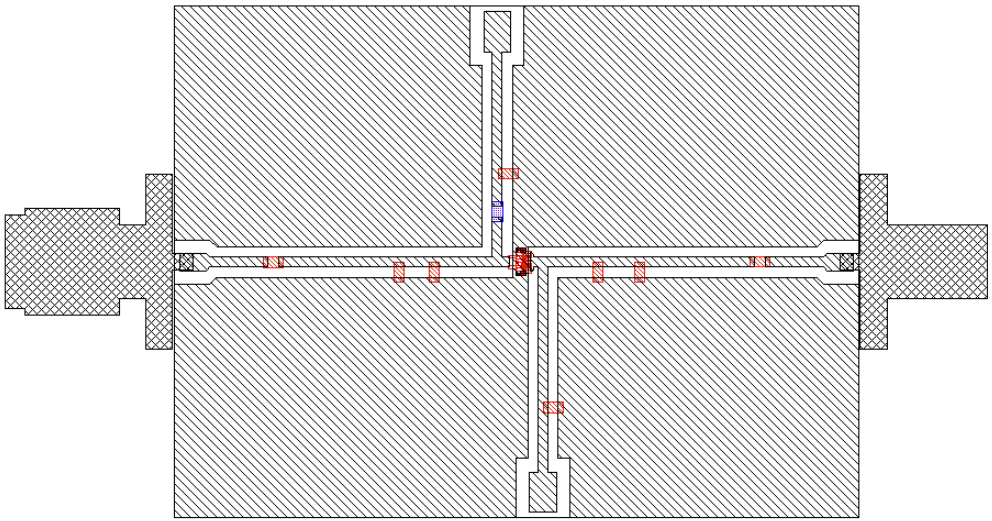


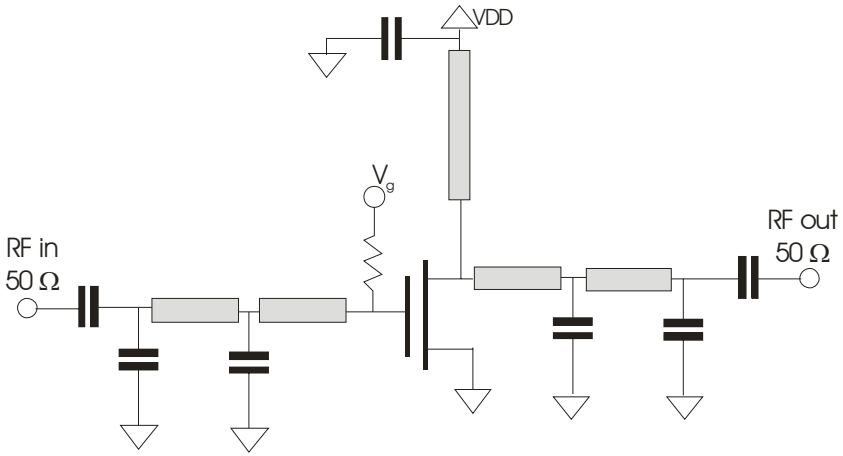
Final power RF-LDMOS transistors for GSM PA



- 120 fingers for each active area
- each finger is 25 µm long

Final power transistor test board

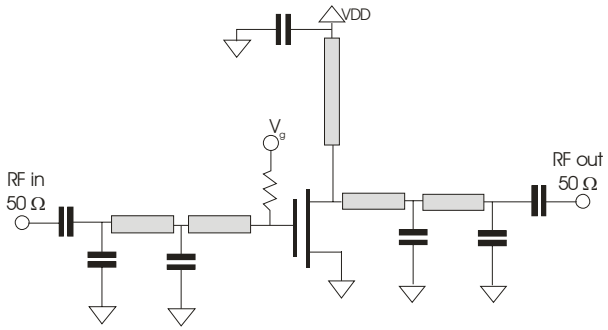




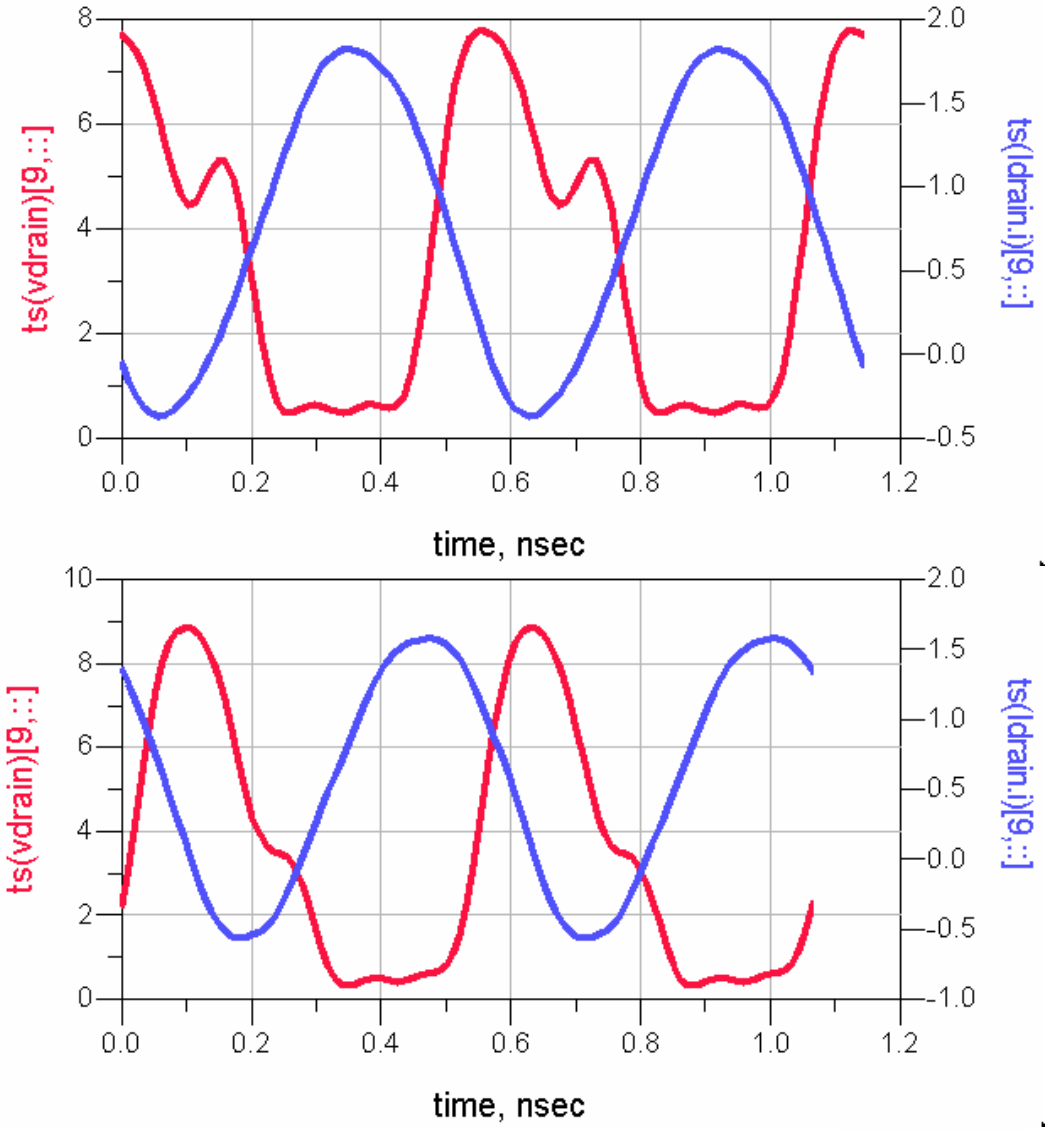
- SMD size: 0.75x1.5 mm (0603)
- Board size: 38x51 mm (BT laminate)
- Output Matching Network implemented for Harmonic Control

CAD optimization maximizing PAE and Pout (W=12mm)

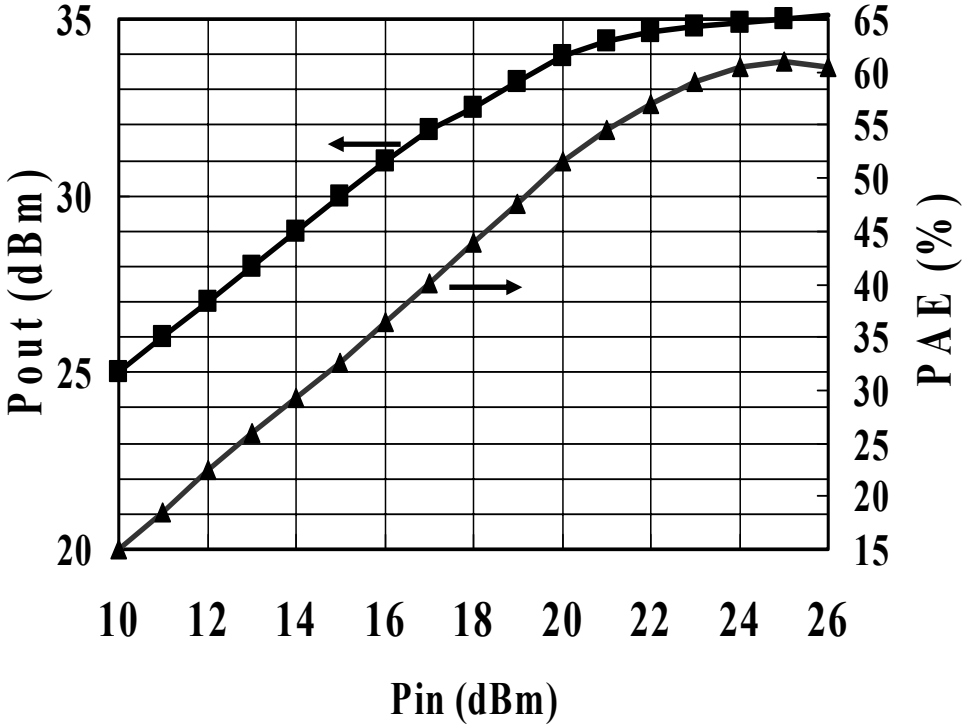
1.75 GHz
Pout = 32.5 dBm
PAE = 48%

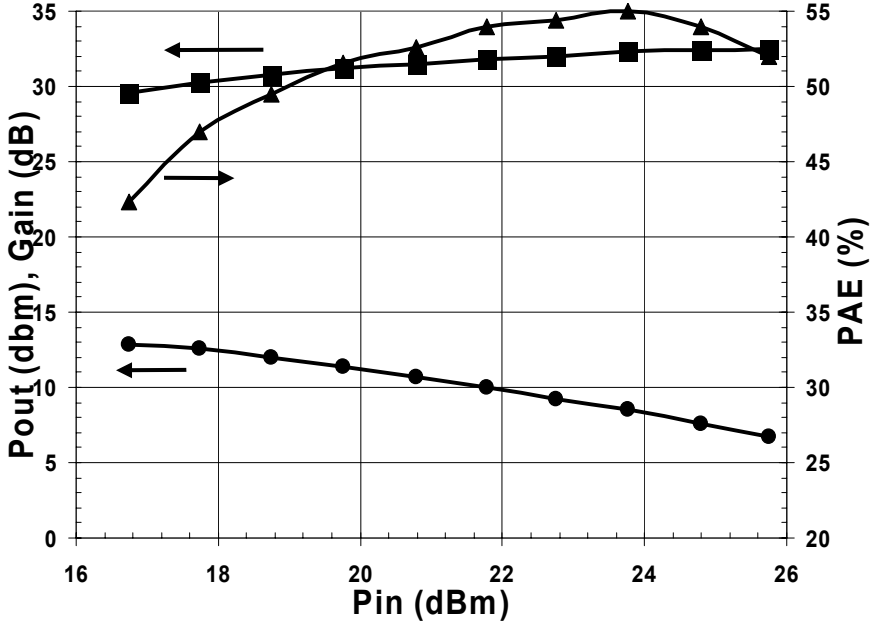


1.88 GHz
Pout = 32 dBm
PAE = 51%



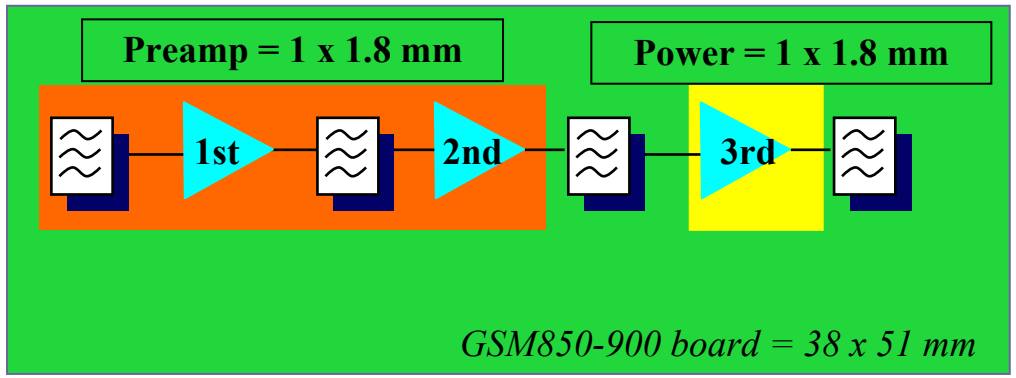
50Ω-50Ω matched final power LDMOS

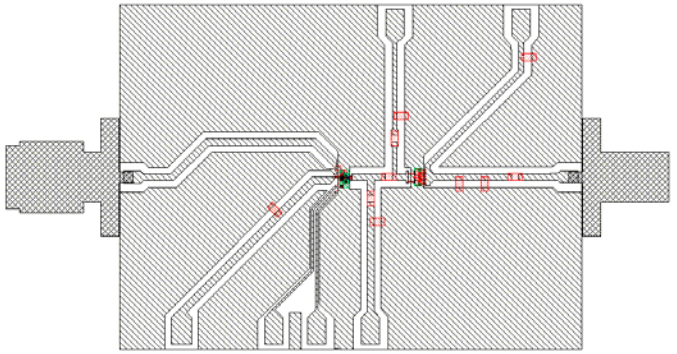


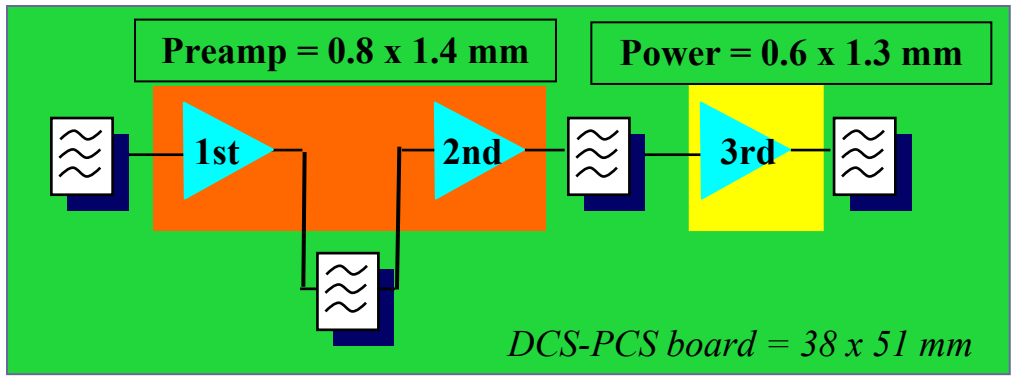


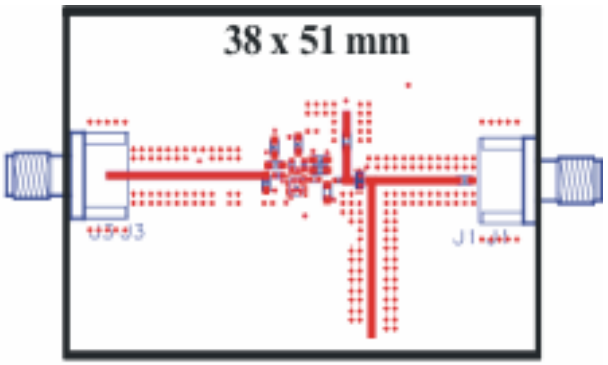
Quad-band GSM850-900 and GSM 1800-1900

RF PA on PCB in order to validate the RF-BCD technology process

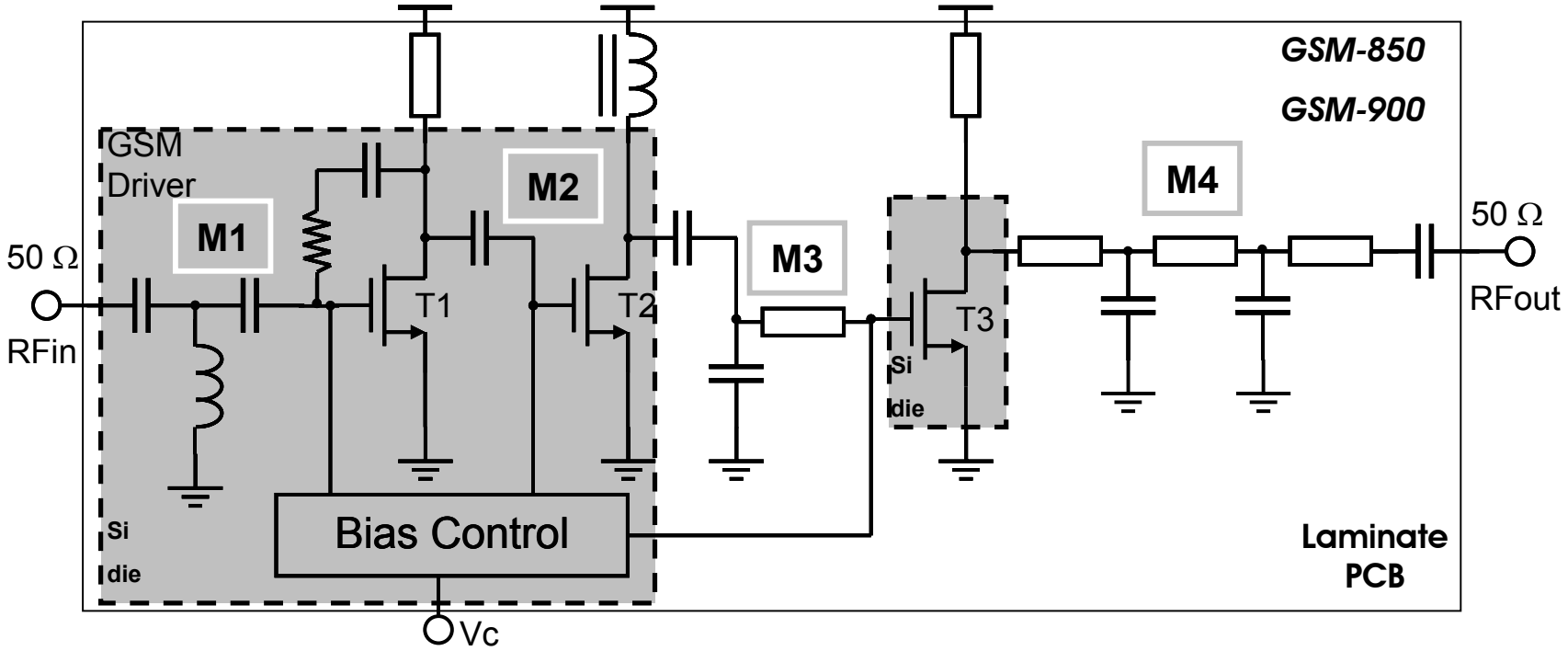


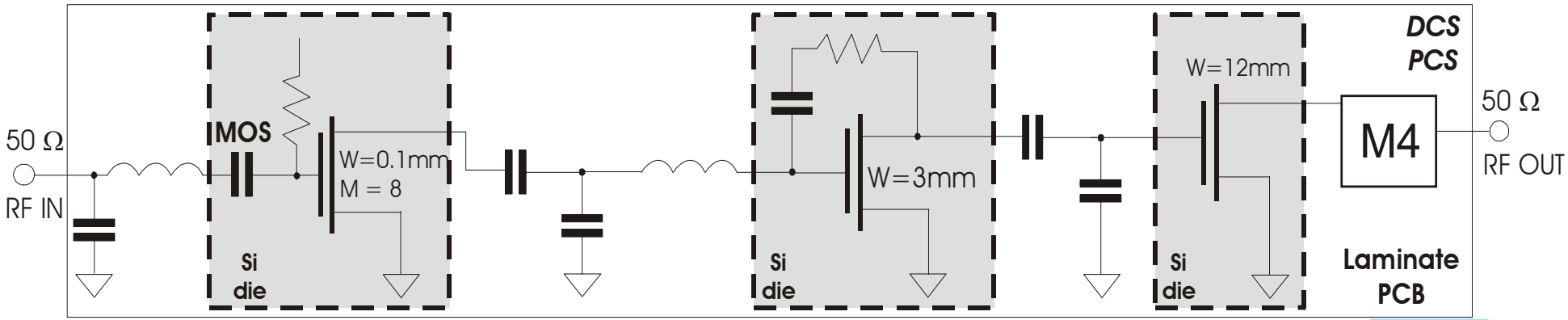




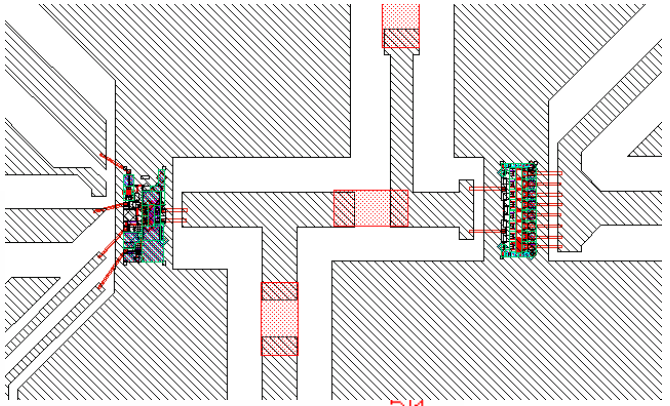


GSM850-900, DCS-PCS Circuit Schematics



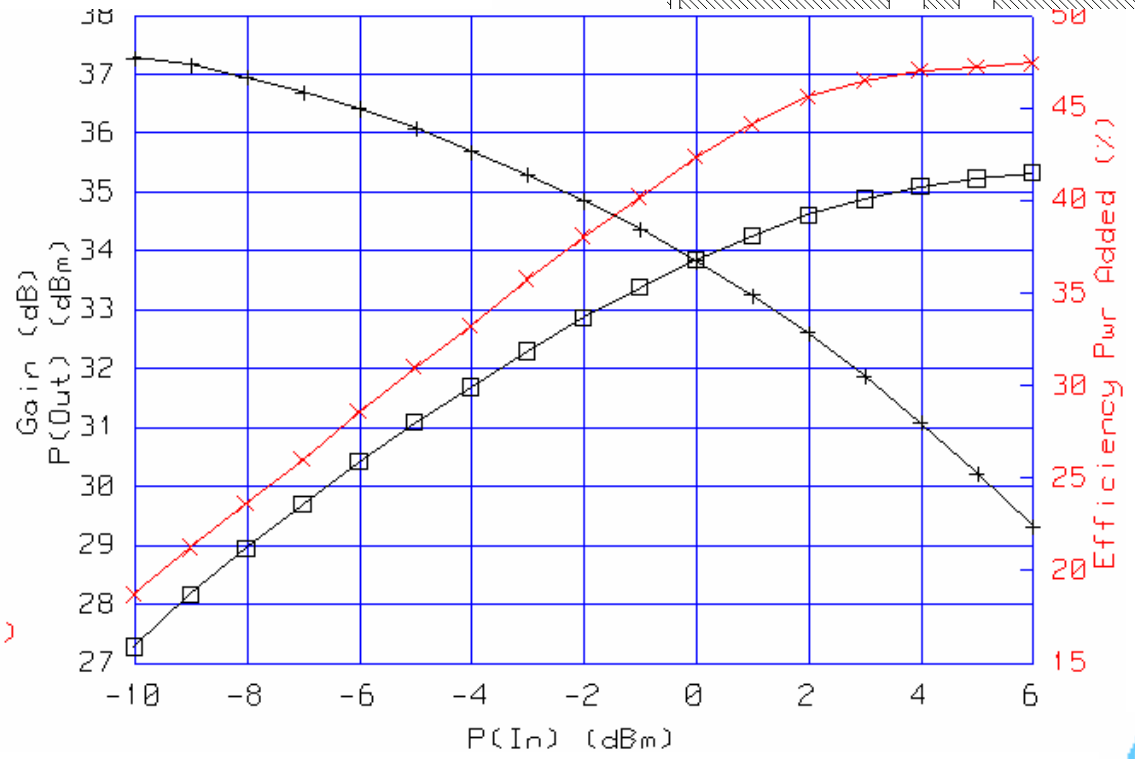


GSM850 RF PA main performances

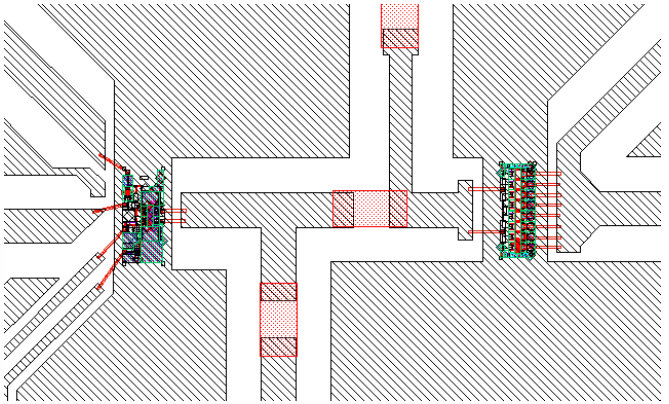


Pin=6dBm
Pout=35.3dBm
PAE=47%

Frequency (f0): .84 GHz
Source Gamma: .02 -32.1
Bias Values Read:
vg: .800 V, ig: 5.254 mA
vd1: 3.501 V, id1: 18.040 mA
vd2: 3.504 V, id2: 104.871 mA
vd3: 3.502 V, id3: 447.667 mA
Load Gamma: .01 4.3
Max Pout: 35.3 dBm
Max Gain: 37.3 dB
Max Eff Add: 47.42%
No compression (1)

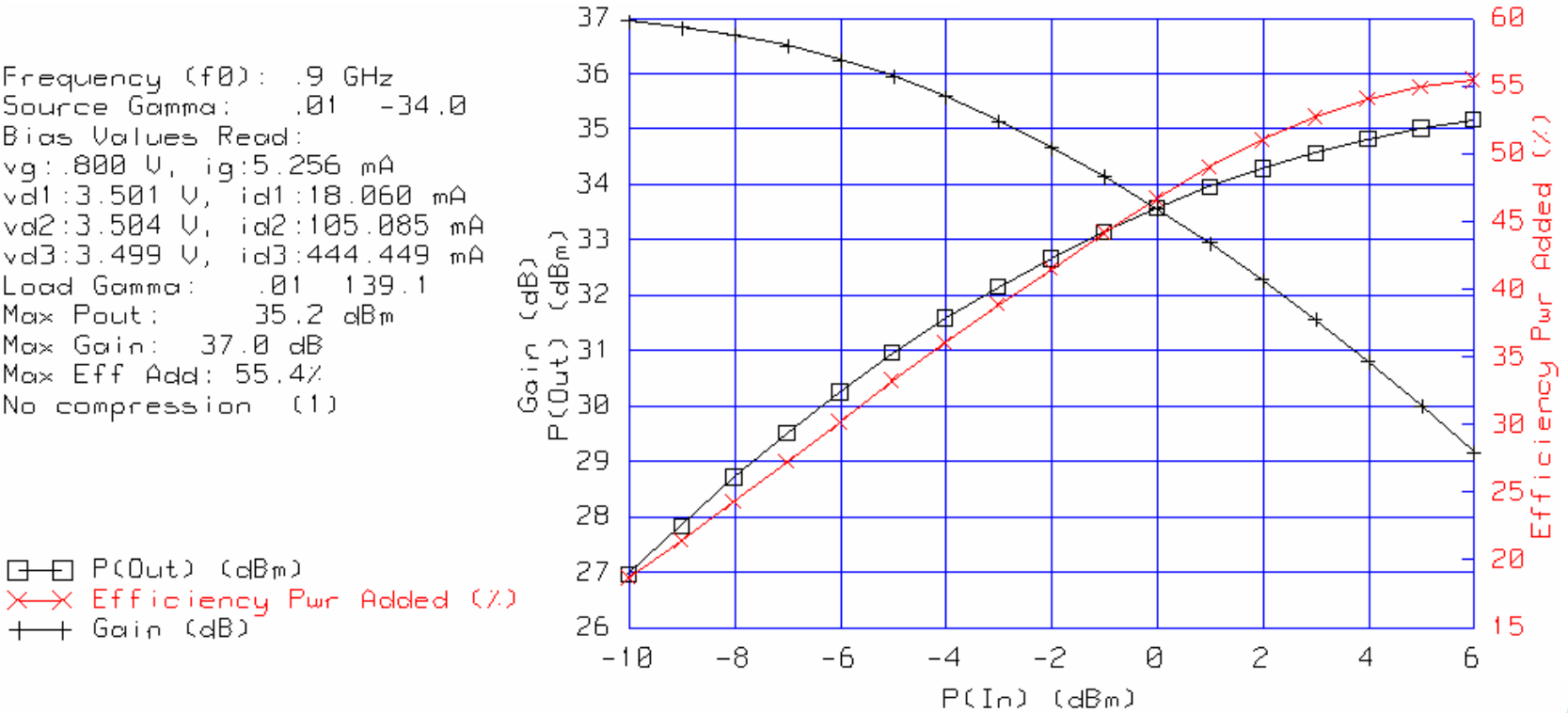


GSM900 RF PA main performances

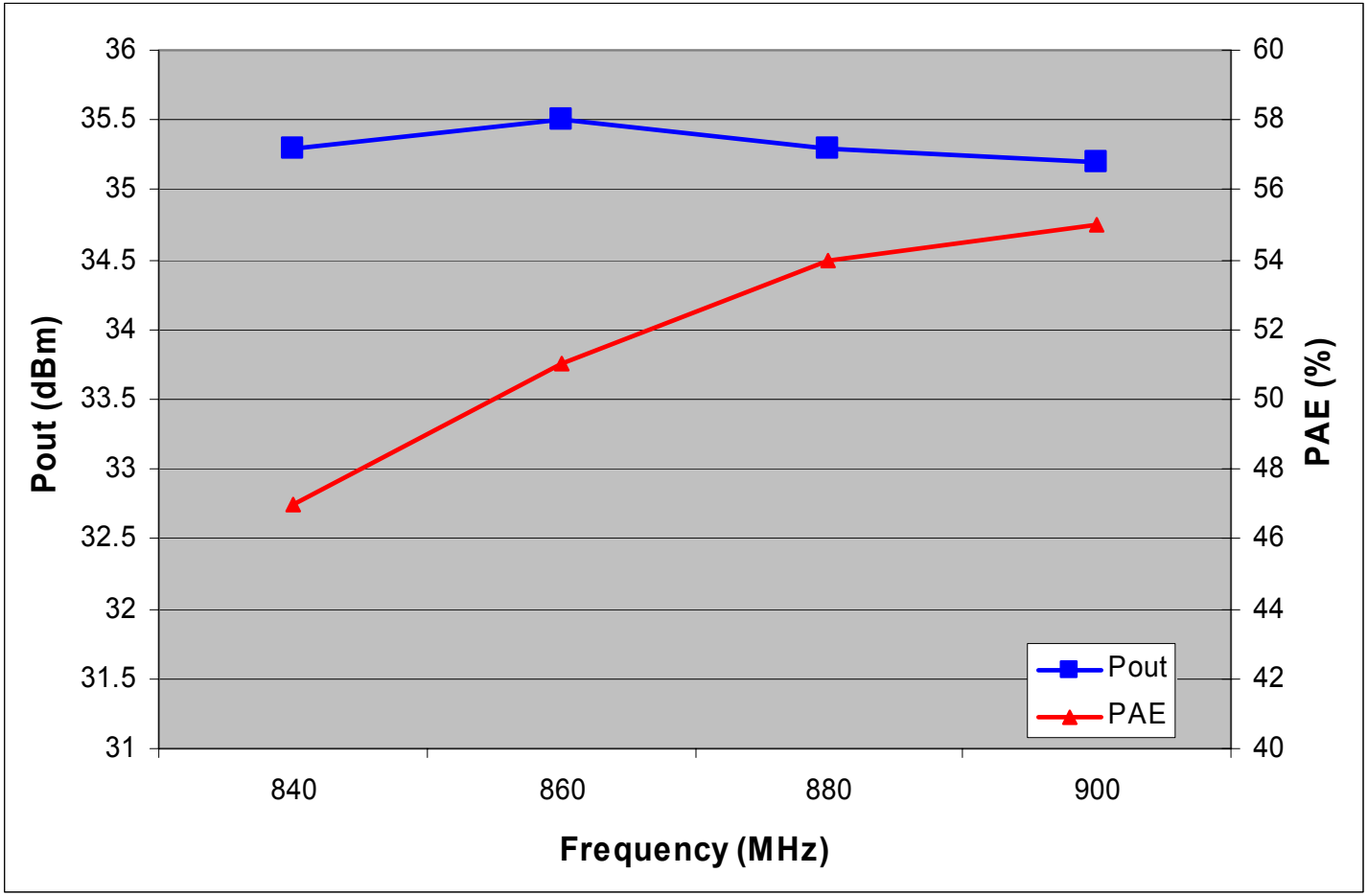


Pin=6dBm
Pout=35.2dBm
PAE=55%

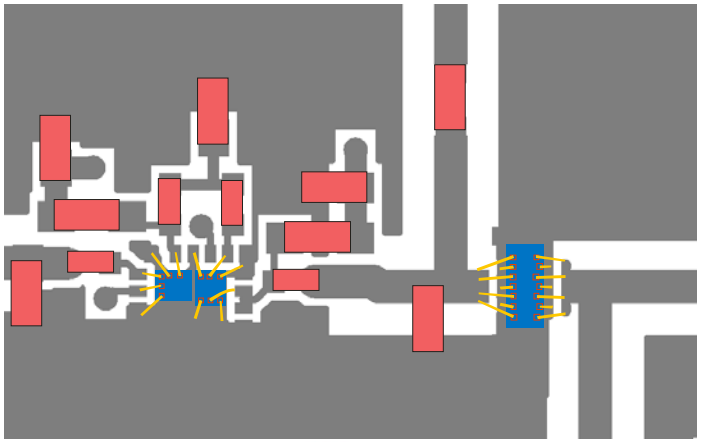
```
Frequency (f0):  .9 GHz
Source Gamma:    .01   -34.0
Bias Values Read:
vg:.800 V, ig:5.256 mA
vd1:3.501 V, id1:18.060 mA
vd2:3.504 V, id2:105.085 mA
vd3:3.499 V, id3:444.449 mA
Load Gamma:      .01   139.1
Max Pout:        35.2 dBm
Max Gain:   37.0 dB
Max Eff Add: 55.4%
No compression  (1)
```



GSM900 RF PA Pout and PAE over frequency

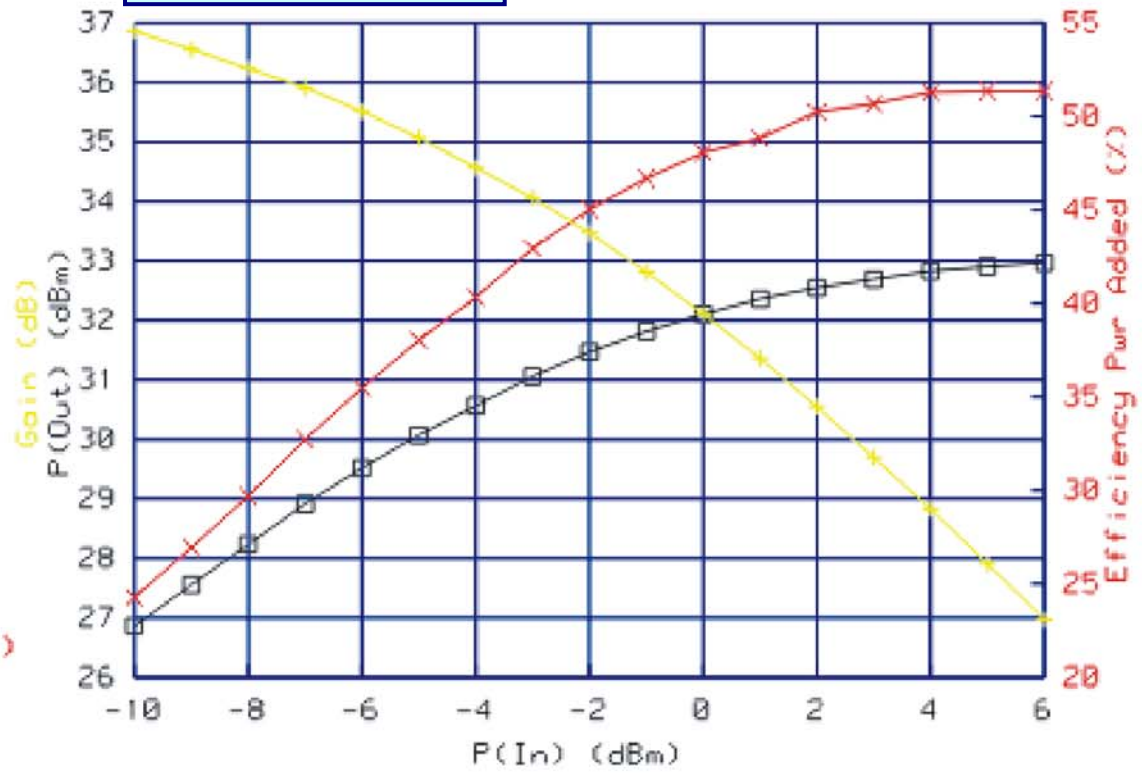


DCS RF PA main performances

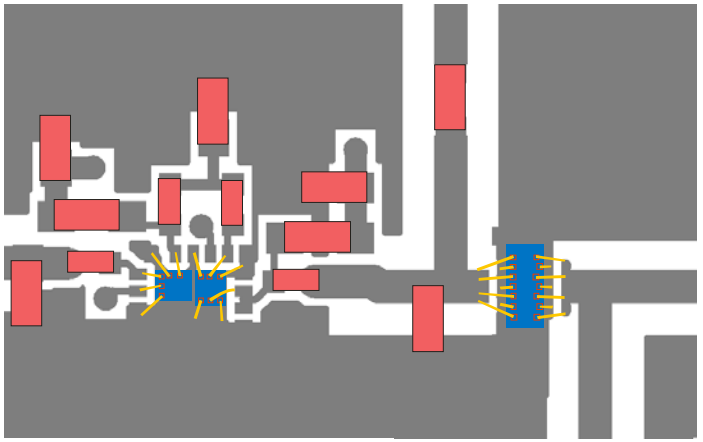


Pin=6dBm
Pout=33dBm
PAE=51.4%

```
Frequency (f0): 1.75 GHz
Source Gamma:    .01   -52.1
Bias Values Read:
vg1:3.501 V, ig1:.998 mA
vg2:.830 V, ig2:.002 mA
vg3:.853 V, ig3:-.578 mA
vd3:3.501 V, id3:426.431 mA
Load Gamma:     .02    34.1
Max Pout:       33.0 dBm
Max Gain:   36.9 dB
Max Eff Add: 51.36%
No compression  (1)
```

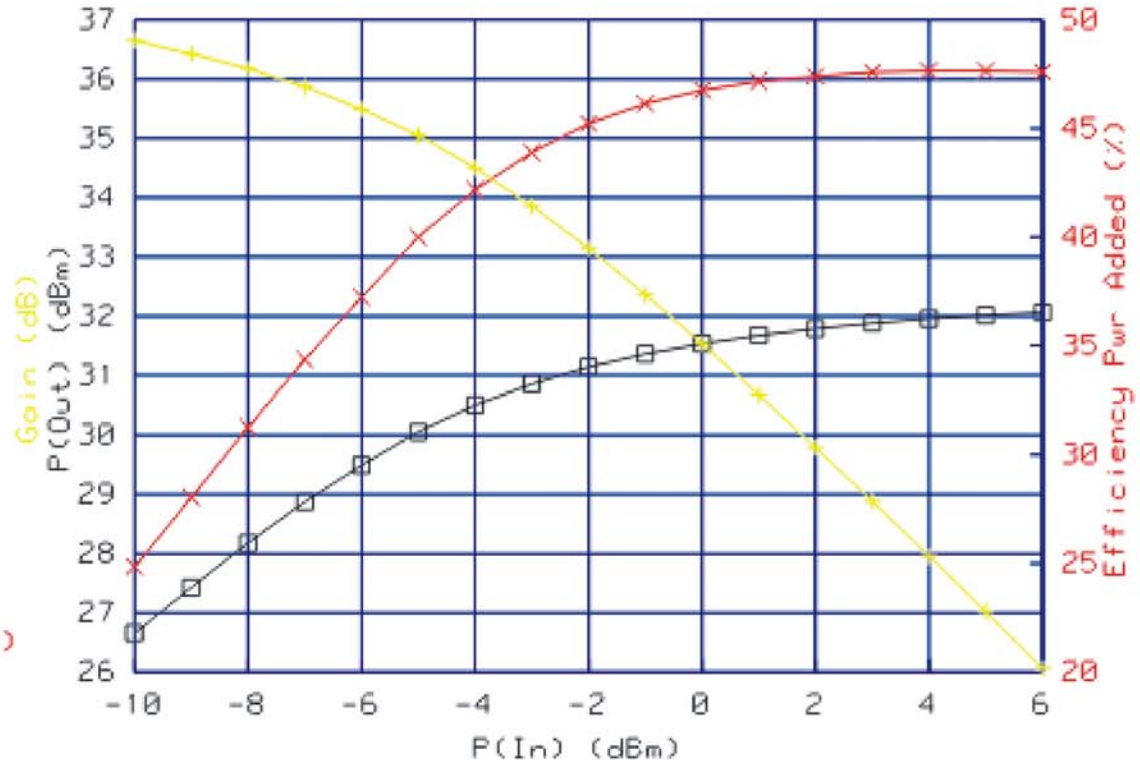


PCS RF PA main performances

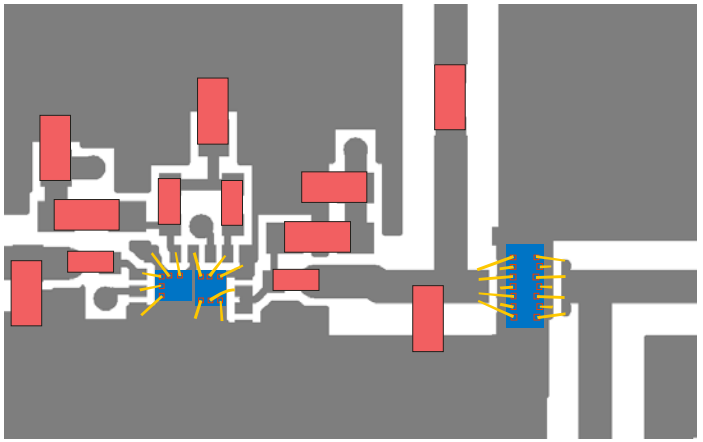


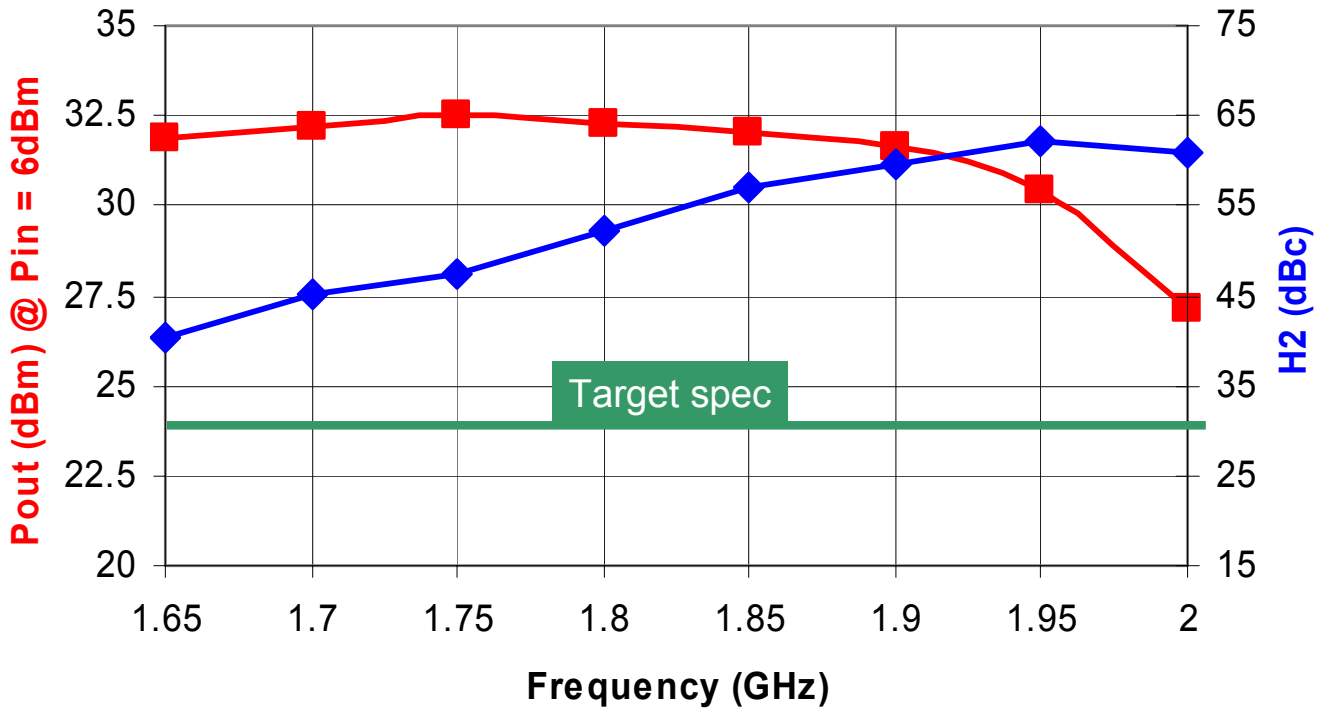
Pin=6dBm
Pout=32.1dBm
PAE=47.7%

```
Frequency (f0): 1.88 GHz
Source Gamma:    .01   43.9
Bias Values Read:
vg1:3.500 V, ig1:.968 mA
vg2:.830 V, ig2:0.000 mA
vg3:.853 V, ig3:-1.220 mA
vd3:3.501 V, id3:426.646 mA
Load Gamma:     .02  112.7
Max Pout:      32.1 dBm
Max Gain:   36.7 dB
Max Eff Add: 47.66%
No compression  (1)
```

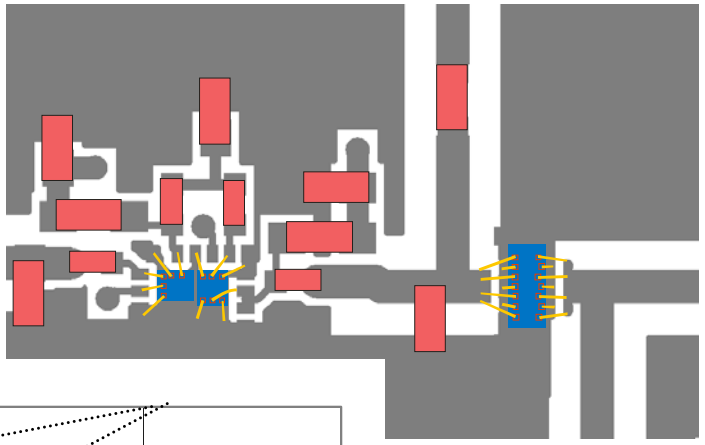


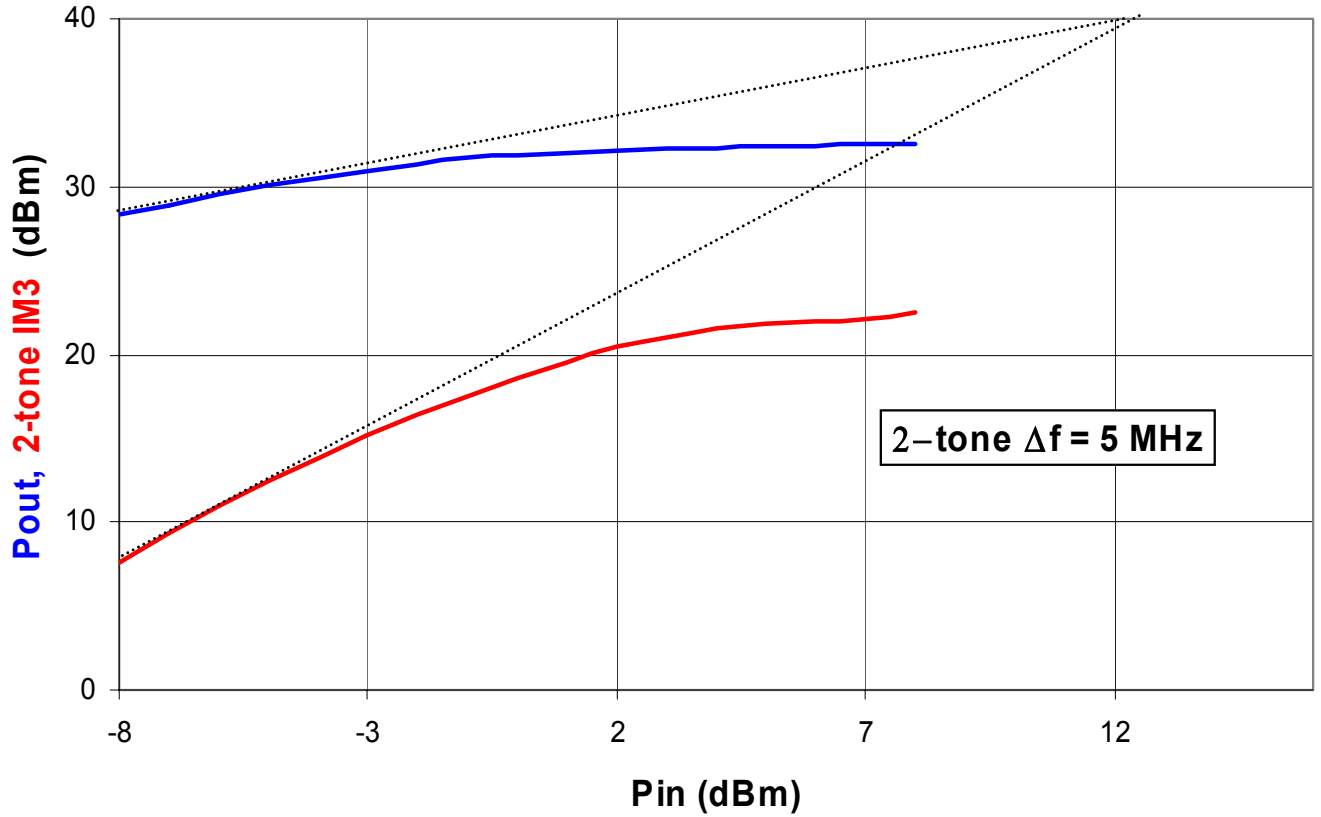
Second harmonic level in the upper band



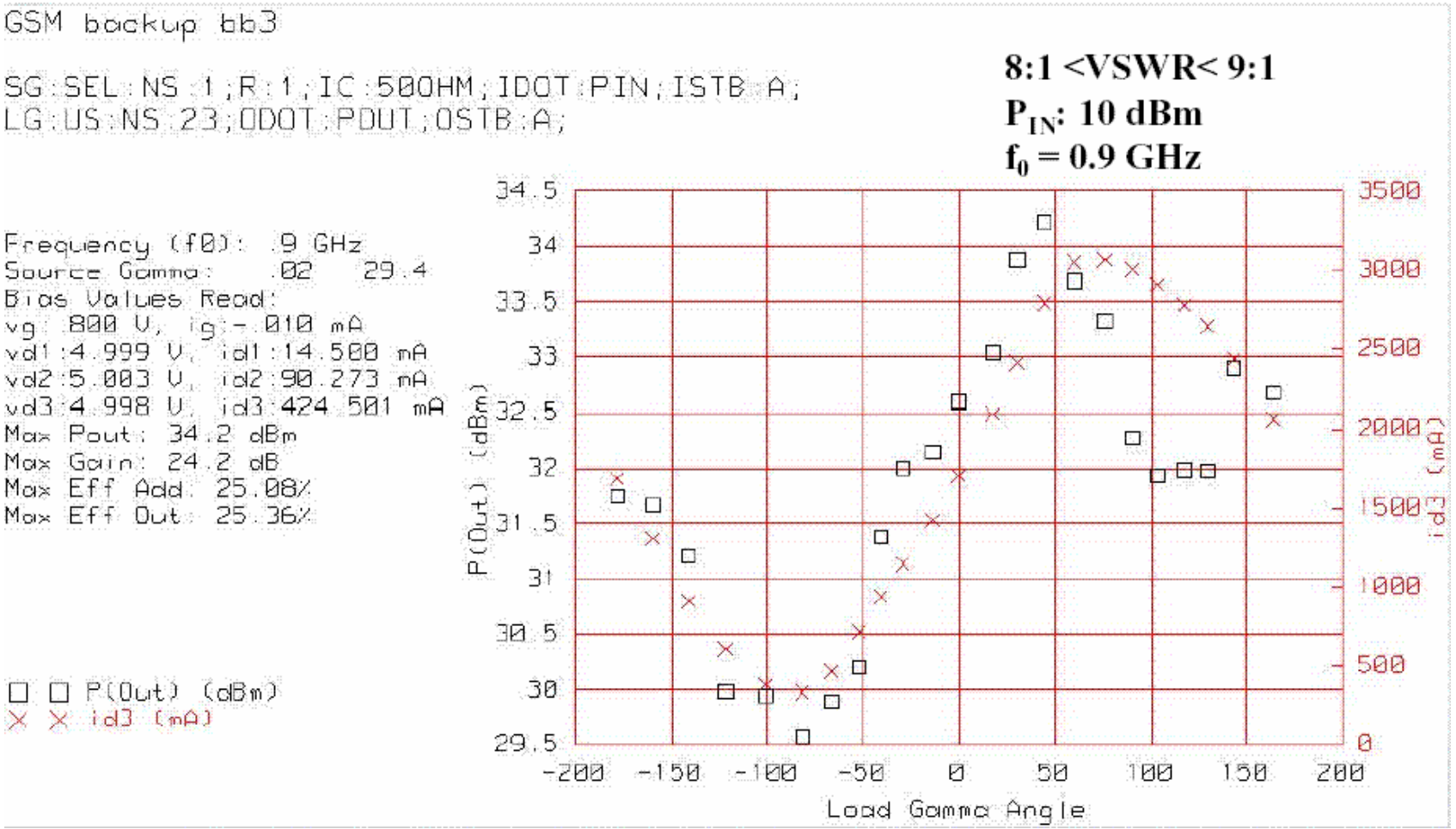


1.75GHz: 2-Tone IM3 vs. Input Power

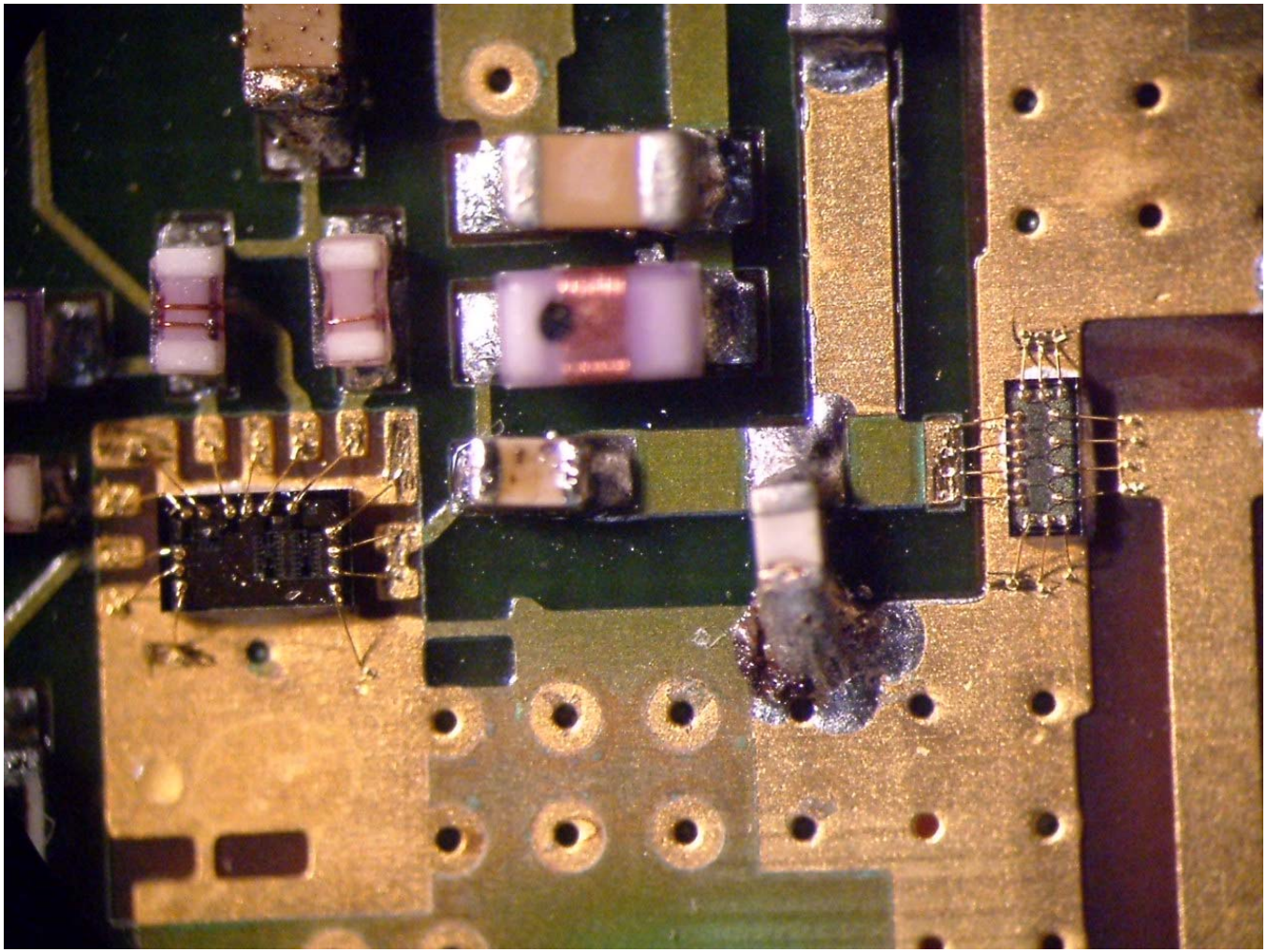




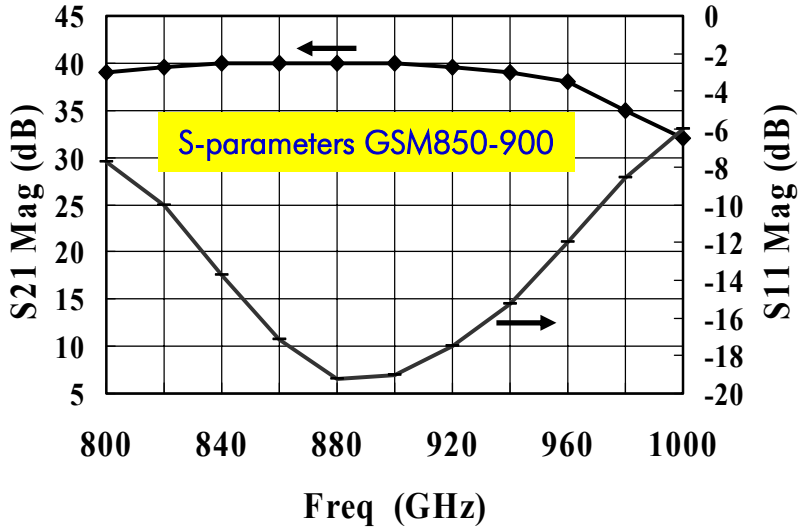
P_{out} and DC drain current vs. VSWR > 8:1 all phases @ 5 V

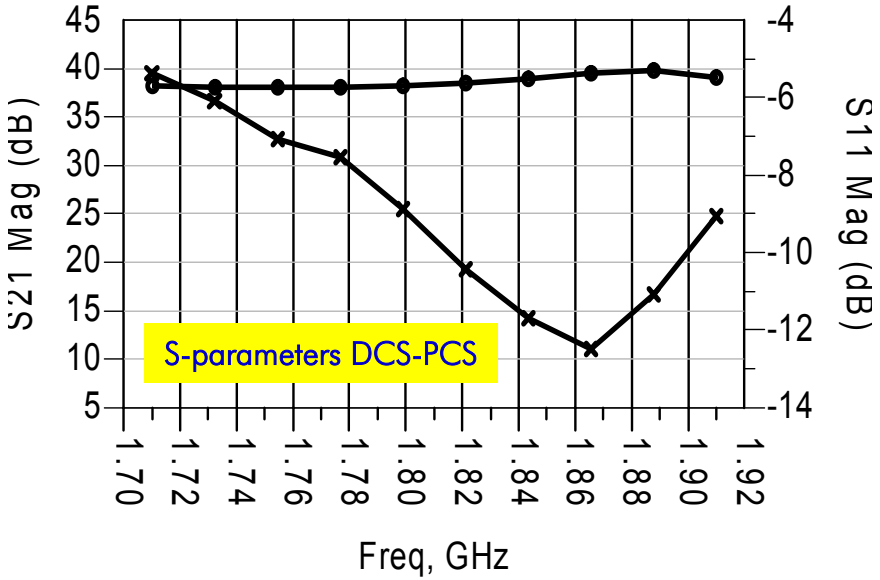


DCS PA on PCB board detail



GSM850-900, DCS-PCS on board summary

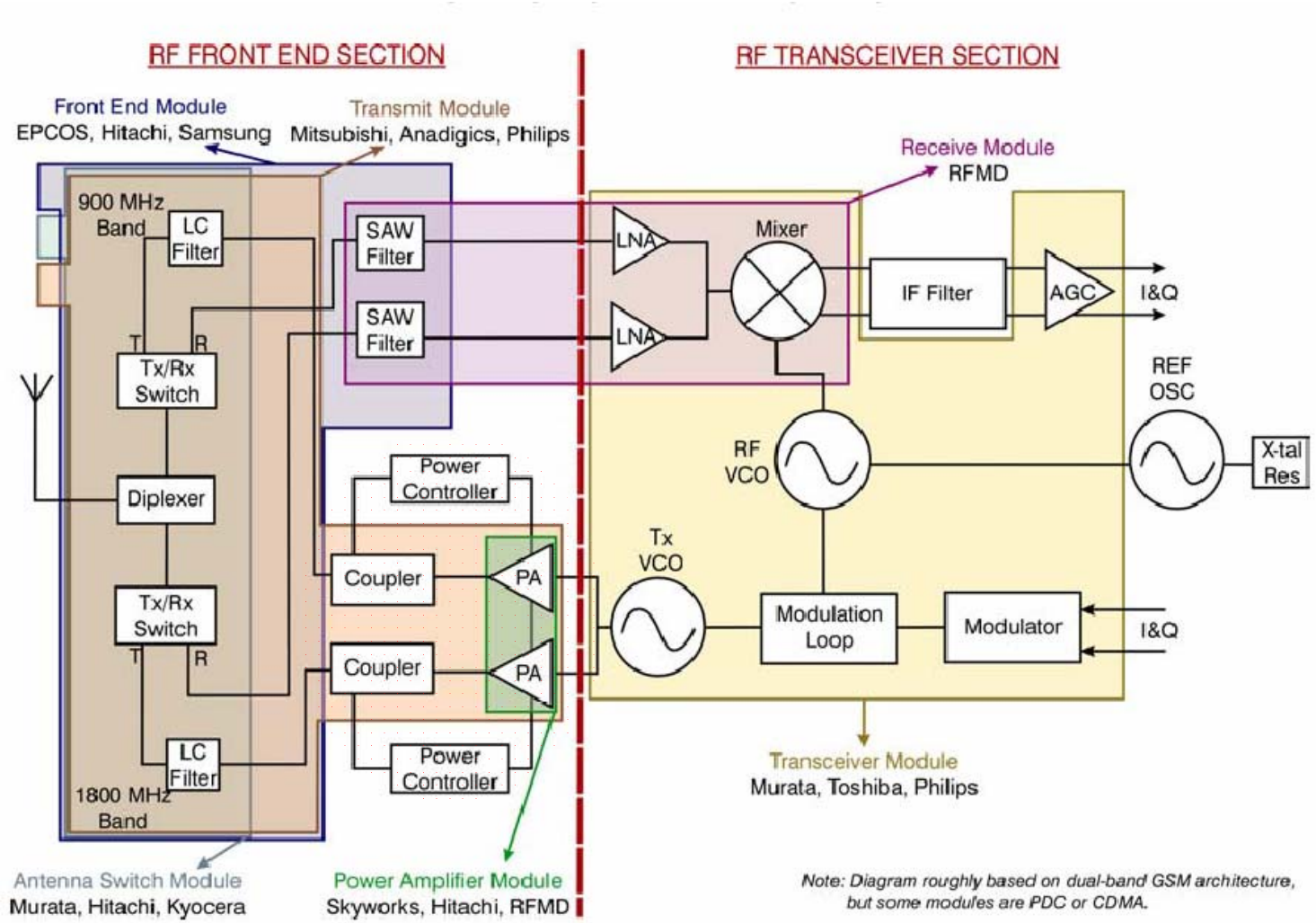




	GSM-850 (board)	GSM-900 (board)	SOA* GSM (module)		DCS (board)	PCS (board)	SOA* DCS/PCS (module)
PIN (dBm)	3	3	0		3	3	0
POUT (dBm)	35	35	35		32.5	32	32.5 / 32
PAE (%)	47	52	47		51	47	47 / 47

* SOA: State Of the Art LDMOS based GSM PA module available on the market

RF front end module moves towards high integration level => LTCC



8x8mm Quad-Band GSM850-900 & DCS-PCS PA on LTCC