POSTECH Activities on CMOS based Linear Power Amplifiers

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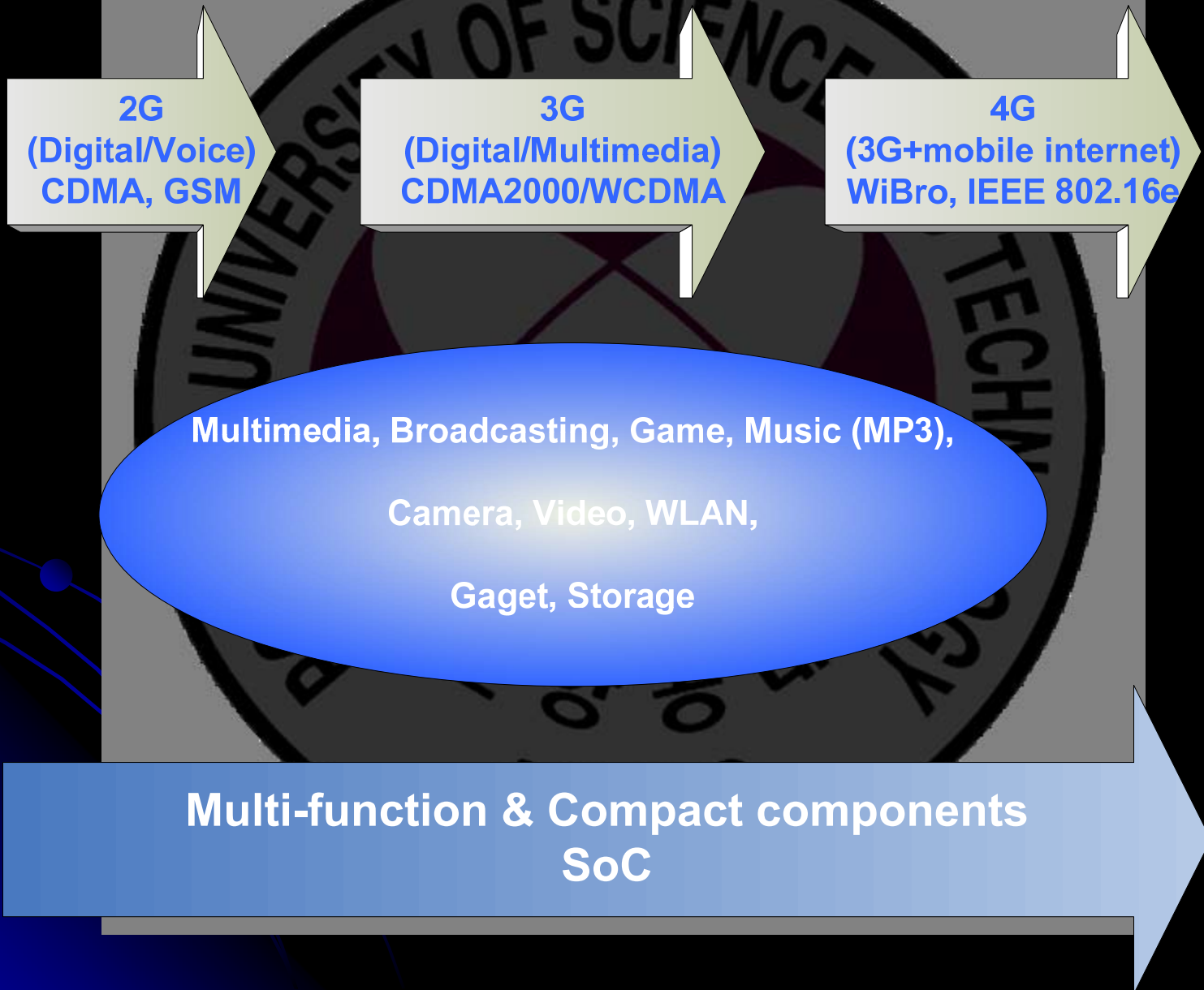
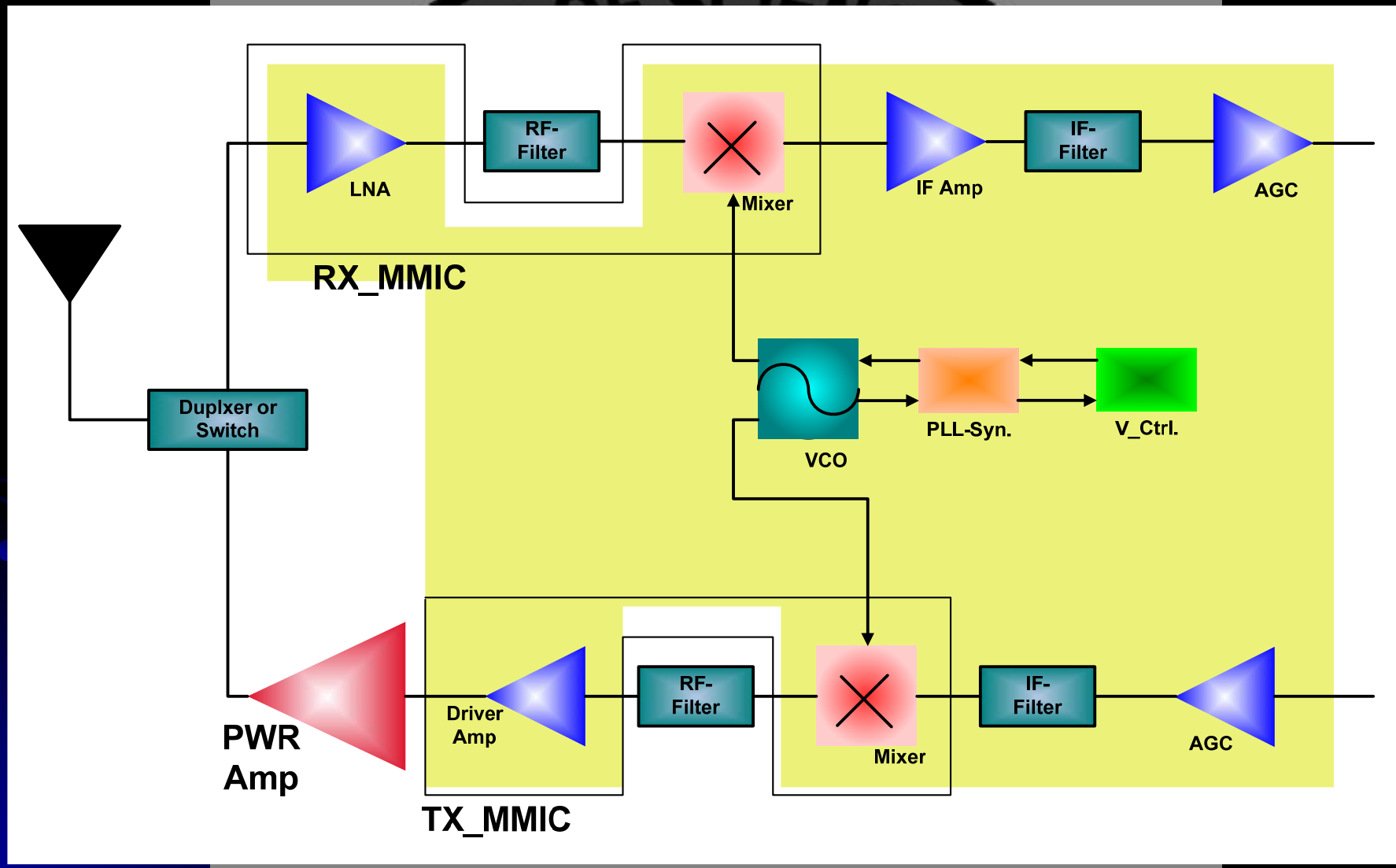
Presentation Outline

- Motivation
- Basic Design Approach
- CMOS PA Linearization
- 3.3 V Operating Single-chip CMOS PA
- Lumped Doherty CMOS PA
- Conclusions

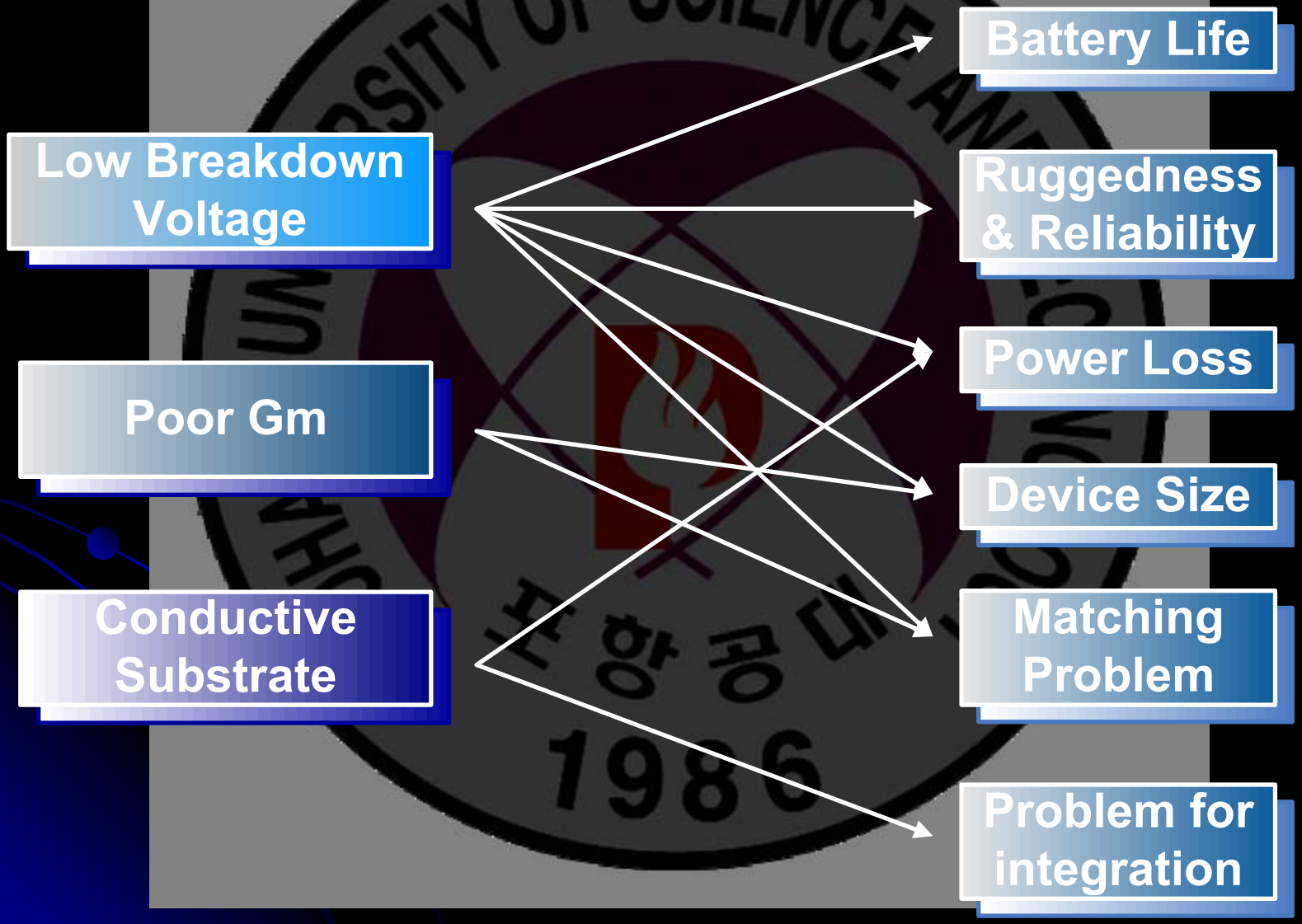
Motivation


2G
(Digital/Voice)
CDMA, GSM
3G
(Digital/Multimedia)
CDMA2000/WCDMA
4G
(3G+mobile internet)
WiBro, IEEE 802.16e
Multimedia, Broadcasting, Game, Music (MP3),
Camera, Video, WLAN,
Gaget, Storage
Multi-function & Compact components
SoC

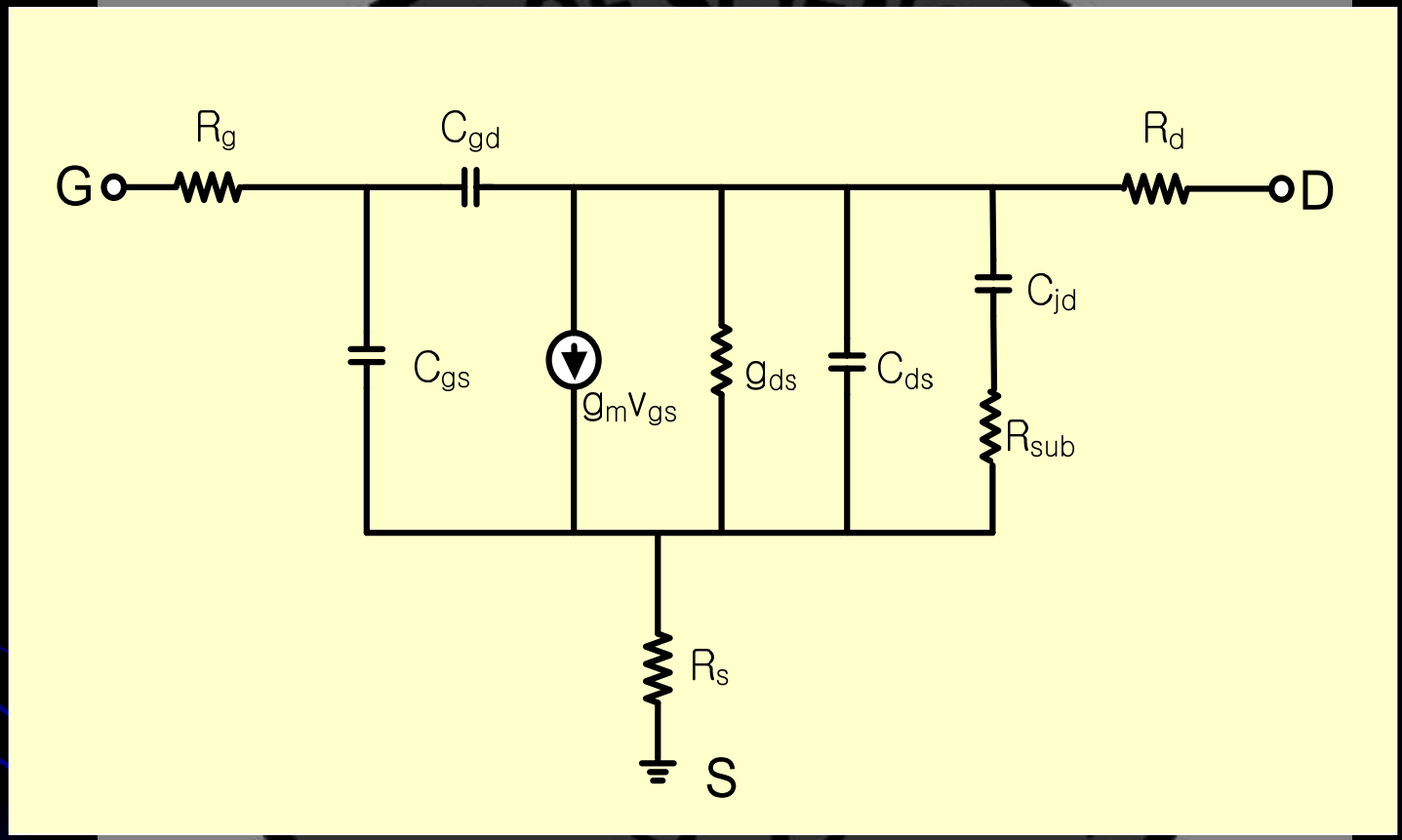
Motivation


LNA
RF-
Filter
Mixer
IF Amp
IF-
Filter
AGC
RX_MMIC
Duplxer or
Switch
VCO
PLL-Syn.
V_Ctrl.
PWR
Amp
Driver
Amp
RF-
Filter
Mixer
IF-
Filter
AGC
TX_MMIC

Challenges for CMOS PA



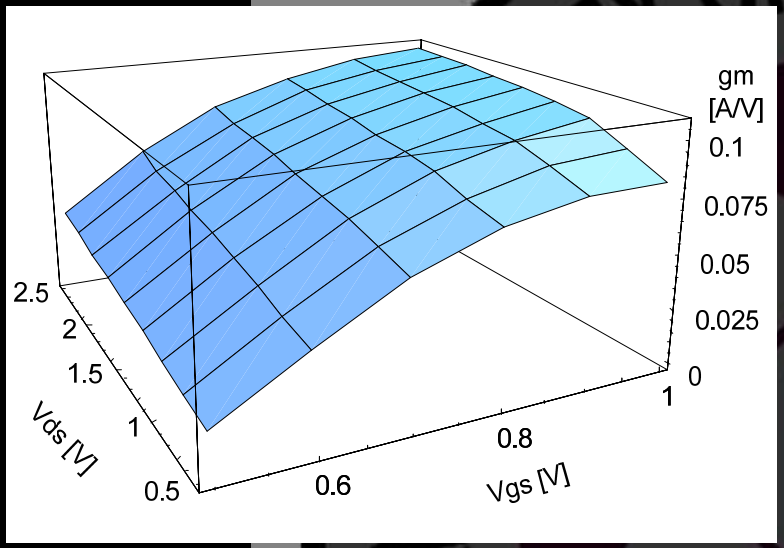
Small-signal equivalent circuit



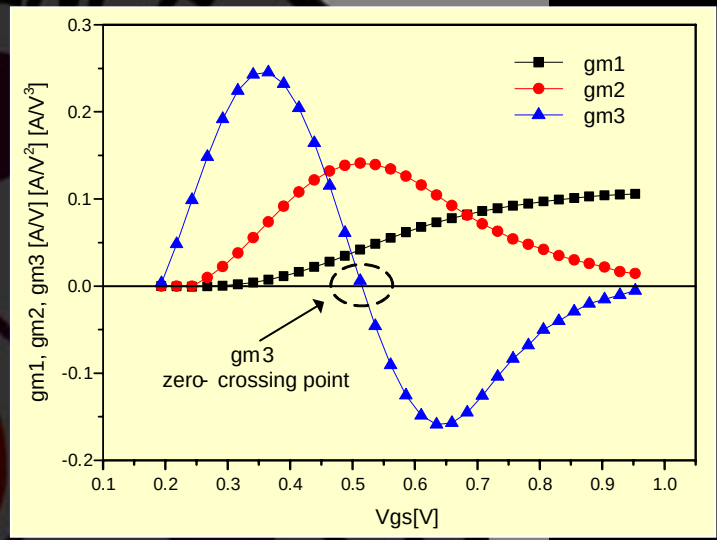
C. E. Biber, M. L. Schmatz, T. Morf, U. Lott, and W. Bächtold, *"A nonlinear microwave MOSFET model for SPICE simulators," IEEE Trans. Microwave Theory and Techn.*, Vol. 46, No. 5, pp. 604-610, May 1998.

Nonlinear Transconductance (g_m)

- **dominant nonlinear source at normal operation**



[Extracted g_m]



[Nonlinear expansion coefficients for g_m]

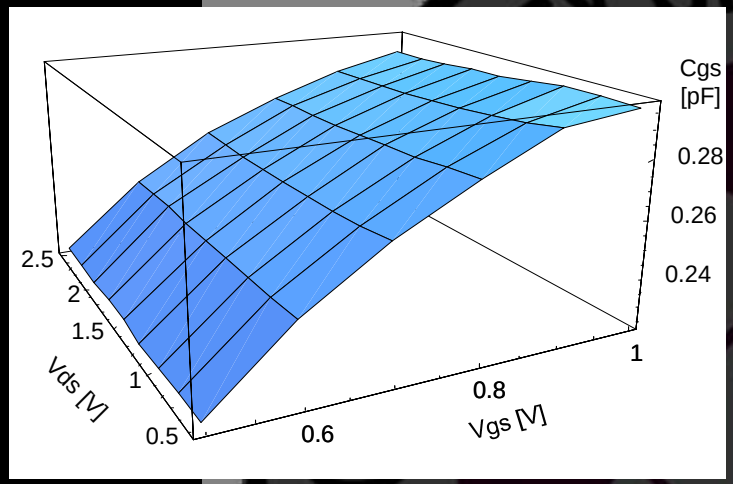
$$i_{trans} = g_{m1}v_{gs} + g_{m2}v_{gs}^2 + g_{m3}v_{gs}^3$$

$$i_{trans,2\omega_2} = \frac{1}{2}g_{m2}v_{gs,\omega_2}^2$$

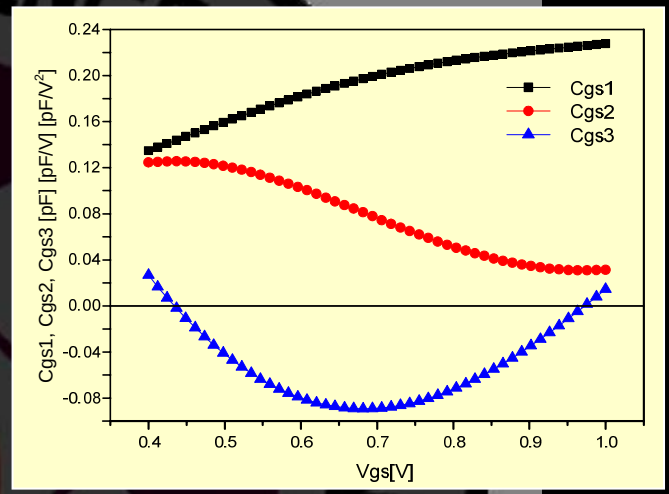
$$i_{trans,2\omega_2-\omega_1} = \frac{3}{4}g_{m3}v_{gs,\omega_2}^2 v_{gs,\omega_1}^*$$

Nonlinear gate-source capacitance (C_{gs})

- **the dominant nonlinear source for a class AB PA**



[Extracted C_{gs}]



[Nonlinear expansion coefficients for C_{gs}]

$$C_{gs} = C_{gs1} + C_{gs2} v_{gs} + C_{gs3} v_{gs}^2$$

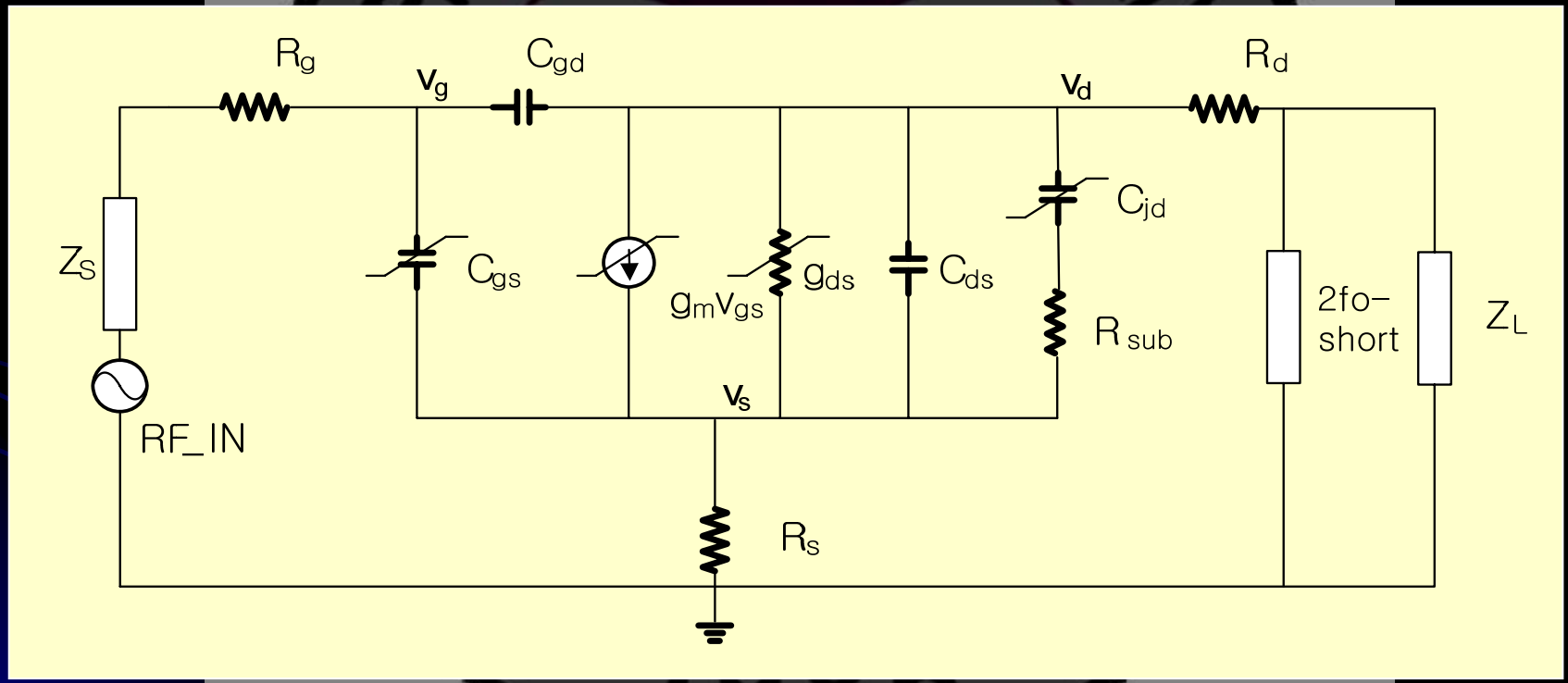
$$i_{Cgs,\omega_2-\omega_1} = j(\omega_2 - \omega_1) C_{gs2} v_{gs,\omega_2} v_{gs,\omega_1}^*$$

$$i_{Cgs,2\omega_2} = j\omega_2 C_{gs2} v_{gs,\omega_2}^2$$

$$i_{Cgs,3\omega_2} = \frac{3}{4} j\omega_2 C_{gs3} v_{gs,\omega_2}^3$$

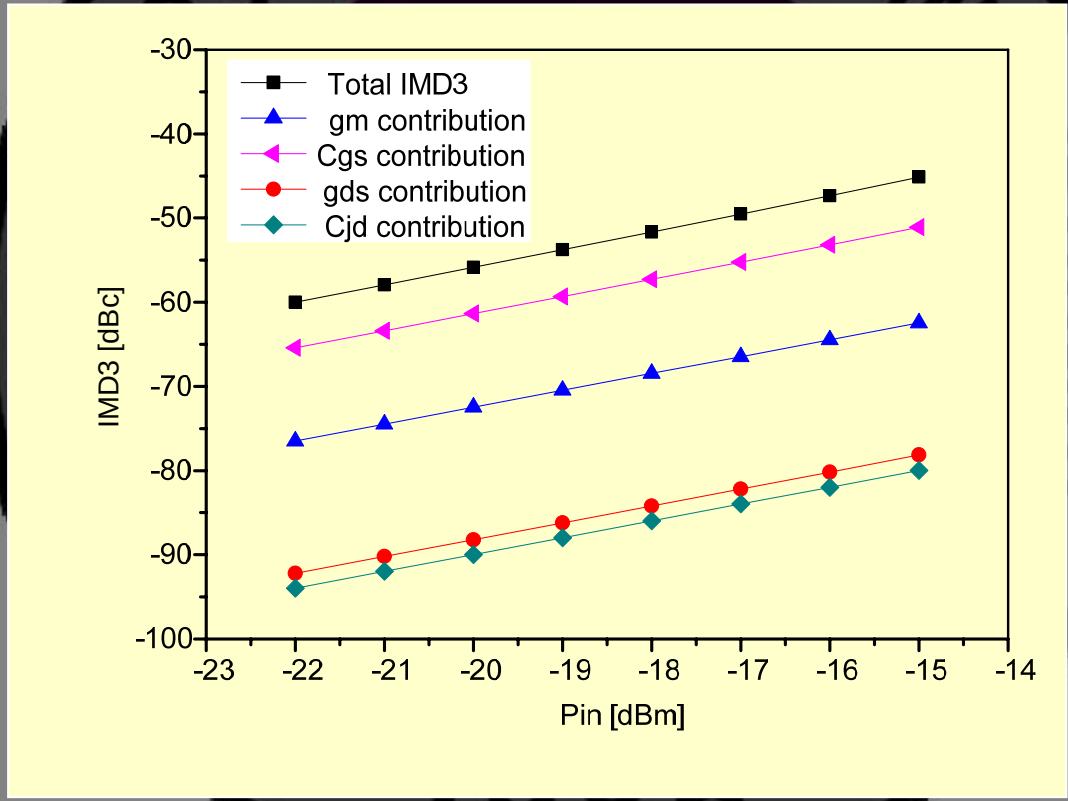
$$i_{Cgs,2\omega_2-\omega_1} = j(2\omega_2 - \omega_1)\frac{3}{4} C_{gs3} v_{gs,\omega_2}^2 v_{gs,\omega_1}^* + j(2\omega_2 - \omega_1) C_{gs2}\left[v_{gs,2\omega_2} v_{gs,\omega_1}^* + v_{gs,\omega_2} v_{gs,\omega_2-\omega_1}^*\right]$$

Analysis of PA linearity using Volterra Series



Harmonic balance simulation of Volterra series

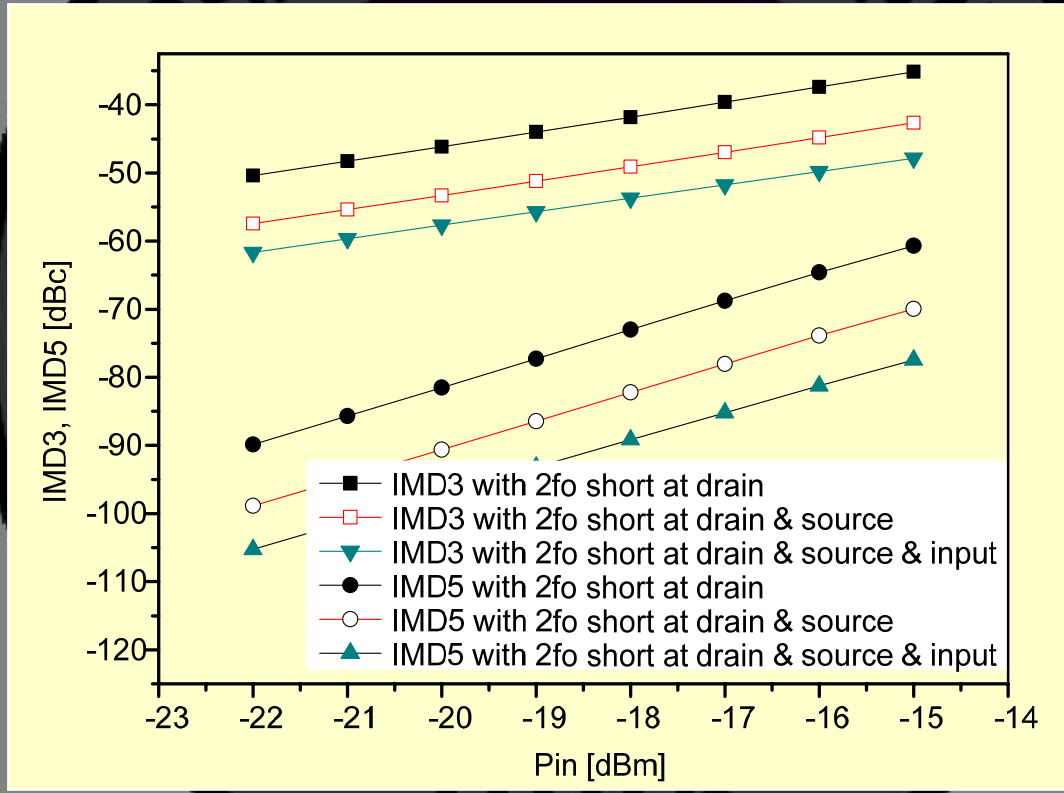
- 2nd harmonic termination at the output & biasing close to g_{m3} zero crossing point



Harmonic distortion from C_{gs} is larger than that from g_m !

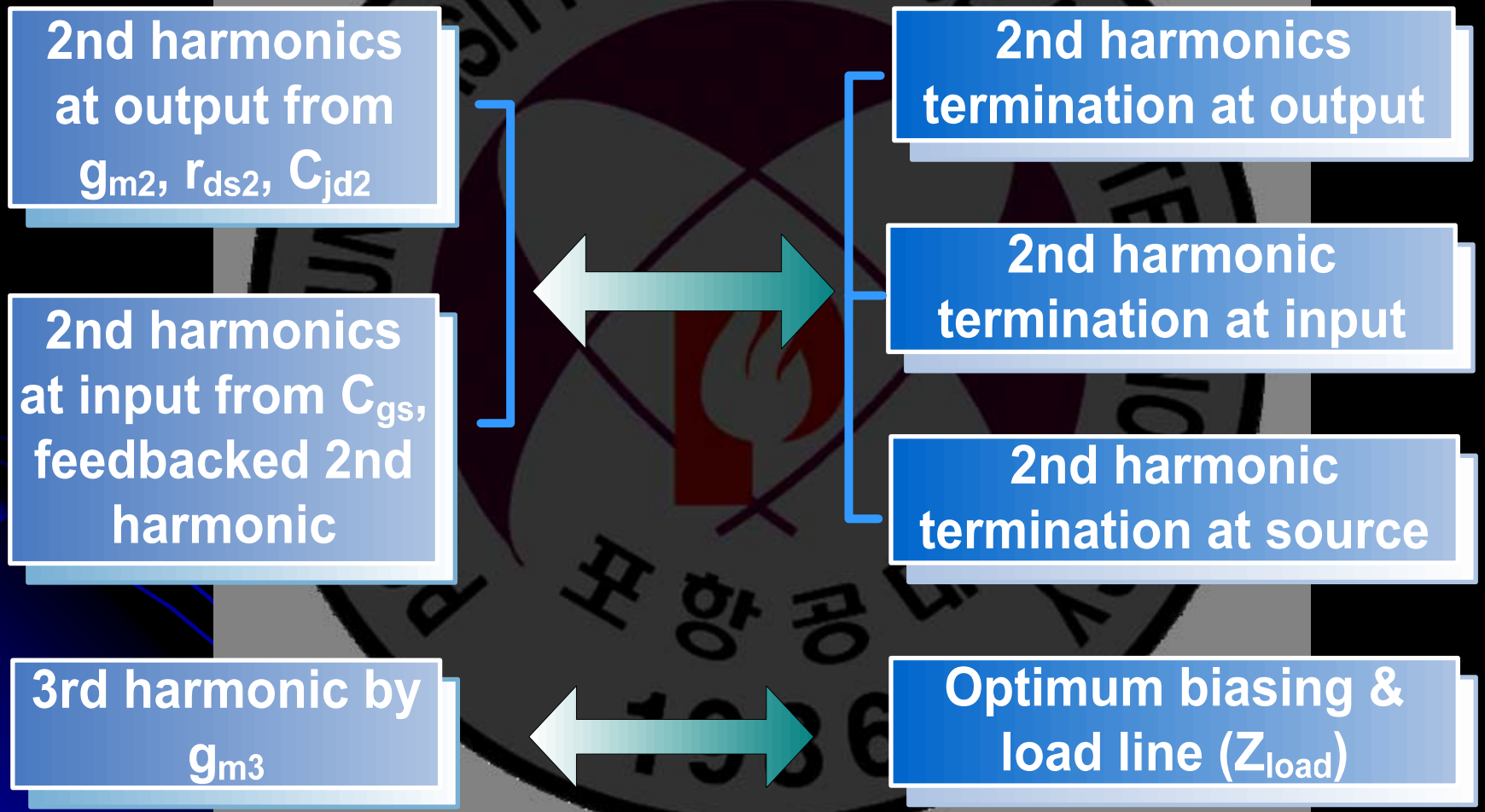
Harmonic balance simulation of Volterra series

- Assuming 0.3 nH of parasitic source inductance for grounding

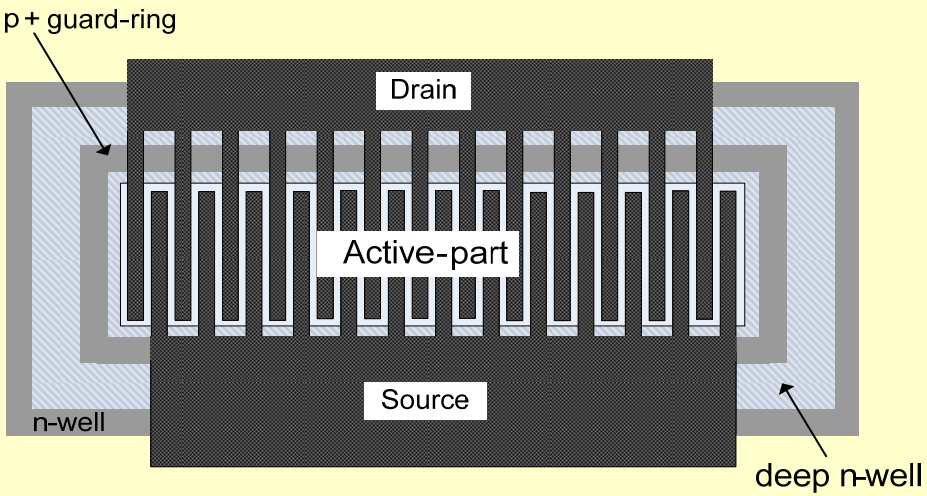


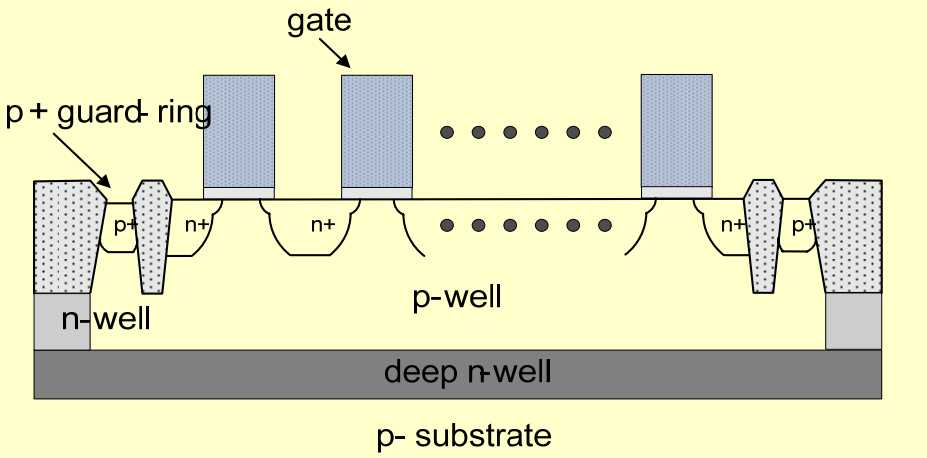
The 2nd harmonic termination at the source suppresses the harmonic distortion at the input and output

Linear CMOS PA Design Approach

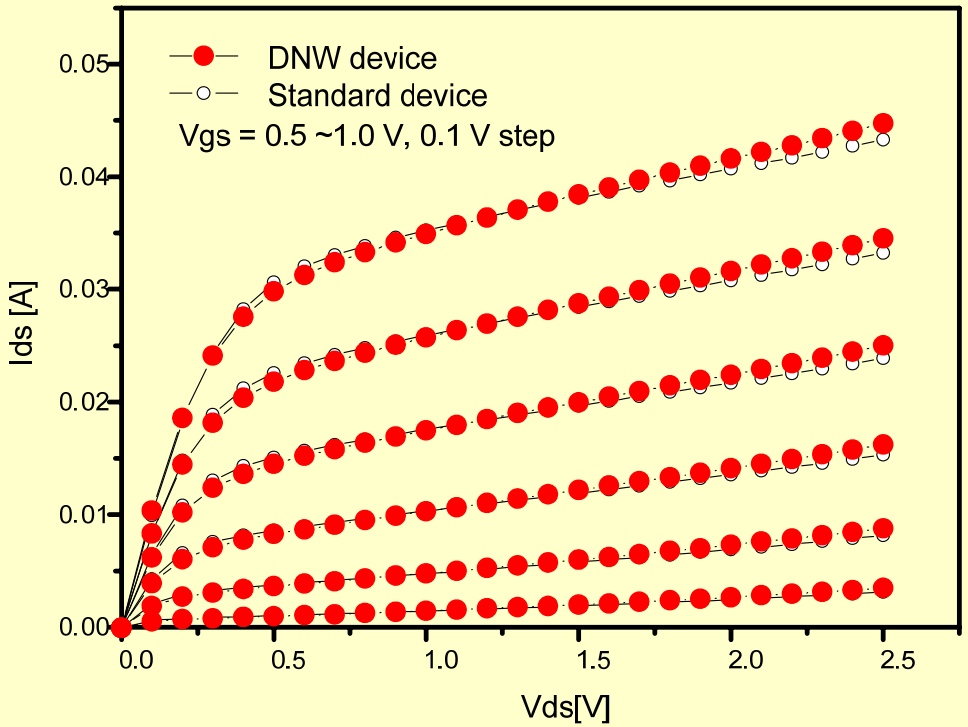


Unit power cell with DNW structure

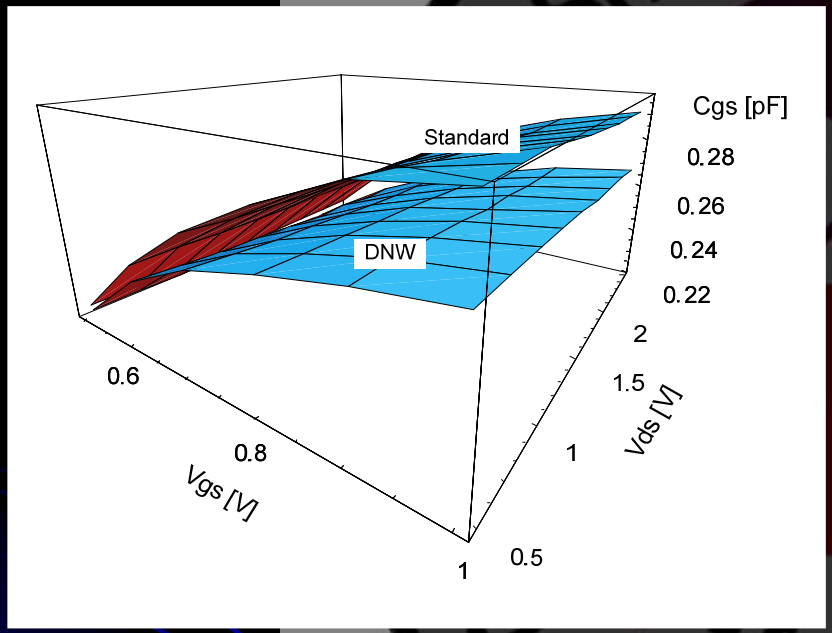




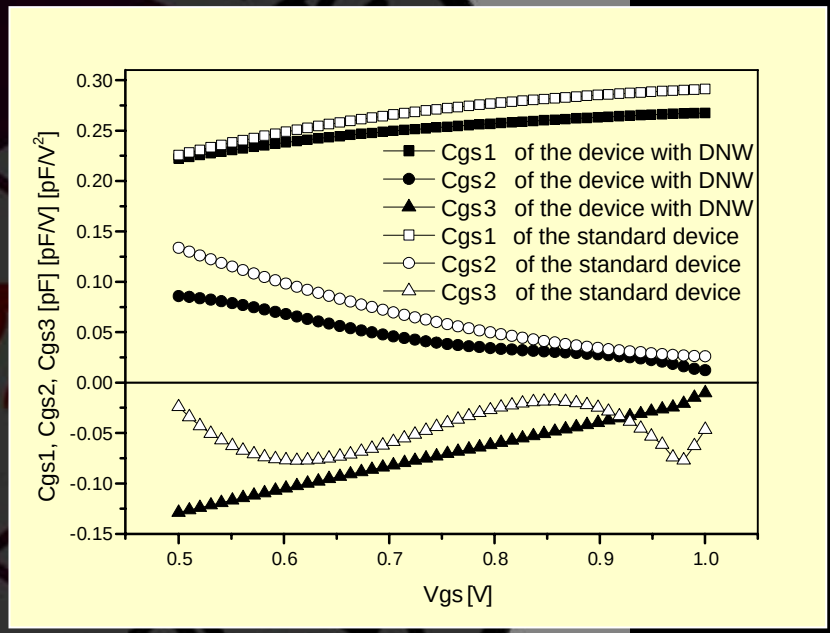
DC_IV Comparisons



Nonlinear gate-source capacitances (C_{gs})



[Extracted C_{gs}]



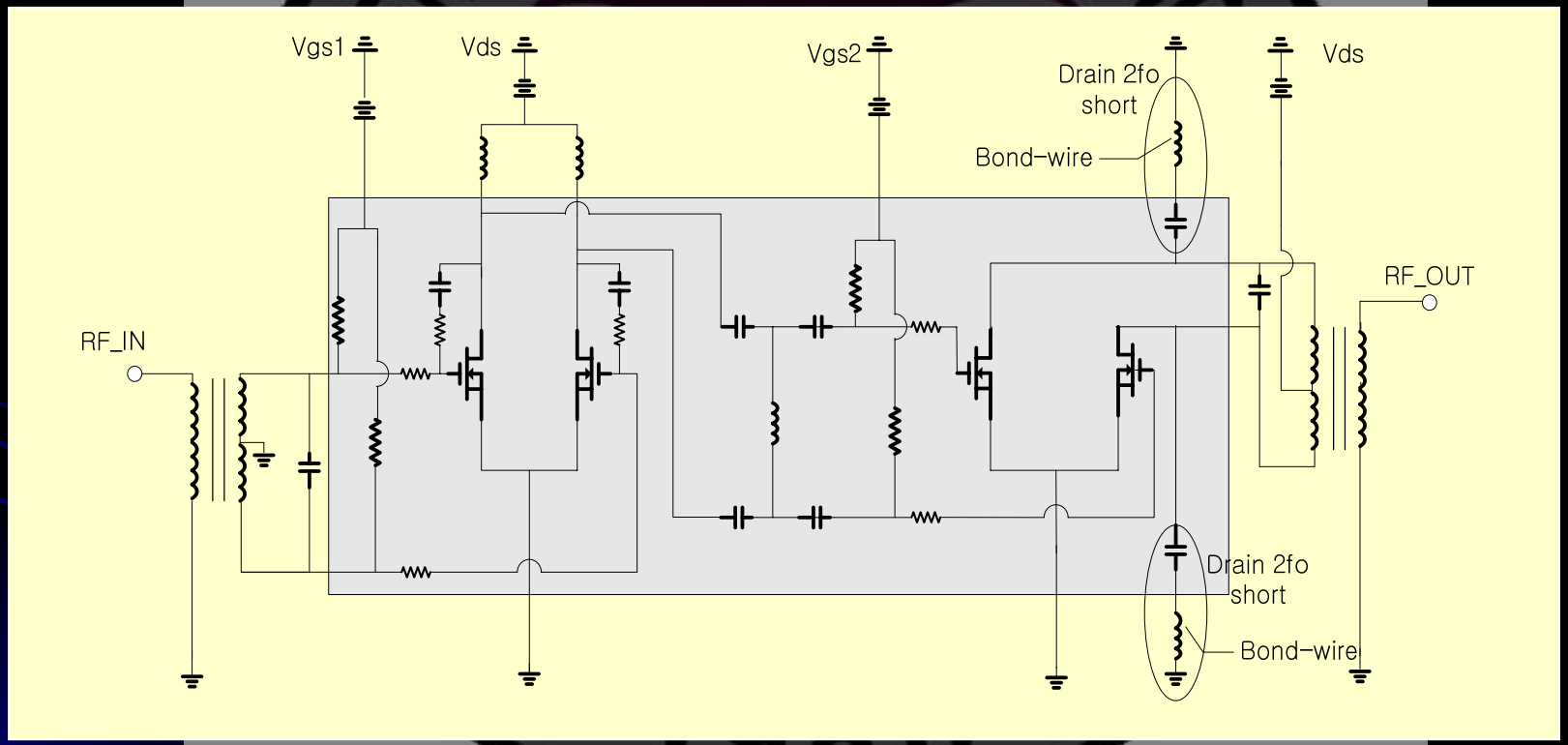
[Nonlinear expansion coefficients for C_{gs}]

J. Su, H. Hsu, S. Wong, C. Chang, T. Huang and J. Y. Sun, "Improving the RF Performance of 0.18 um CMOS With Deep n-Well Implantation," *IEEE Electron Device Letters*, Vol. 22, No. 10, pp. 481-483, Oct 2001.

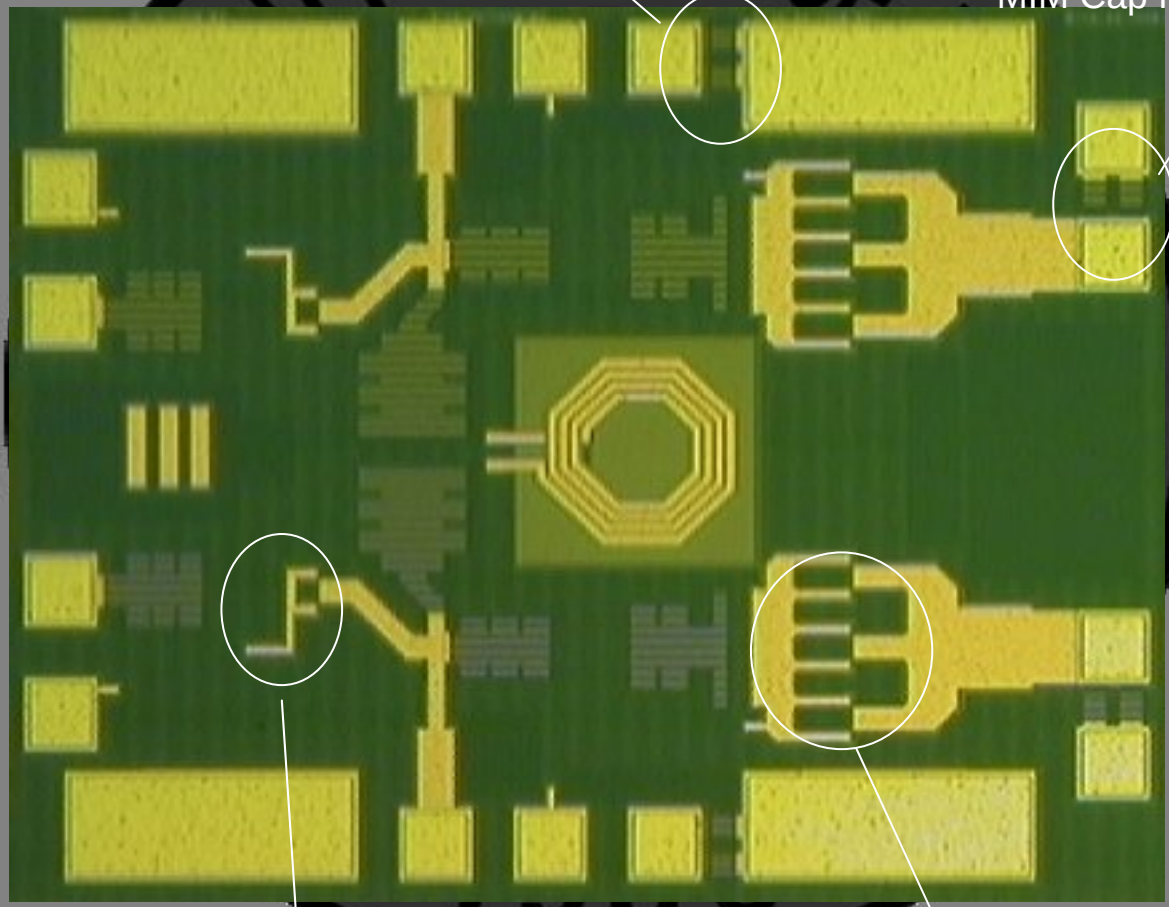
The calculated contributions for IMD3 generation using Volterra series analysis

	Std.	DNW		Std.	DNW
g_m contribution	-56.4 dBc	-54.78 dBc	C_{gs} contribution	-44.6 dBc	-55.9 dBc
r_{ds} contribution	-72 dBc	-68.5 dBc	C_{jd} contribution	-74 dBc	-85.5 dBc
IMD3 of the standard device = -38.1 dBc IMD3 of the device with DNW = -42.1 dBc					
Center Frequency = 2.45 GHz, Tone-spacing = 2 MHz, Pin = -14 dBm					

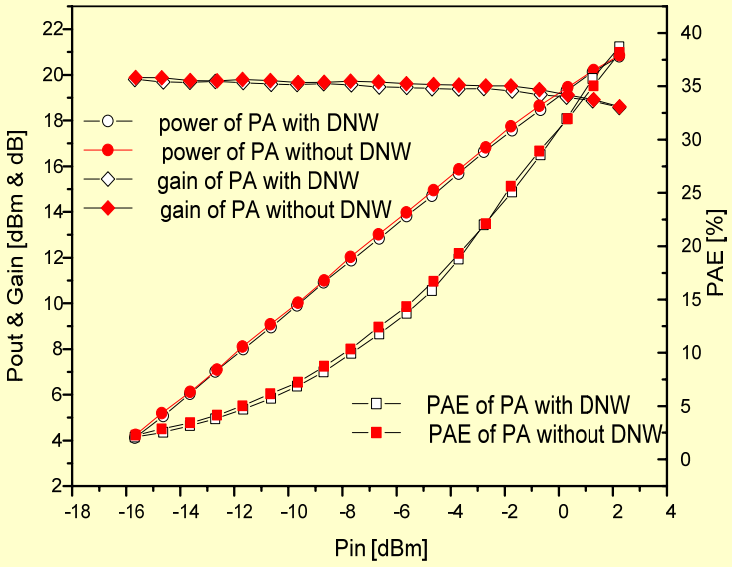
DNW Effects of 0.18 um Balanced CMOS PA

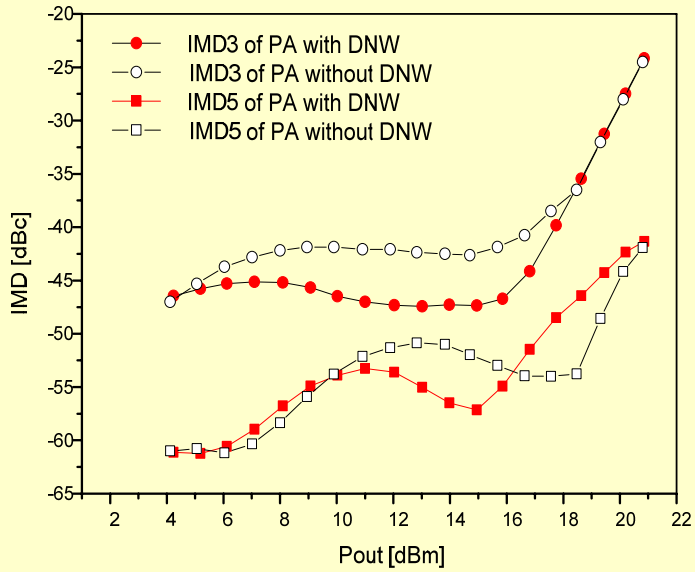


CMOS Chip Photo of Balanced PA

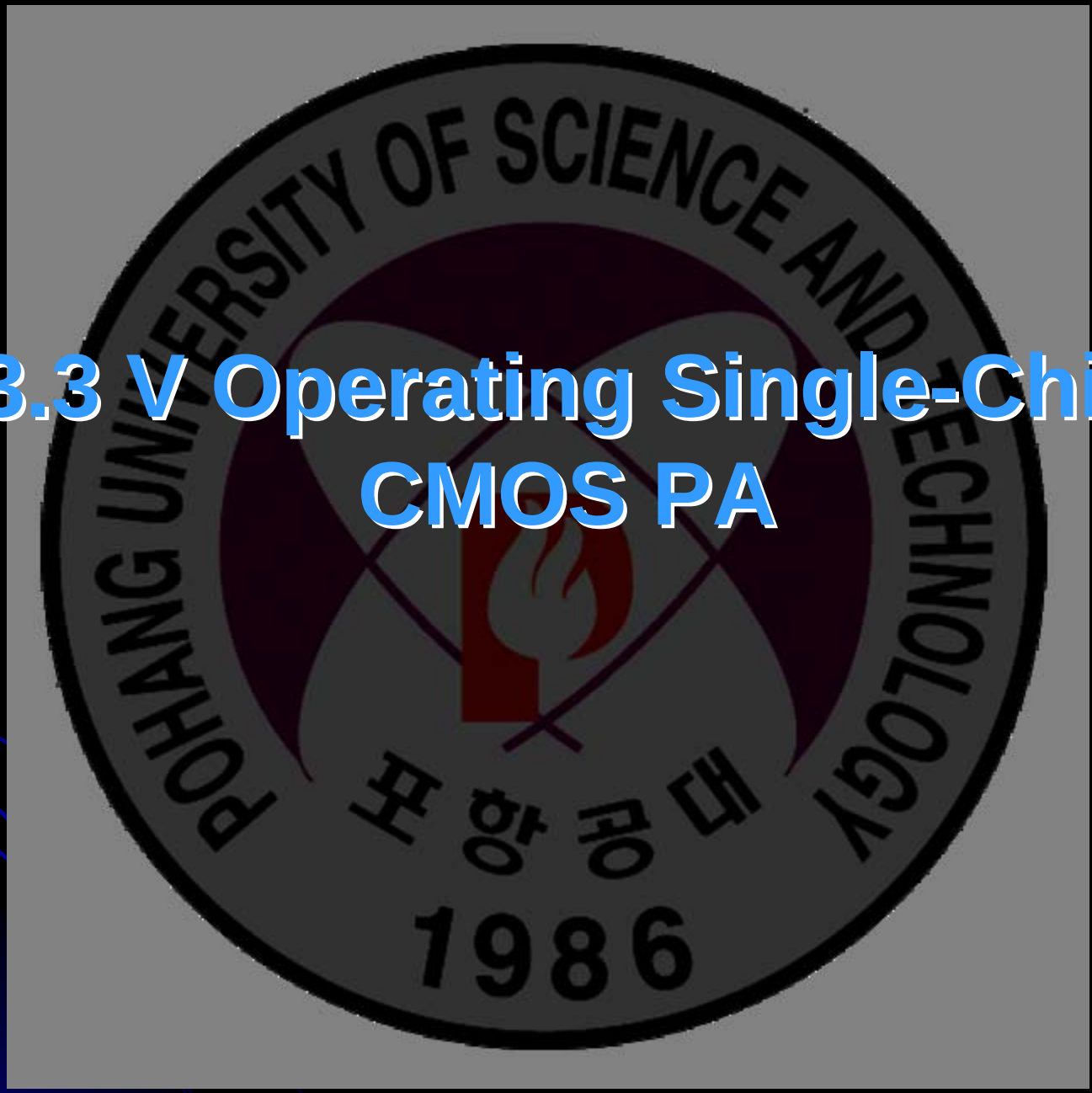


RF performance comparison of the Balanced PA's



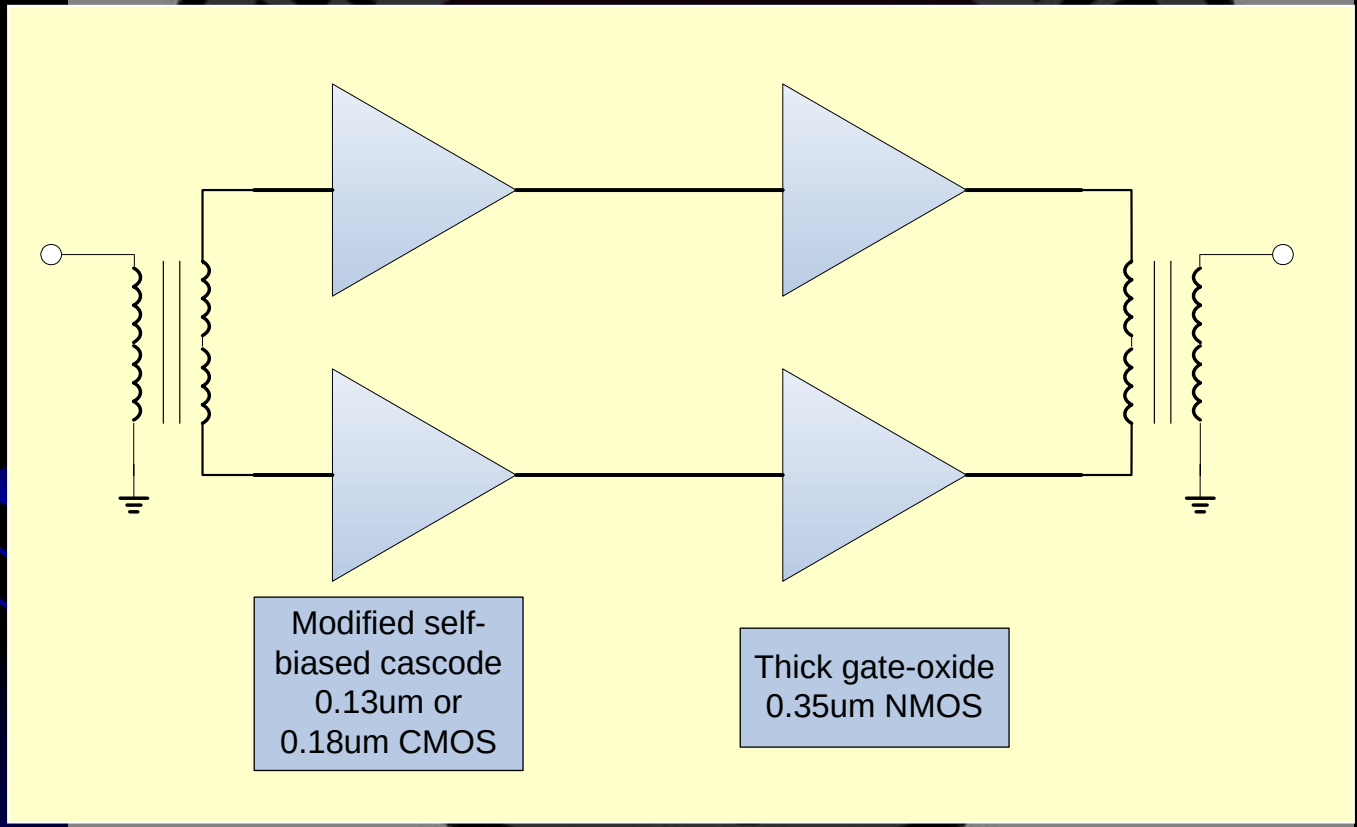


- P_{out} : 20.2 dBm, Gain : 18.7 dB, PAE : 35 % at P_{1dB}
- Linearity maintains under -45 dBc of IMD3 and -57 dBc of IMD5 for an output power backed-off more than 5 dB from P_{1dB}.
- PA with DNW improves the IMD3 and IMD5 about 7dB without disturbing the power performances (P_{out}, PAE)

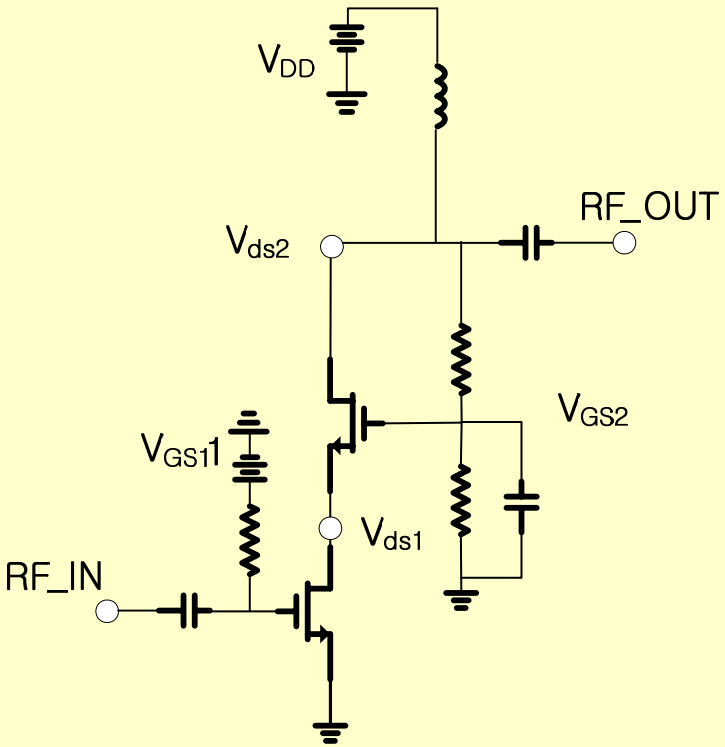


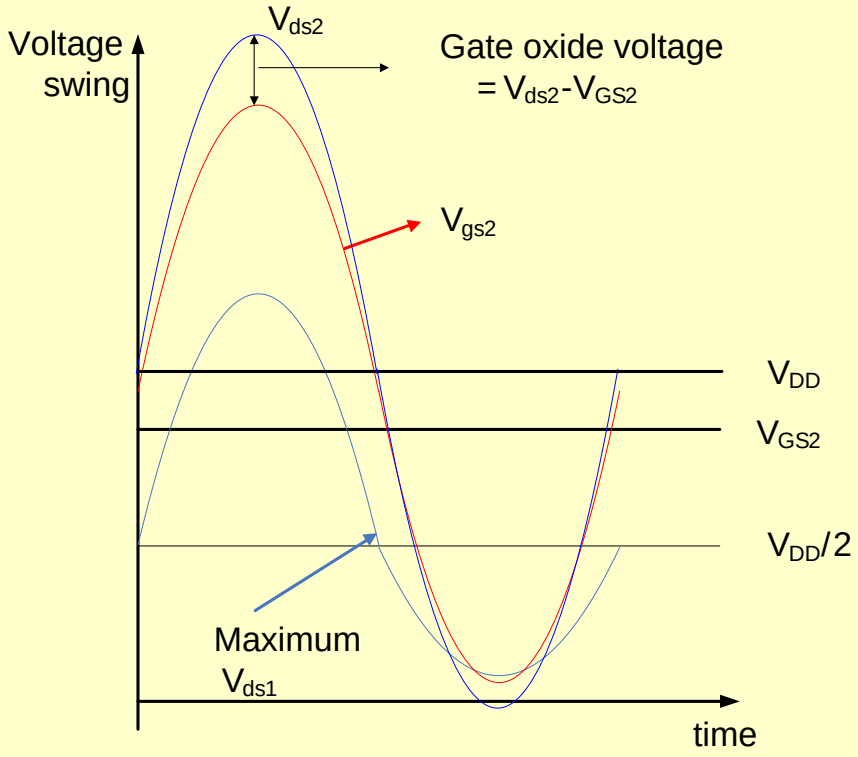
3.3 V Operating Single-Chip CMOS PA

Prototype of 3.3 V operating linear CMOS PA

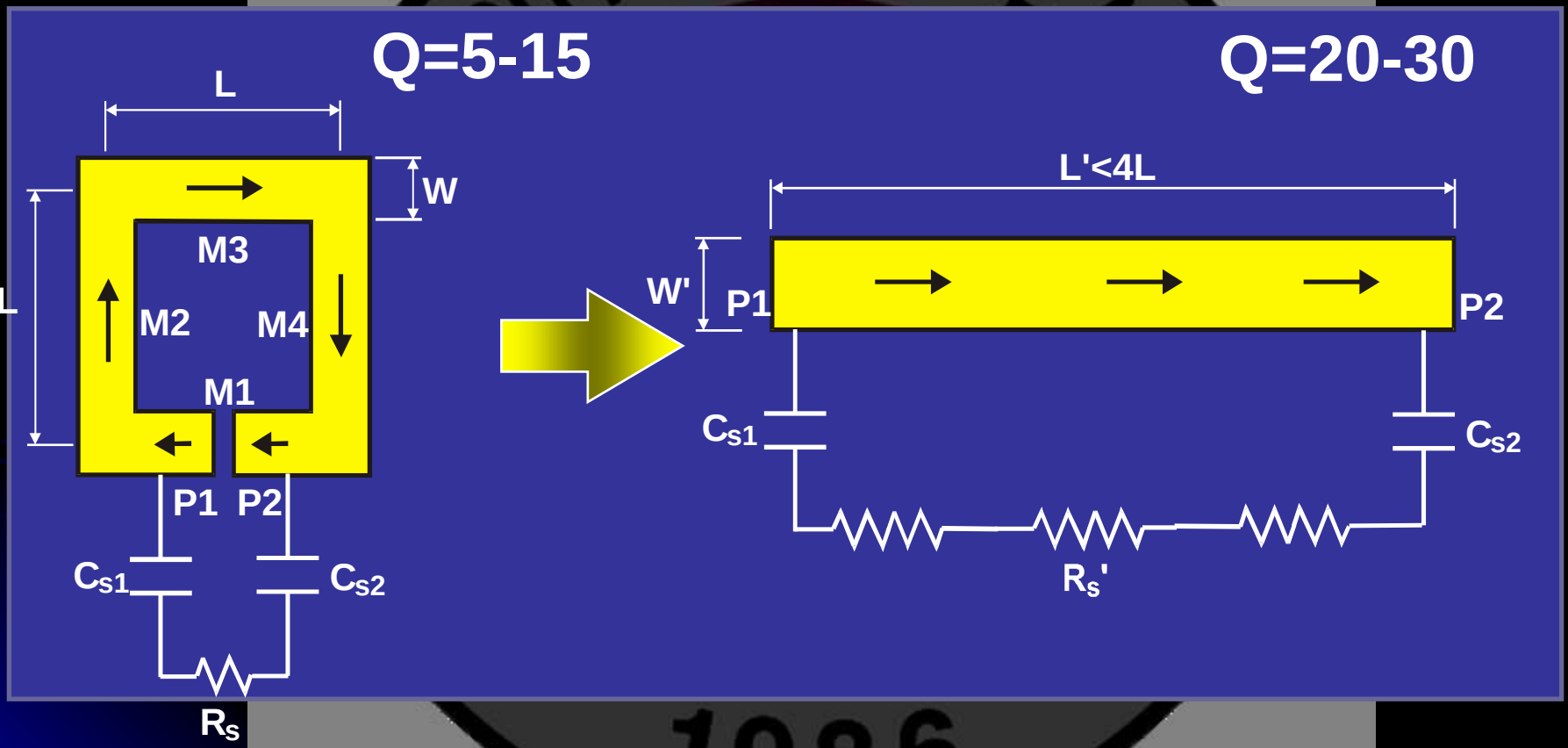


Modified Self-Biased Cascode



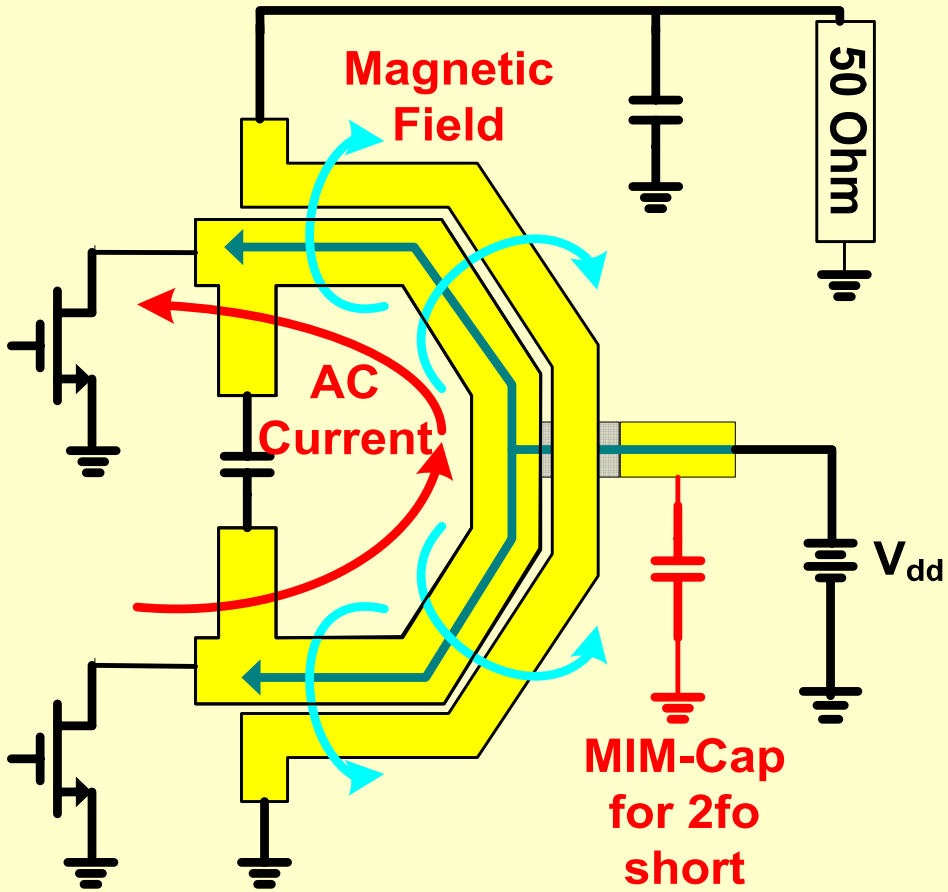


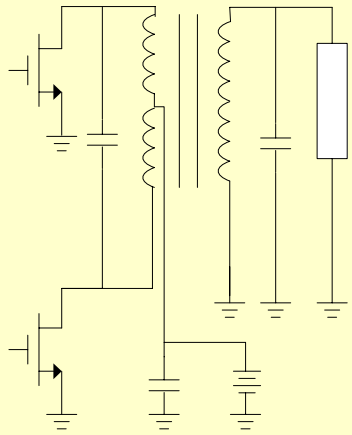
One-turn Inductor vs. Slab Inductor



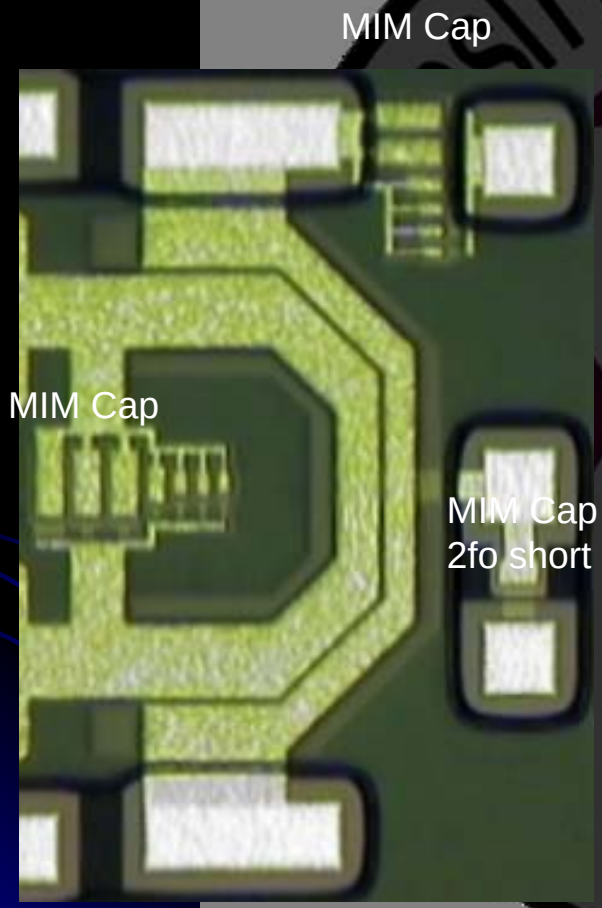
- Slab inductor provides higher Q, thus lower loss

Magnetically Coupled Transformer



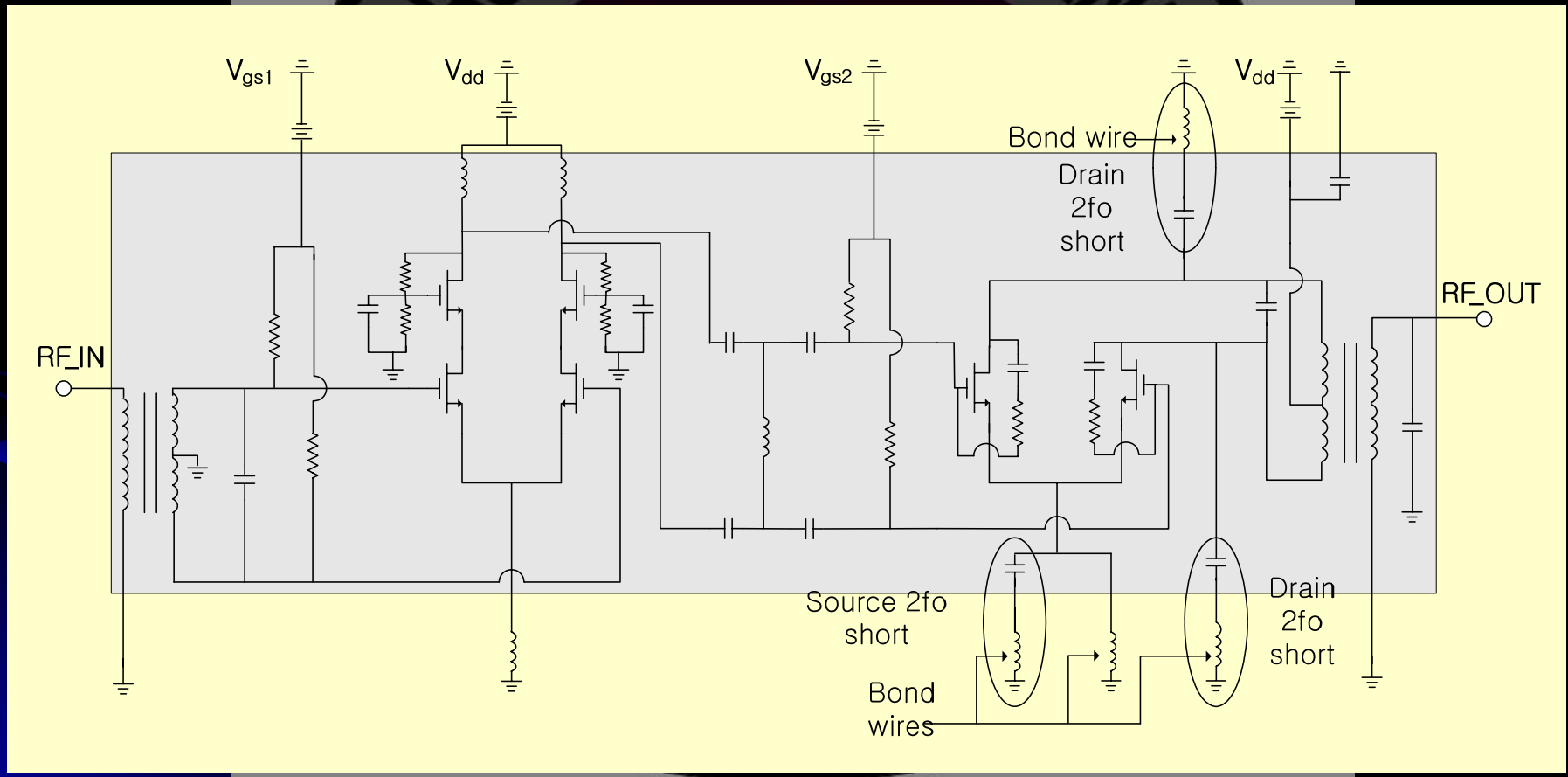


Integrated transformer performance



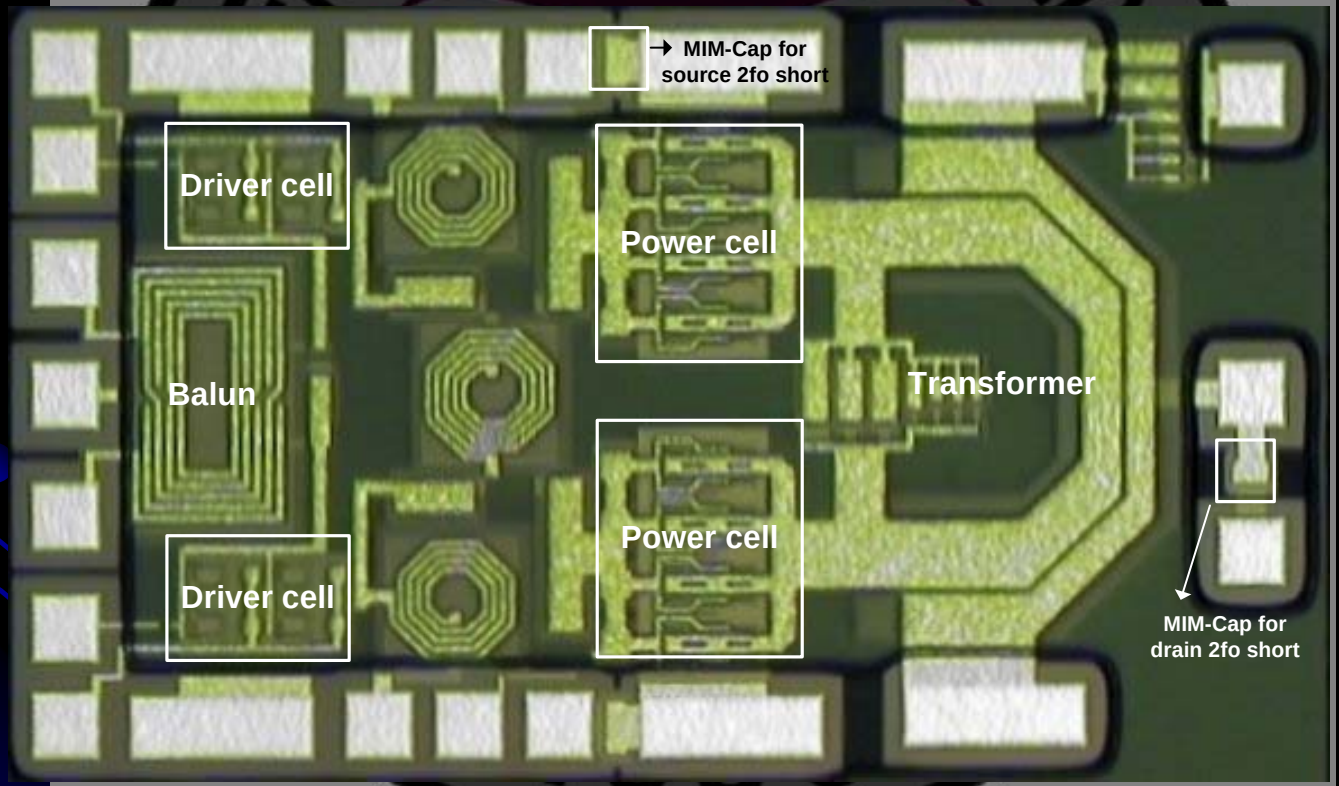
Metal	Cu or Al (3um)
Substrate	Si (15 S/m)
Conductivity	4.7e-7 ~3.4e-7 S/m
Size	600 x 700
Loss	0.5~0.8 dB
PAE	89~80 %
Zout	13 +j*1

3.3 V operating Single-Chip CMOS PA (0.18 um process)

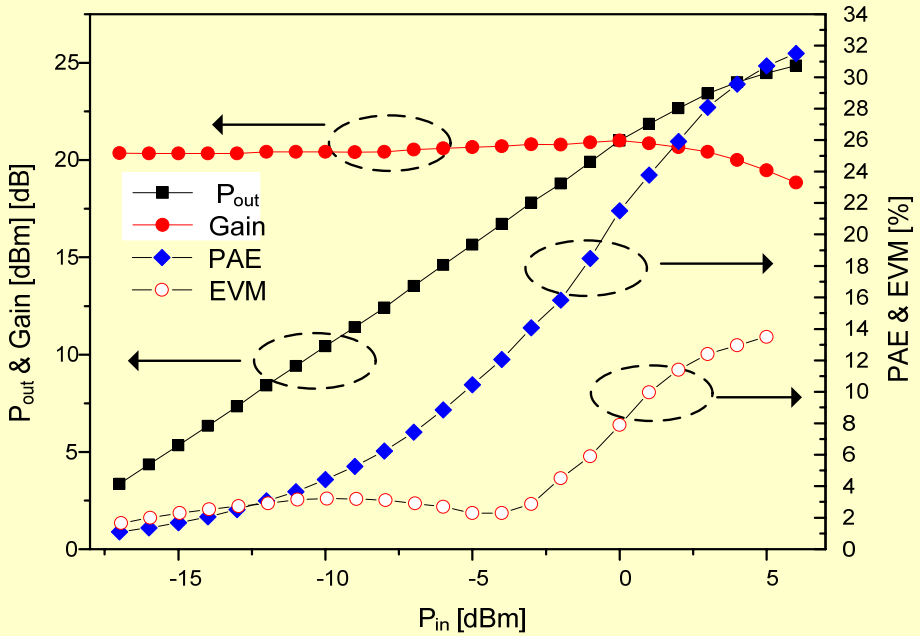


3.3 V operating Single-Chip CMOS PA

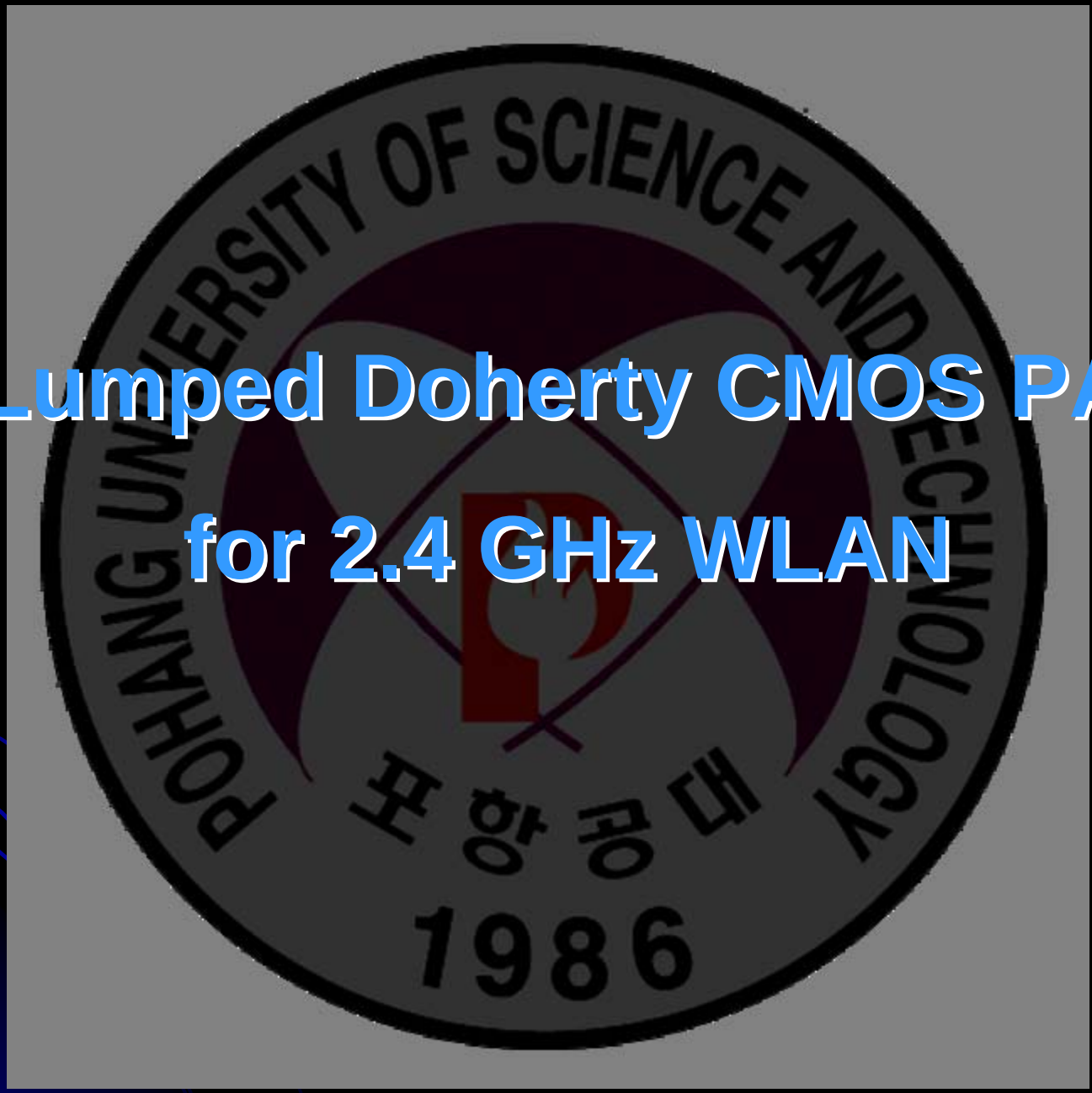
(1 x 1.7 mm²)



RF performance of 3.3 V Operating Single-Chip CMOS PA (2.4 GHz)

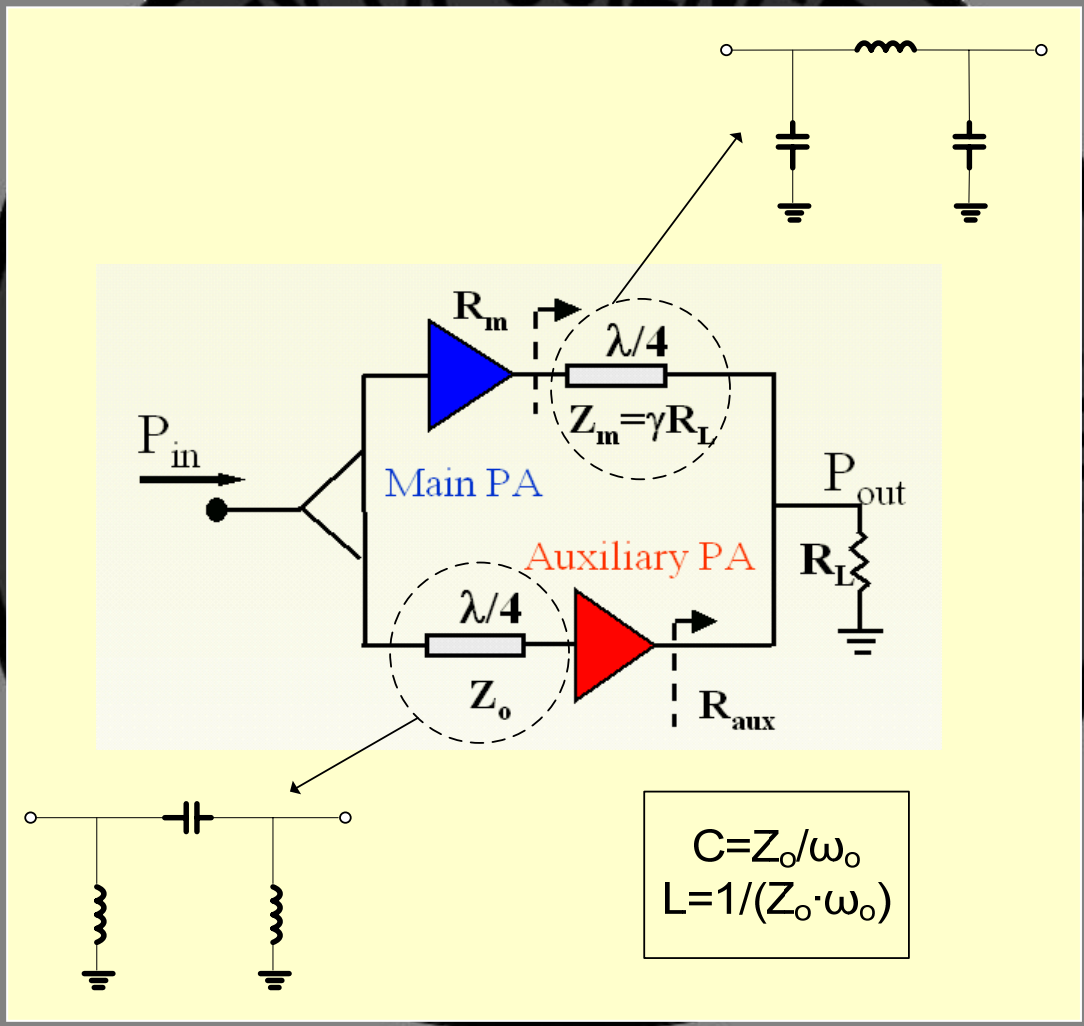


Technology	0.18 um CMOS	
Power Supply	3.3 V	
Frequency	2.4 GHz	
Area	1 x 1.7 mm^2	
RF performances at P_{1dB}	**measured**	
P_{out}	24.5 dBm	
Power gain	19.8 dB	
PAE	31 %	
OFDM signal Test	**54 Mbps/64 QAM**	
EVM	4.5 %	3 %
Average power	18.8 dBm	17.9 dBm
PAE	15.8 %	14 %

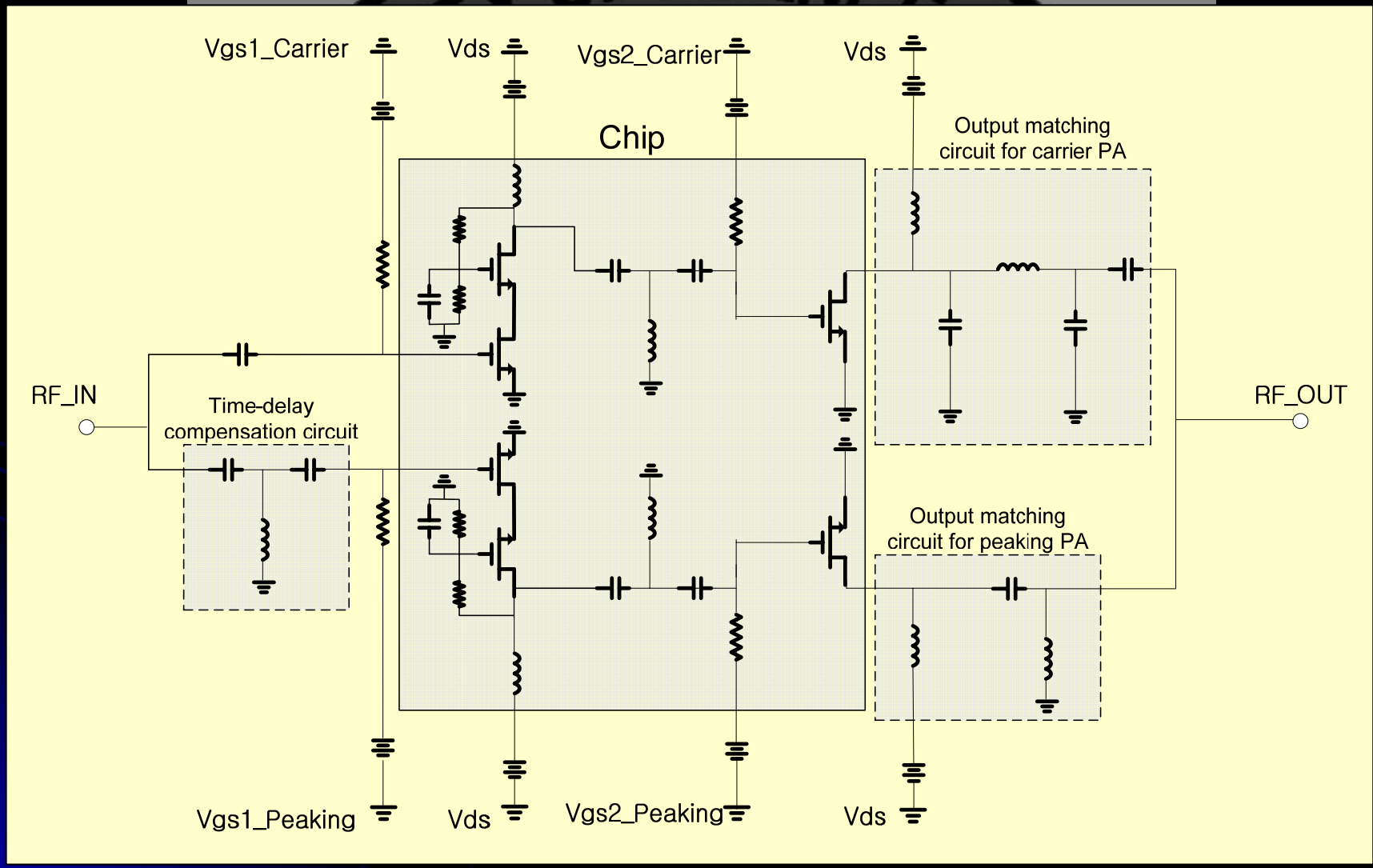


Lumped Doherty CMOS PA for 2.4 GHz WLAN

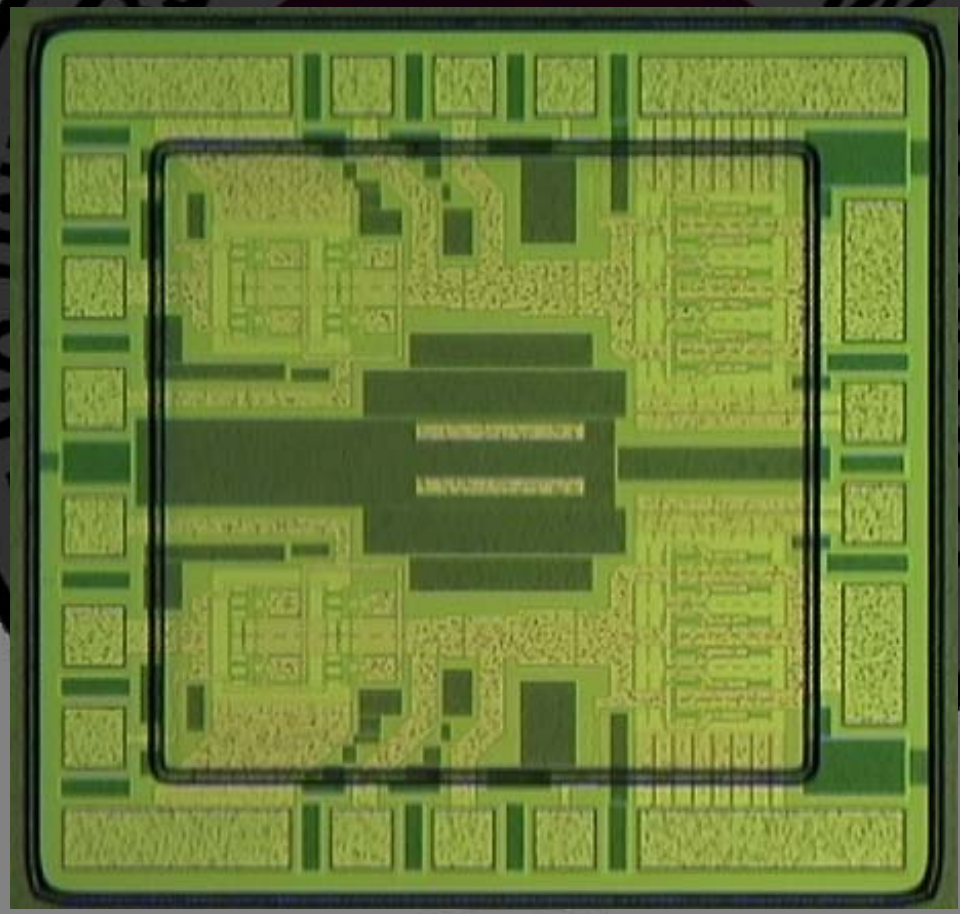
Lumped Doherty Conversion Concept



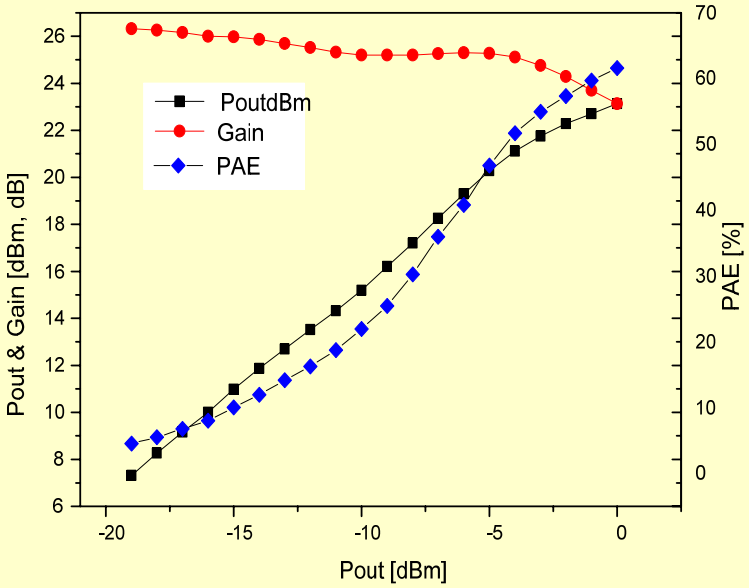
Prototype of 2-Stage Lumped Doherty Circuit

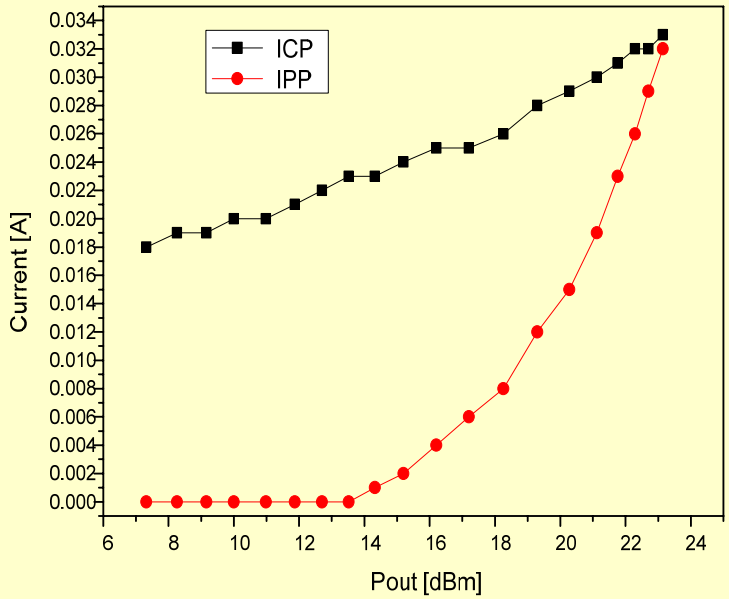


Example of 3.2 V operating Doherty CMOS PA (1 x 1 mm²)



RF performance of 3.2 V Operating Lumped Doherty CMOS PA





P_{1dB} = 22.7 dBm
PAE = 60 % at P_{1dB}
PAE = 35 % at P_{5dB}

Comparison of Measured Results

Design	Technology (um)	Gain [dB]	$Pout_{max}$ [dBm]	PAE [%] @			
				$Pout_{max}$	P_{1dB}	Back-off	
						4 dB	8 dB
Ballweber	0.6	5	19	30	26	14	6
Giry	0.35	24.6	23.5	35	24	13	6
Sowlati	0.18	36	23	42	18	8	4
Ding	0.18	12	22	44	36	18	8
This work	0.13	↑ 23	↑ 23.2	↑ 62	60	38	20

Conclusions

- Basic design approach and linearization methods for CMOS PA are established.
- 3.3 V operation single-chip CMOS PA
  - A circuit prototype for a linear CMOS PA with high voltage operation is proposed.
  - The integrated transformer is a prominent solution for a balanced single-chip PA with low loss.
- Lumped Doherty CMOS PA
  - Proposed first-step for the fully integrated CMOS Doherty PA.
  - Demonstrated good performances of CMOS PA comparable to GaAs based PA