Modeling of Devices for Power Amplifier Applications

David E. Root
Masaya Iwamoto
John Wood

Contributions from

Jonathan Scott
Alex Cognata

Agilent Worldwide Process and Technology Centers
Santa Rosa, CA USA

Agilent Technologies

Presentation Outline

- Introduction
- Nonlinear Charge Modeling
- Electro-Thermal Modeling
- Advanced Measurements
- Mathematical CAD Techniques
- Summary & Conclusions

Power Amplifier Requirements and Modeling Implications

Linearity: Harmonic and Intermodulation Distortion; ACPR; AM-AM; AM-PM

Efficiency: PAE; Fundamental Output Power; Self-biasing

Modeling Challenges from device physics (III-V transport), complex signals, multiple time-scale dynamics, and the wide variety of device designs in many material systems

Accuracy over bias, frequency, and temperature; power

Perspective for this talk:

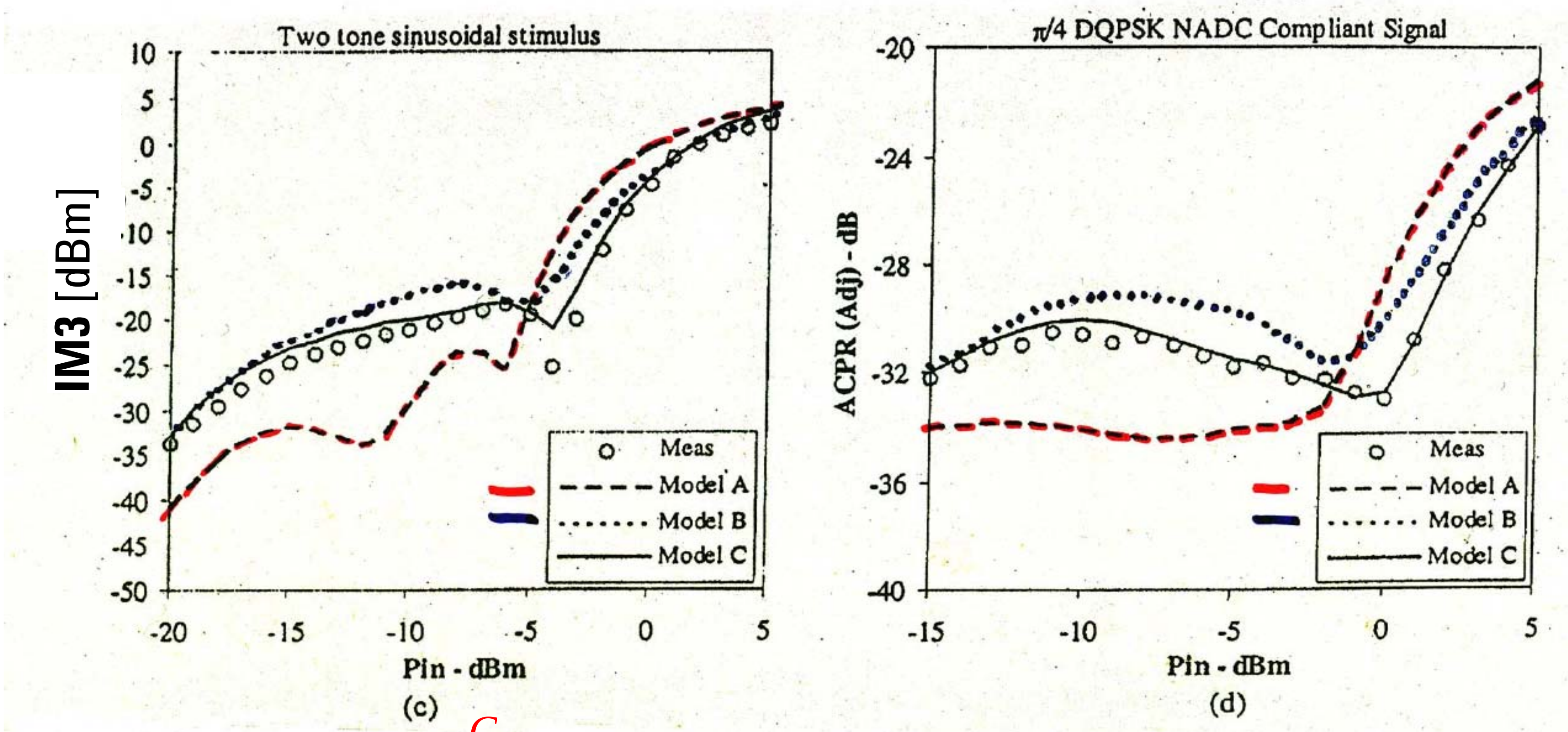
- **Modeling of III-V HBTs & HEMTs for circuit simulation**
- **Primarily from CAD perspective**

Presentation Outline

- Introduction
- Nonlinear Charge Modeling
- Electro-Thermal Modeling
- Advanced Measurements
- Mathematical CAD Techniques
- Summary & Conclusions

Nonlinear Charge Modeling: MOTIVATION

FET models with same I-V eq.s but different charge eq.s [2]



Model A = $\dfrac{C_{j0}}{\sqrt{1-V/\phi}}$

Model B = Modified Statz Model (1987)

Model C = "Agilent (HP) FET Model" (1991) = $\oint_{Contour} \vec{C} \cdot d\vec{V}$

Charge model is critical for distortion simulation

Charge Modeling Problem for Circuit Simulation

Specify two (e.g. Gate and Drain)
charge functions, Q_i, $i=G,D$ such that:

$$I_i(t) = I_i(V_{GS}(t), V_{DS}(t)) + \frac{dQ_i(V_{GS}(t), V_{DS}(t))}{dt}$$

Can calculate charge function from physics (in theory) [6].

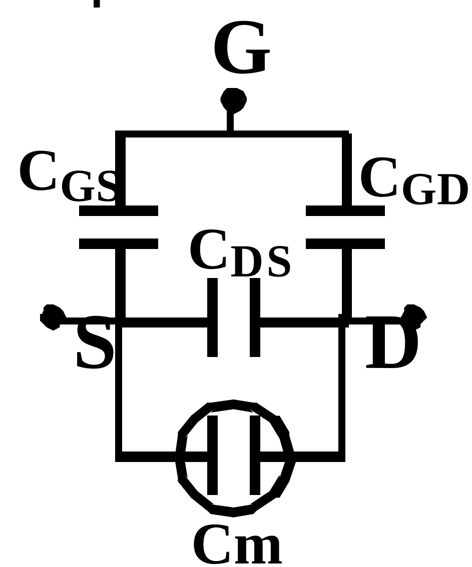
<u>"Inverse modeling" alternative (not just table-based):</u>

Relate model functions to small-signal data and equivalent ckt.

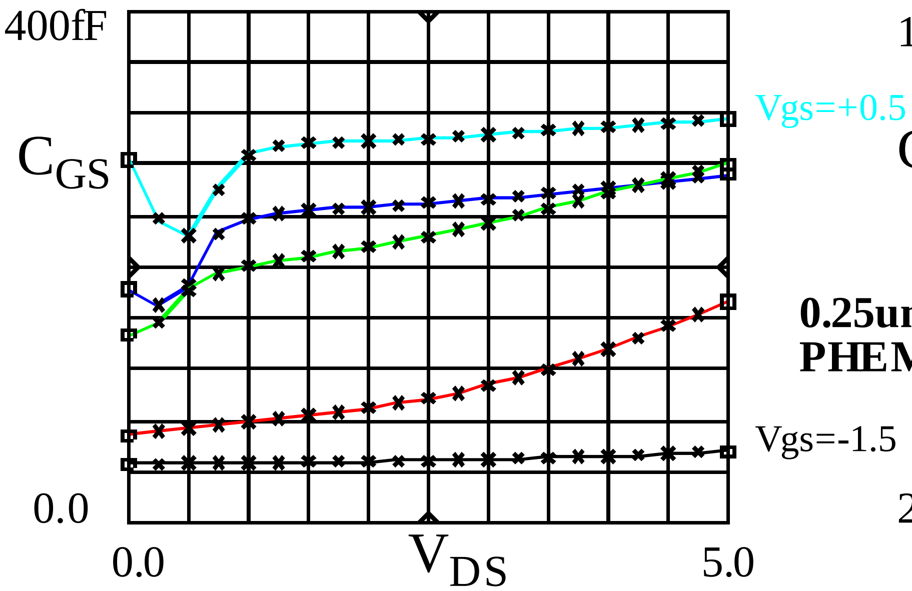
data

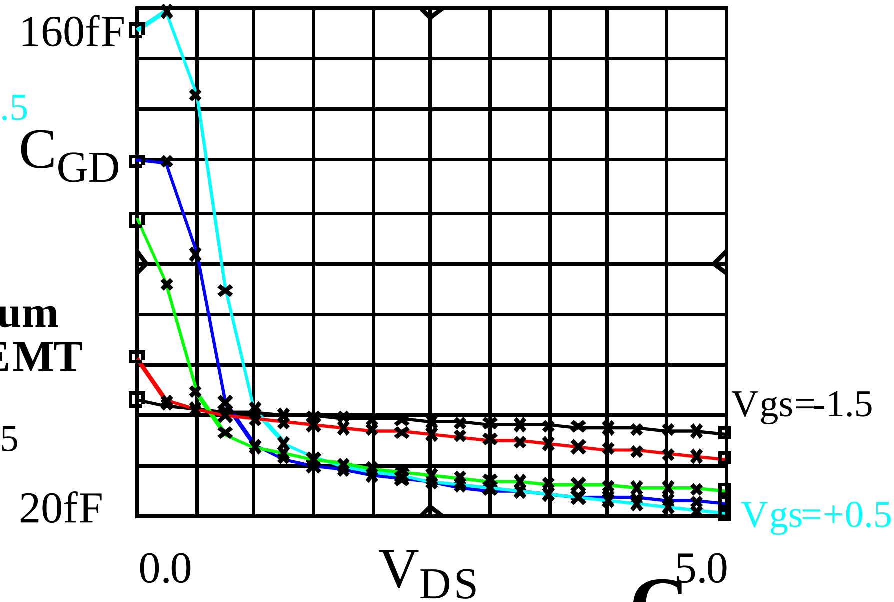
$$\frac{\mathrm{Im}(Y_{\mathrm{int}})}{\omega} = \begin{bmatrix} \frac{\partial Q_G}{\partial V_{GS}} & \frac{\partial Q_G}{\partial V_{DS}} \\ \frac{\partial Q_D}{\partial V_{GS}} & \frac{\partial Q_D}{\partial V_{DS}} \end{bmatrix} = \begin{bmatrix} C_{GS} + C_{GD} & -C_{GD} \\ C_m - C_{GD} & C_{DS} + C_{GD} \end{bmatrix}$$

Derivatives of model function



Measured Bias-Dependent FET Gate Capacitances

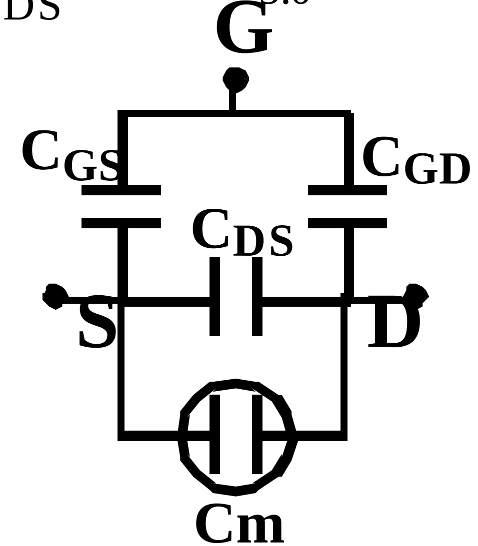




0.25um PHEMT

The measured data cannot be modeled by two, two-terminal nonlinear capacitors

A *single* Q_G function must model *both* C_{GS} and C_{GD}



A model Q_G function consistent w. SS data exists if and only if

(1) $$\frac{\partial(C_{GS}^{meas} + C_{GD}^{meas})}{\partial V_{DS}} = \frac{-\partial C_{GD}^{meas}}{\partial V_{GS}}$$ (D. Root *2001 ISCAS Short Course*)

This is a *constraint* on

pairs of independently measured Y– parameters (or S-parameters)
pairs of "measured" device capacitances (attached to gate node)

This is the modeling principle of *Terminal Charge Conservation*

The prescription for model charge calculation is, then:

(2) $$Q_G^{\text{model}} = \oint_{contour} [(C_{GS}^{meas} + C_{GD}^{meas})dV_{GS} - C_{GD}^{meas} dV_{DS}]$$

Similar conditions to (1) and (2) can be written at the drain

Measured FET data are very consistent with (1) at gate
Somewhat less consistent at drain

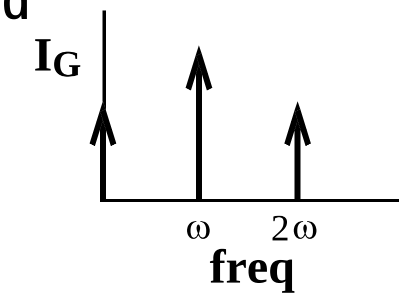
Why not use independently measured capacitances?

$$I_G(t) = I_G(V_{GS}(t), V_{DS}(t)) +$$

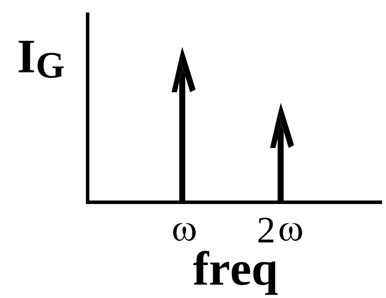
$$C_{GS}^{meas}(V_{GS}(t), V_{DS}(t))\frac{dV_{GS}(t)}{dt} + C_{GD}^{meas}(V_{GS}(t), V_{DS}(t))\frac{dV_{GD}(t)}{dt}$$

This model will fit bias-dependent capacitances perfectly
BUT: It can be shown the capacitance terms yield
a spectrum with a *DC component!*

Root RAWCON98



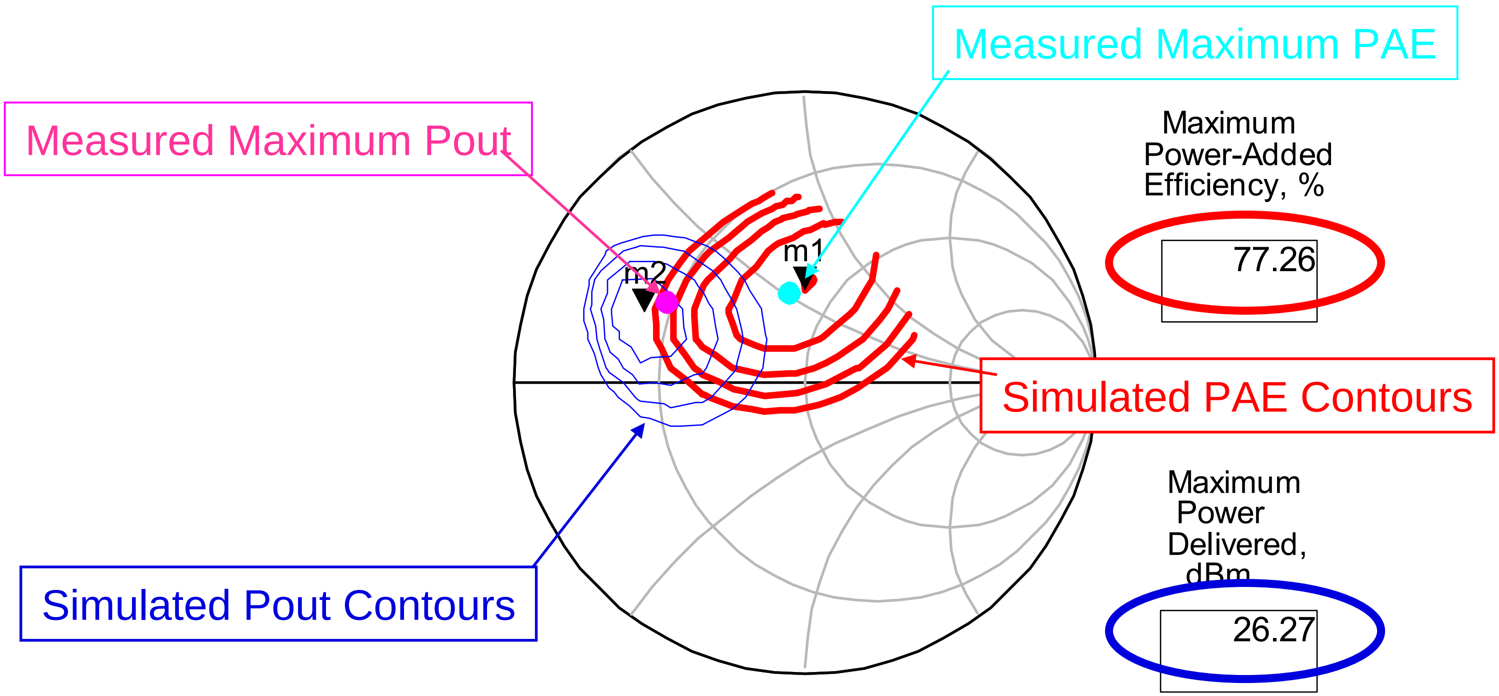
Terminal Charge Conserving capacitances
do not produce a DC component



Enforcing Terminal Charge Conservation
is a *modeling trade-off*. It is *not* physical charge cons. (KCL)

Example: EPHEMT Large-Signal Model [24]

Analytic I-V, table-based charge and gate current, + self-heating



Simulated EPHEMT Load-Pull contours for Pmax & PAE.

Max PAE: 77.26% meas. 77.16% simulated.

Max Power: 26.26 dBm measured and simulated

Terminal Charge Conservation and III-V HBT Modeling [4]

Intrinsic common-emitter HBT Y-parameters are of the form:

$$\frac{\mathrm{Im}(Y_{\mathrm{int}})}{\omega} = \begin{bmatrix} \frac{\partial Q_{BB}}{\partial V_{BE}} & \frac{\partial Q_{BB}}{\partial V_{CE}} \\ \frac{\partial Q_{CC}}{\partial V_{BE}} & \frac{\partial Q_{CC}}{\partial V_{CE}} \end{bmatrix} = \begin{bmatrix} \frac{\partial Q_{BB}}{\partial V_{BC}} + \frac{\partial Q_{BB}}{\partial I_C} g_m & -\frac{\partial Q_{BB}}{\partial V_{BC}} + \frac{\partial Q_{BB}}{\partial I_C} g_{CE} \\ \frac{\partial Q_{CC}}{\partial V_{BC}} + \frac{\partial Q_{CC}}{\partial I_C} g_m & -\frac{\partial Q_{CC}}{\partial V_{BC}} + \frac{\partial Q_{CC}}{\partial I_C} g_{CE} \end{bmatrix} = \begin{bmatrix} \tilde{C}_B + \tilde{\tau}_B \cdot g_m & -\tilde{C}_B + \tilde{\tau}_B \cdot g_{CE} \\ \tilde{C}_C + \tilde{\tau}_C \cdot g_m & -\tilde{C}_C + \tilde{\tau}_C \cdot g_{CE} \end{bmatrix}$$

Where: $\tilde{\tau}_C = \frac{\partial Q_{CC}}{\partial I_C} = \frac{\mathrm{Im}(Y_{21} + Y_{22})}{\omega\left(g_m + g_{CE}\right)}$ $\qquad \tilde{C}_C = \frac{\partial Q_{CC}}{\partial V_{BC}} = \frac{\mathrm{Im}(Y_{21})}{\omega} - \tilde{\tau}_C \cdot g_m$

Necessary and Sufficient Conditions
For model Q_{CC} consistent with ss data:

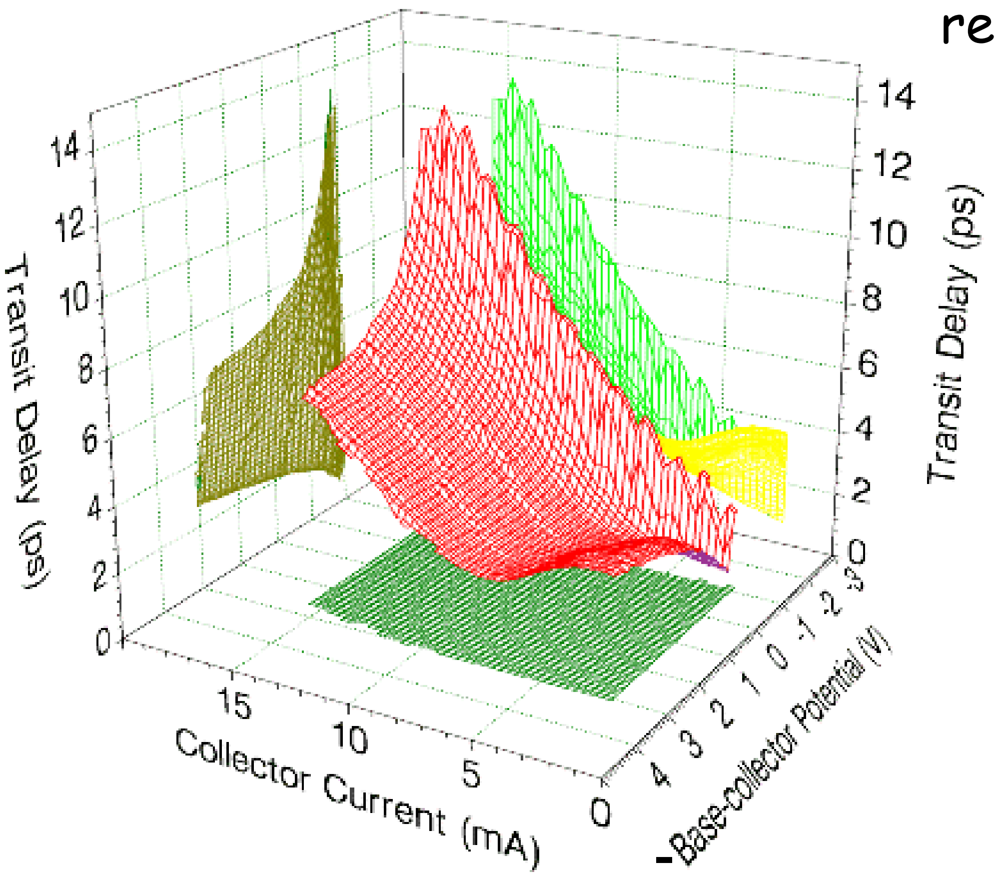
$$\frac{\partial \tilde{\tau}_C}{\partial V_{BC}} = \frac{\partial \tilde{C}_C}{\partial I_C}$$

Q_{CC} can then be constructed directly from data by:

$$Q_{CC} = \oint_{contour} [\tilde{C}_C dV_{BC} + \tilde{\tau}_C dI_C]$$

III-V HBT Base-Collector Delay / Capacitance model [4]

Measured base-collector transit time



Shape of delay (before Kirk effect) related to velocity-field curves

$$\frac{\partial \tilde{\tau}_C}{\partial V_{BC}} = \frac{\partial \tilde{C}_C}{\partial I_C}$$

"Capacitance cancellation" effect in III-V HBTs follows

$$Q_{CC} = \oint \tilde{C}_C dV_{BC} + \tilde{\tau}_C dI_C$$

$$(Q_{dif} \neq \tau(V, I) \cdot I)$$

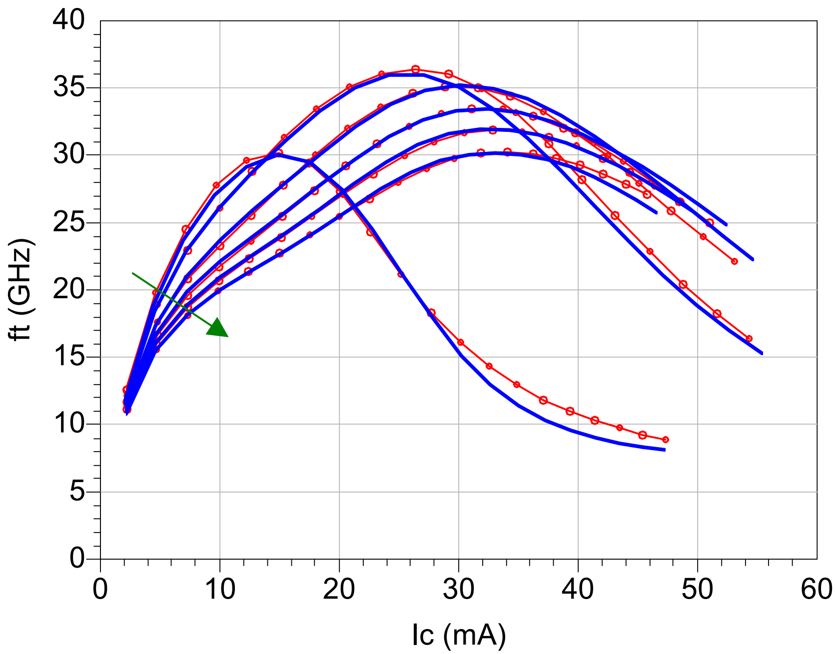
Device data, model equations, and physics consistent

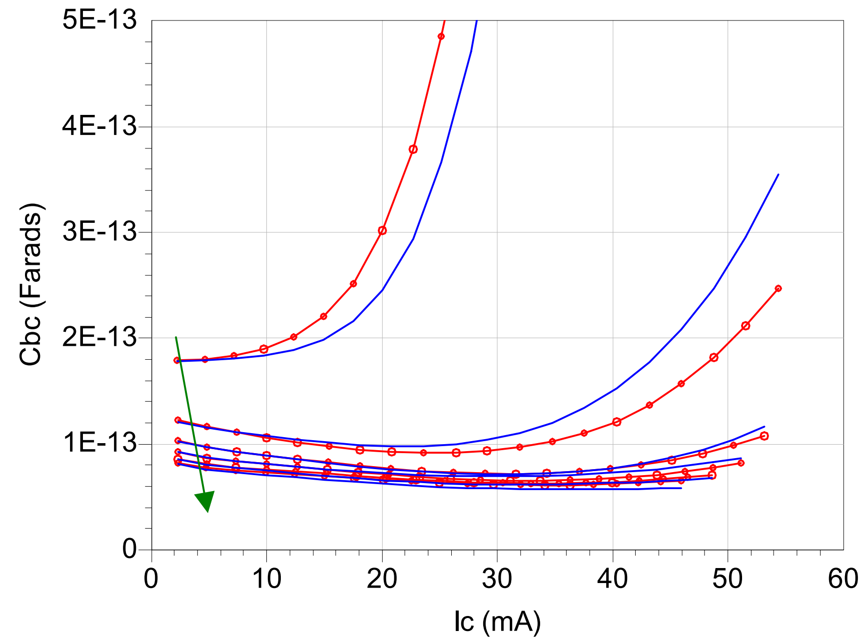
GaAs HBT power cell (“2x20 quad-emitter” device): (4x2x20) f_T & C_{BC} vs. I_C

Measurements

Simulations [25]

V_{CE}=0.5 to 3V w/0.5V per step

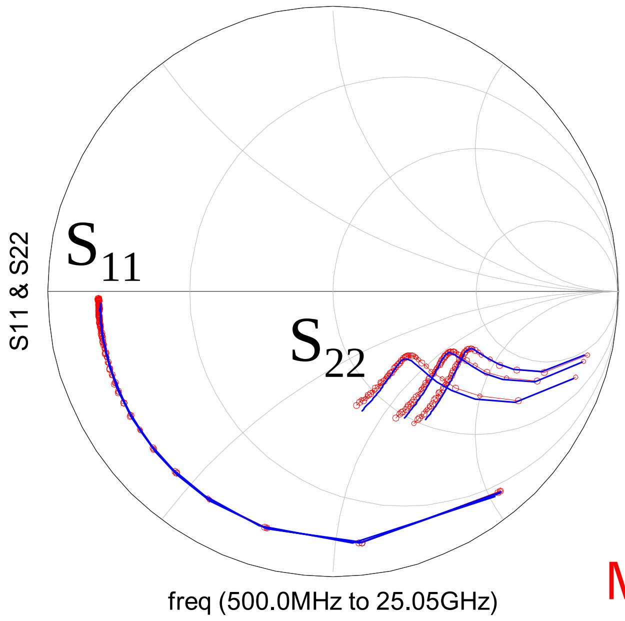


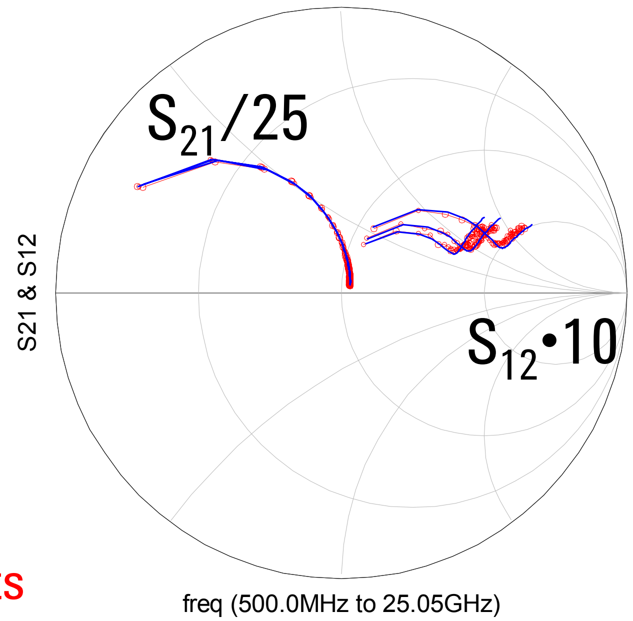


Accurate charge model necessary to fit both
f_T and C_{BC}, simultaneously over wide range of bias.

Si-based models do not fit this behavior well, generally

GaAs HBT power cell ("2x20 quad-emitter" device): S-parameters: 0.5-25.05 GHz





Measurements

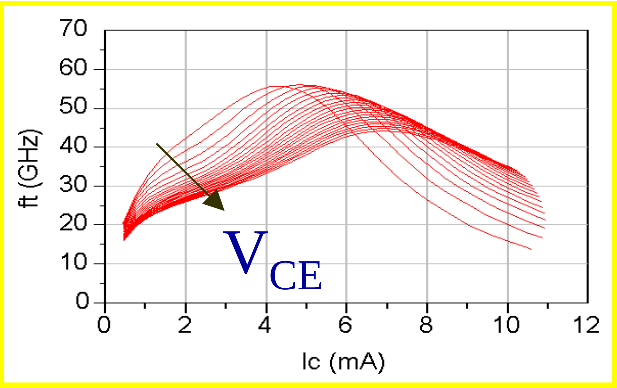
Simulations

V_{CE}=1,2,3V

J_C=0.05mA/μm^2

Agilent Technologies

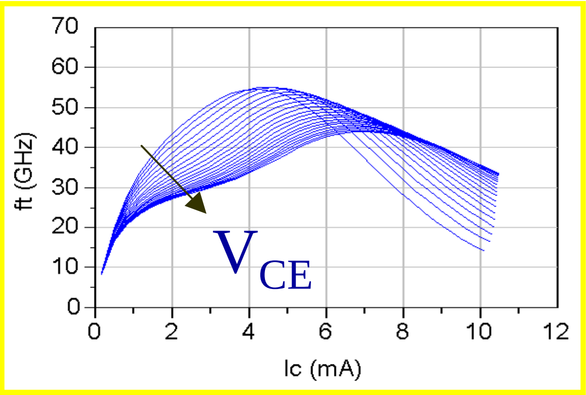
Nonlinear Charge Modeling: Bias-Dependent IM3 of III-V HBTs [4]

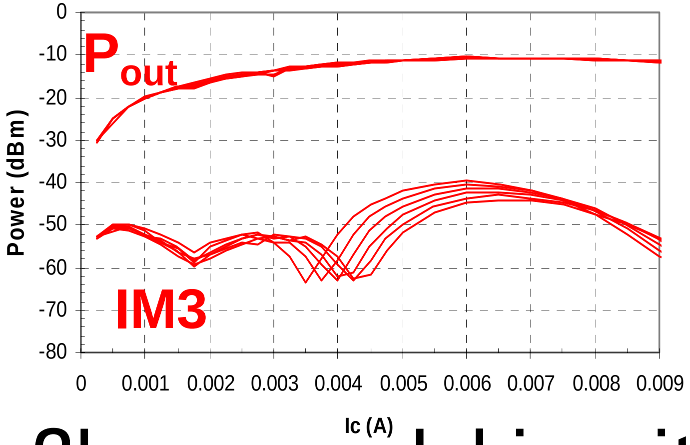


Measured f_T
Simulated f_T

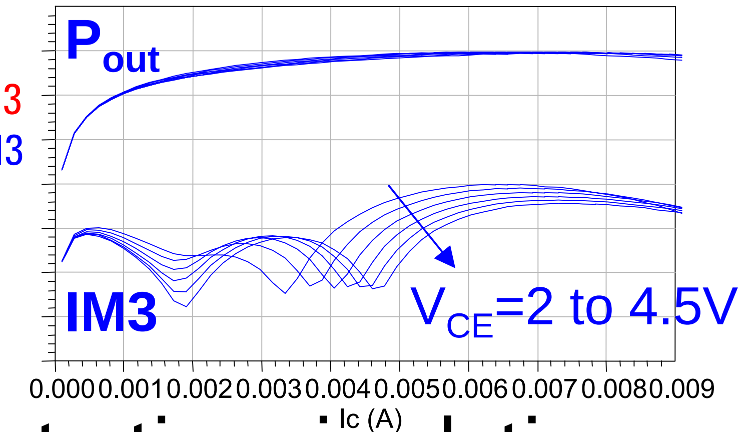
f_T related to τ

τ modeled by Q



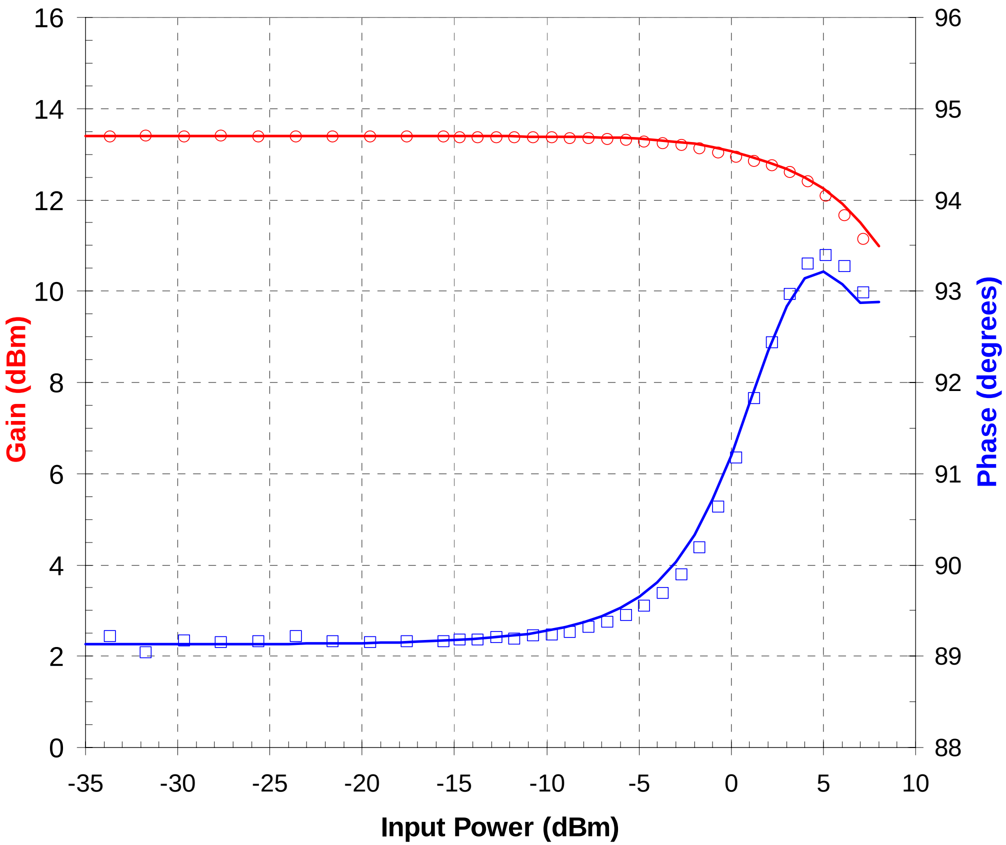


Measured Pout, IM3
Simulated Pout, IM3



Charge model is critical for distortion simulation

6x(2x14)μm^2 InGaP/GaAs HBT cell: AM-AM and AM-PM distortions



Symbols: Measurement

Solid lines: Simulation

V_{CE}=3.5V

J_C=0.12mA/μm^2

Frequency=5GHz

R_L=50Ω

Good collector charge model critical for accurate AM-AM and AM-PM

Presentation Outline

- Introduction
- Nonlinear Charge Modeling
- Electro-Thermal Modeling
- Advanced Measurements
- Mathematical CAD Techniques
- Summary & Conclusions

Dynamic electro-thermal (self-heating) model
Algebraic perspective

T(t) is a *dynamical variable*

$$I_c(t) = I_c(V_{be}(t), V_{ce}(t), T(t))$$

$$Q_{tc}(t) = Q_{tc}(V_{bc}(t), I_c(V_{be}, V_{ce}, T(t)), T(t))$$

Charge due to transit delay is a function of temperature

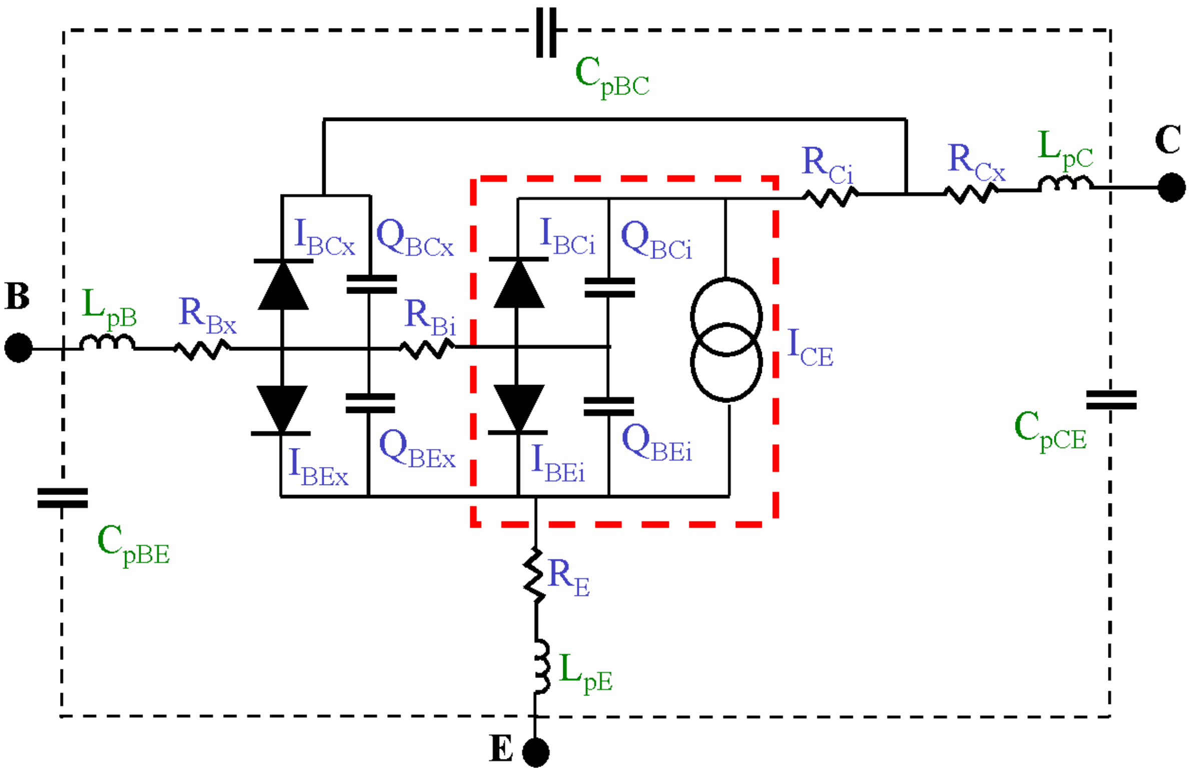
Temperature evolution equation based on dissipated power

$$\tau \frac{dT}{dt} + \Delta T = R_{TH} I_C V_{CE}$$ simplified

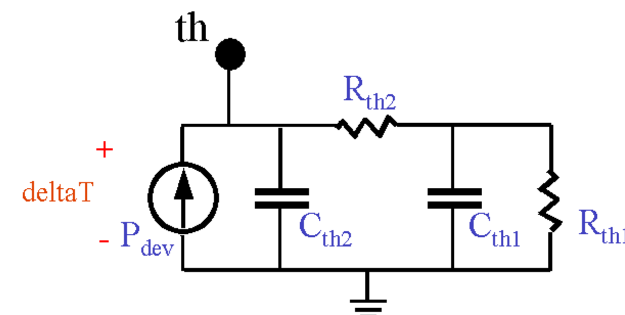
T(t) calculated by the simulator *self-consistently*

Dynamic electro-thermal (self-heating) model [25]

Currents, Voltages, and T(t) calculated by the simulator *self-consistently* using *coupled electrical and thermal equivalent circuits*



$$T_{dev} = T_{amb} + deltaT$$

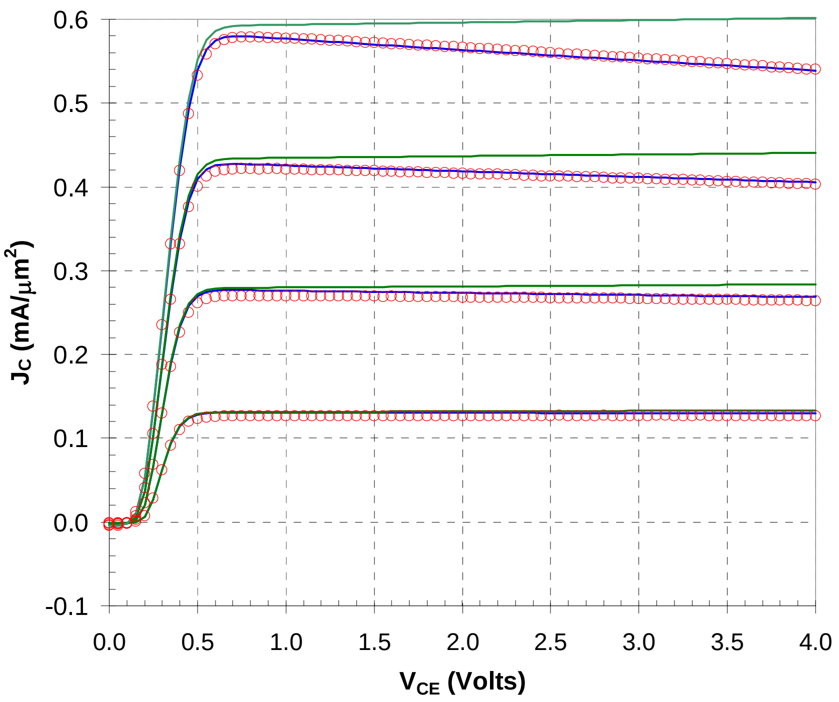


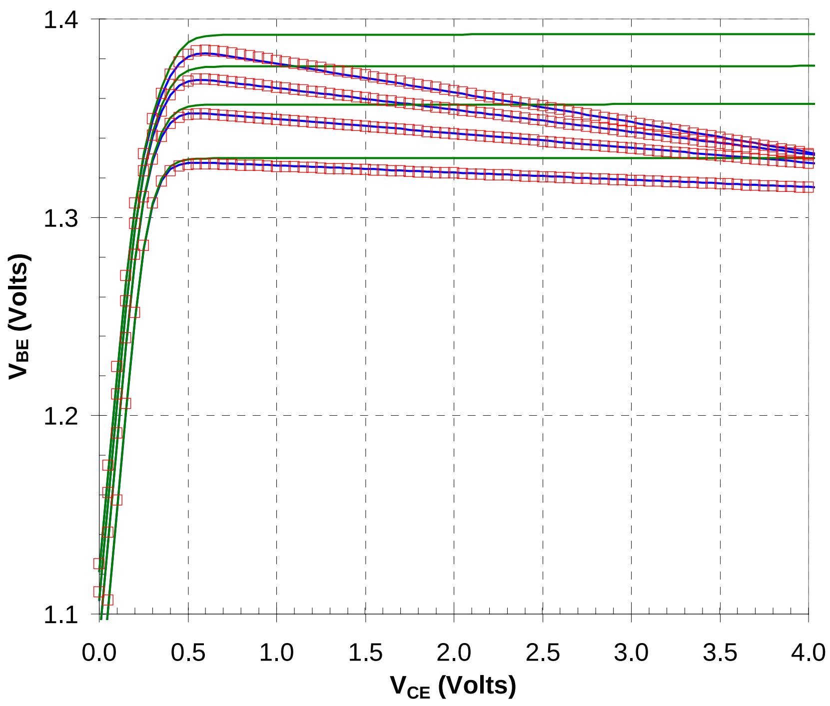
T_{dev}=device junction temperature

T_{amb}=device ambient (backside) temperature

2-pole thermal circuit used. Collapsible to single node.

Self-heating model (static case)



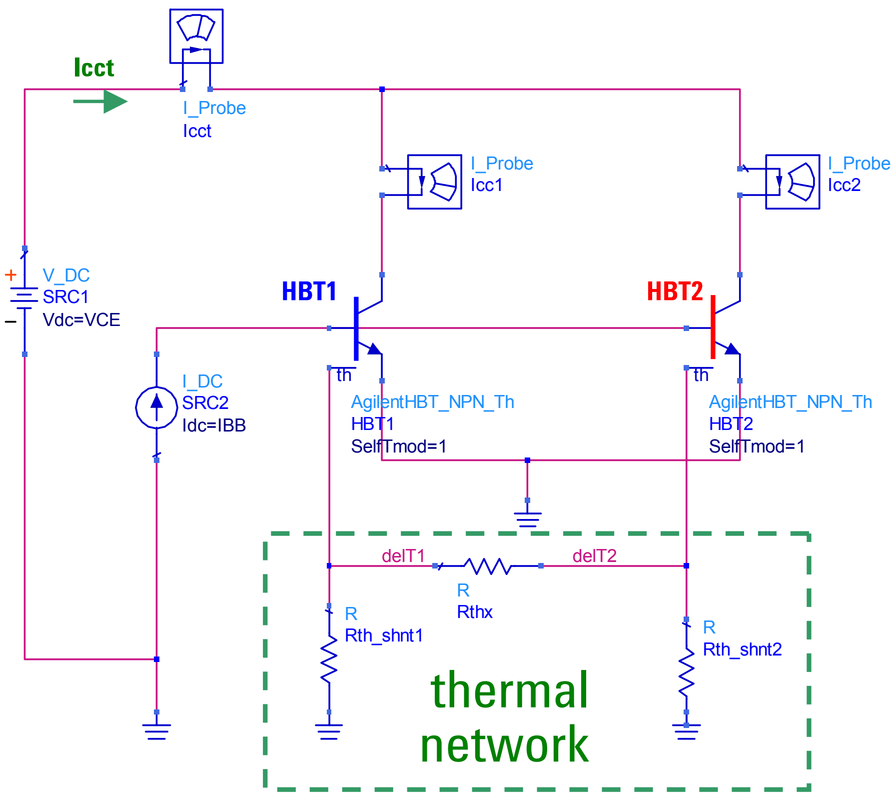


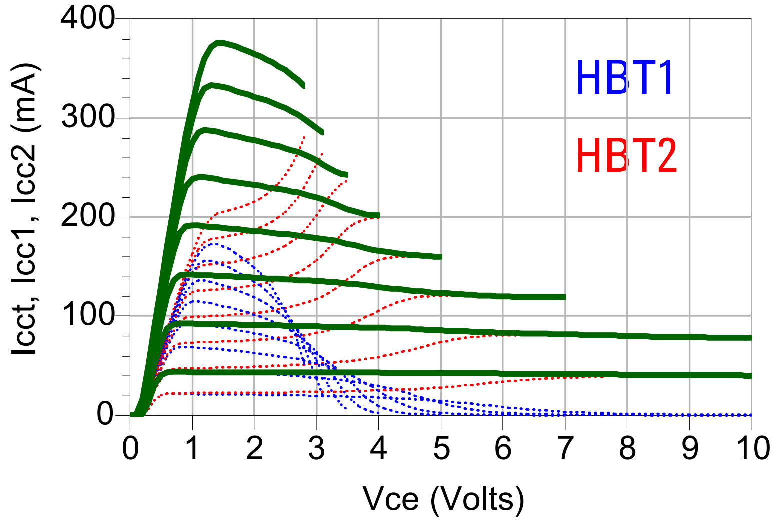
Measurement

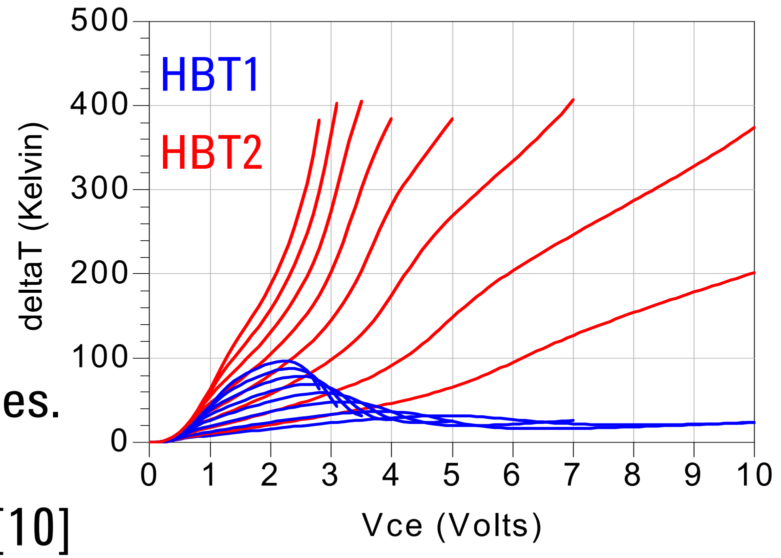
Self-heating model [25]

Isothermal model

Thermal Coupling: Current Collapse Instability Simulated with III-V HBT Model [25]







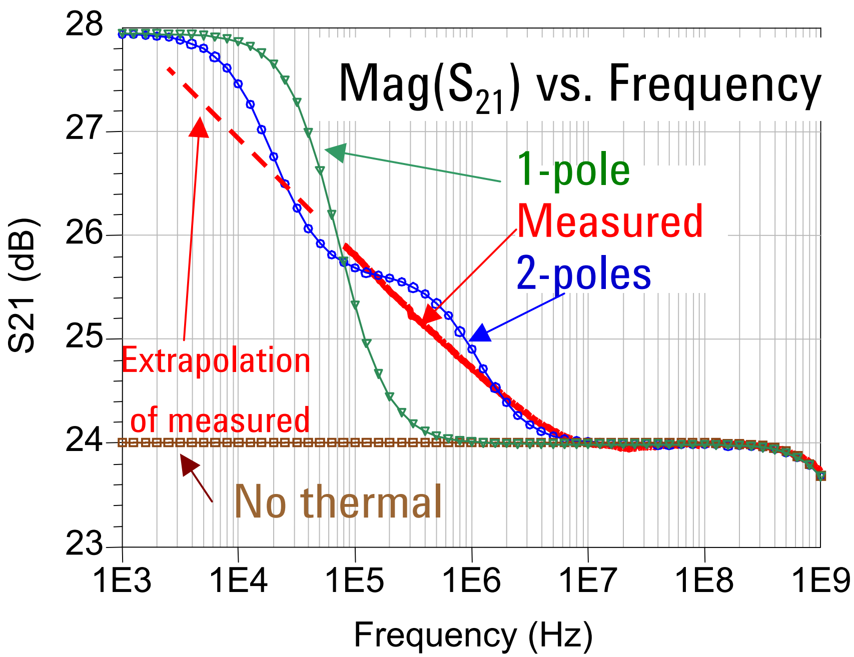
- Thermal node allows interactions between devices.
- Temp limited for convergence (but see [11])
- Realistic thermal constitutive relations required [10]

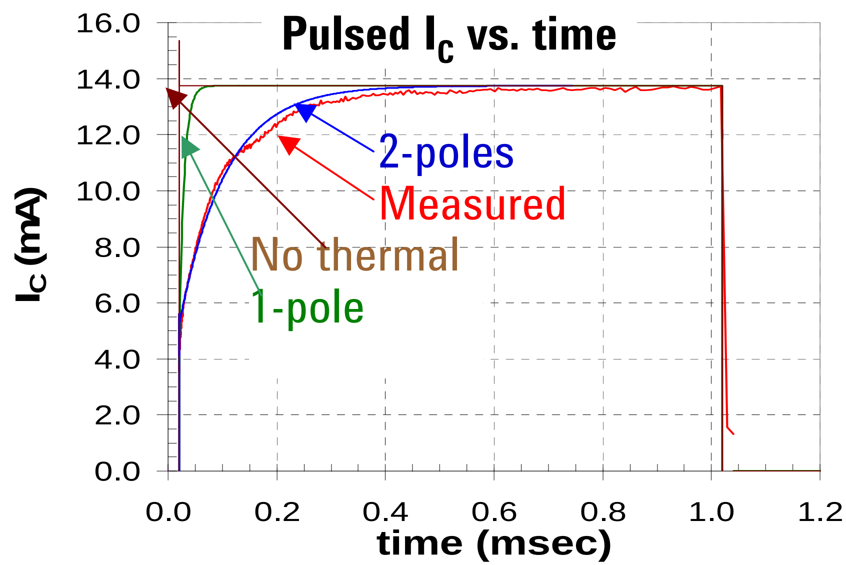
Dynamic electro-thermal III-V HBT Model

Low Freq. S-parameters and Pulse Response Measured/Simulated

Comparison of different thermal equivalent circuits in

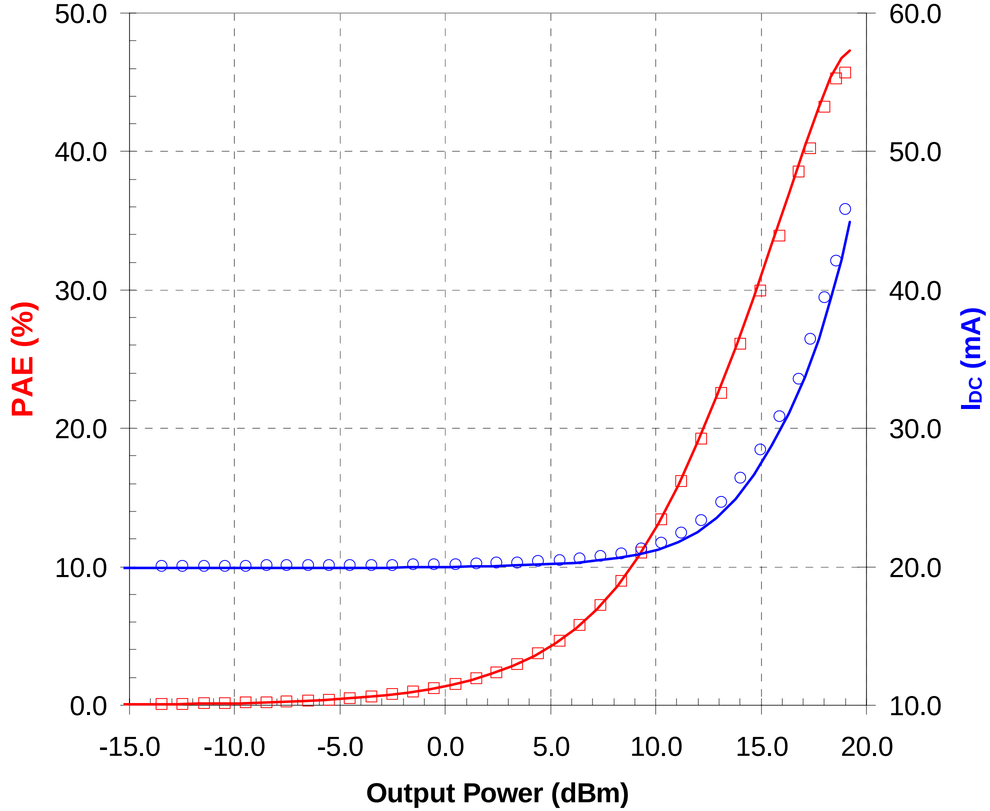
Linear (s-parameter) and Transient (time-domain) cases





Two poles are more accurate than one [8].
Compromise between speed and accuracy (SPICE).
Distributed models can be used for HB analysis [7].

6x(2x14)μm^2 InGaP/GaAs HBT cell: Electro-thermal Model Simulates PAE & I_{DC} Accurately



V_{CE}=3.5V

J_C=0.12mA/μm^2

Frequency=5GHz

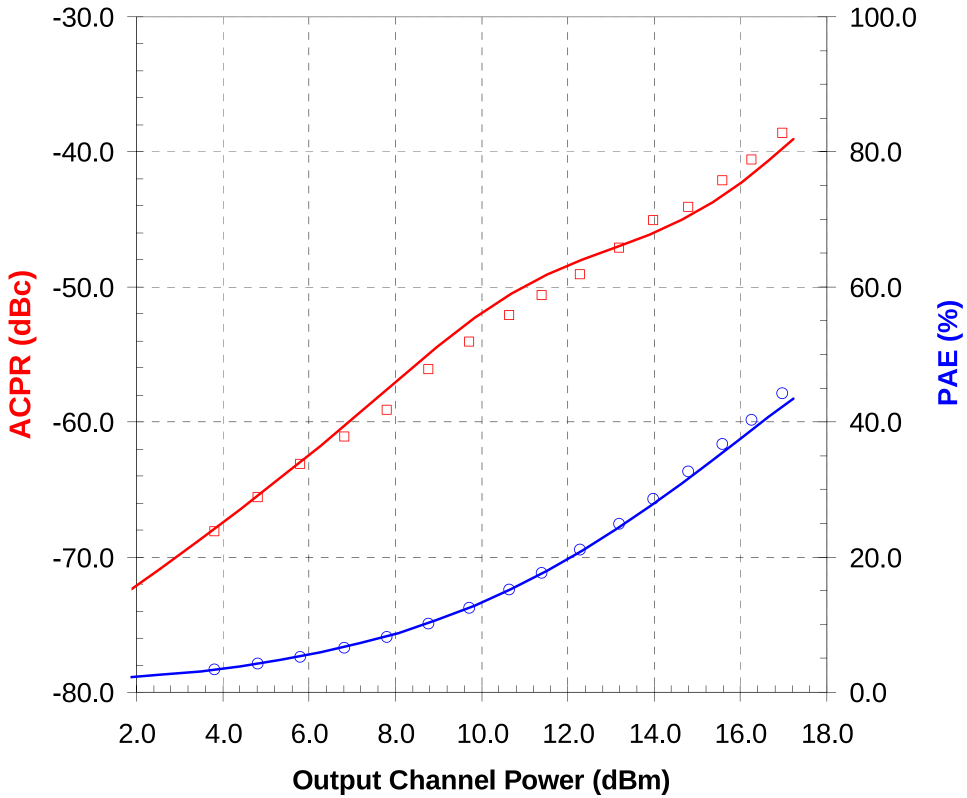
R_L=50Ω

Simulation: 1-tone HB

Symbols: Measurement

Solid lines: Simulation

$6x(2x14)\mu m^2$ InGaP/GaAs HBT cell: ACPR & PAE vs. Output Power



V_{CE}=3.5V

J_C=0.12mA/μm^2

Frequency=1.9GHz

R_L=50Ω

Modulation: IS-95 Rev. Link

Simulation: Envelope

Symbols: Measurement

Solid lines: Simulation

Agilent Technologies

Presentation Outline

- Introduction
- Nonlinear Charge Modeling
- Electro-Thermal Modeling
- Advanced Measurements
- Mathematical CAD Techniques
- Summary & Conclusions

Advanced Measurements

Essential for

- **Model Development**
- **Model Validation**
- **Device characterization for technology development**

Can not always infer dynamic large-signal behavior from only static (DC) or linear (*S*-parameter) data

Preferred for characterizing limiting behavior (e.g. breakdown)

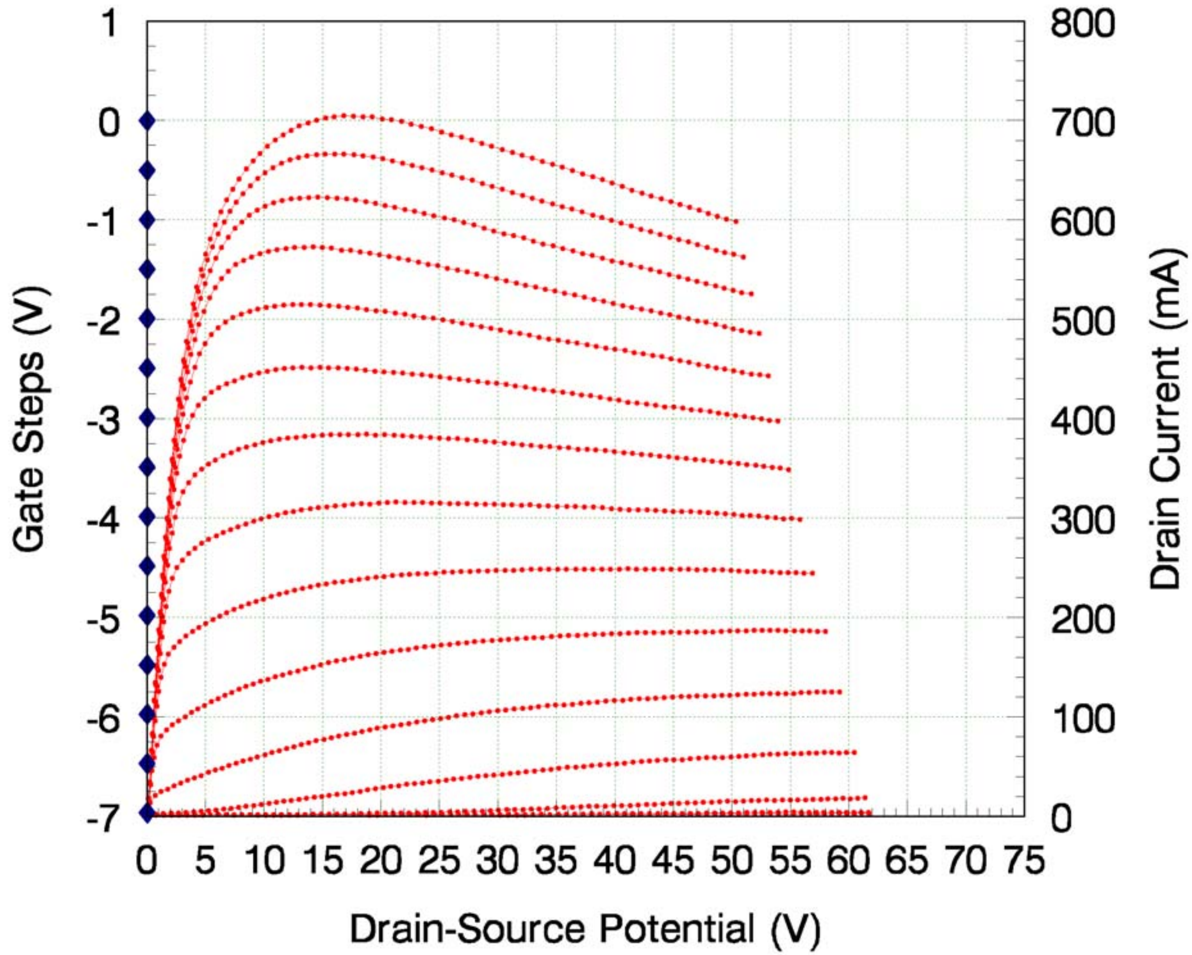
GaN Devices

1 mm 10 fingers

GaN on Si

f_T ~ 30GHz

Pulse width 2us



Pulsed measurements provide much more data than can be measured under static (DC) conditions

micro GaN GmbH

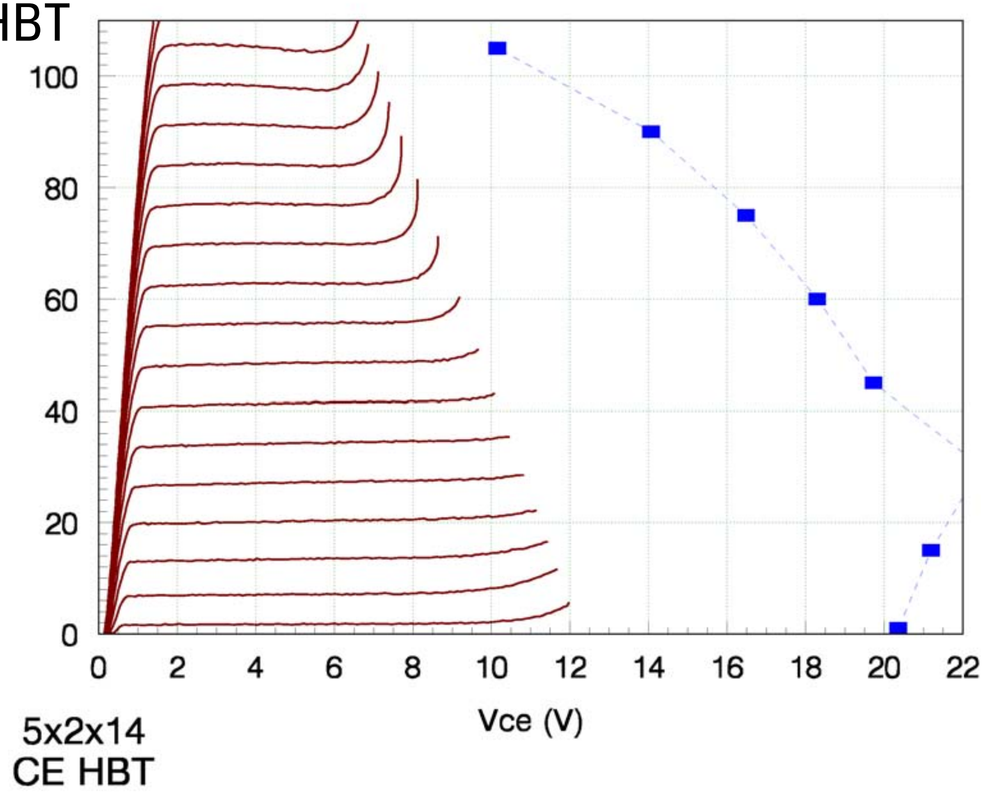
Agilent Technologies

Pulsed data on III-V HBT
Current dependence of breakdown [15]

5x2x14 CE GaAs HBT

f_T ~ 60GHz

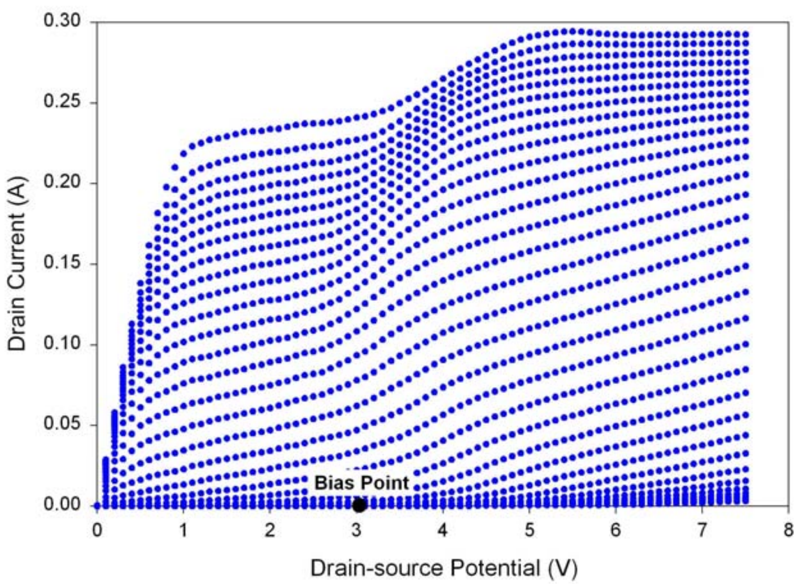
Pulse width 1us

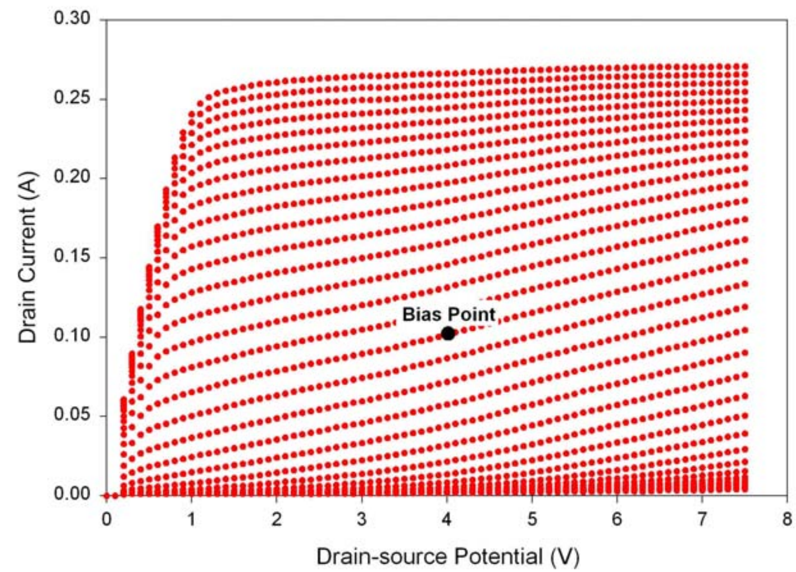


Can observe and extract breakdown parameters

Pulsed Bias Measurements

Same 0.25um PHEMT device

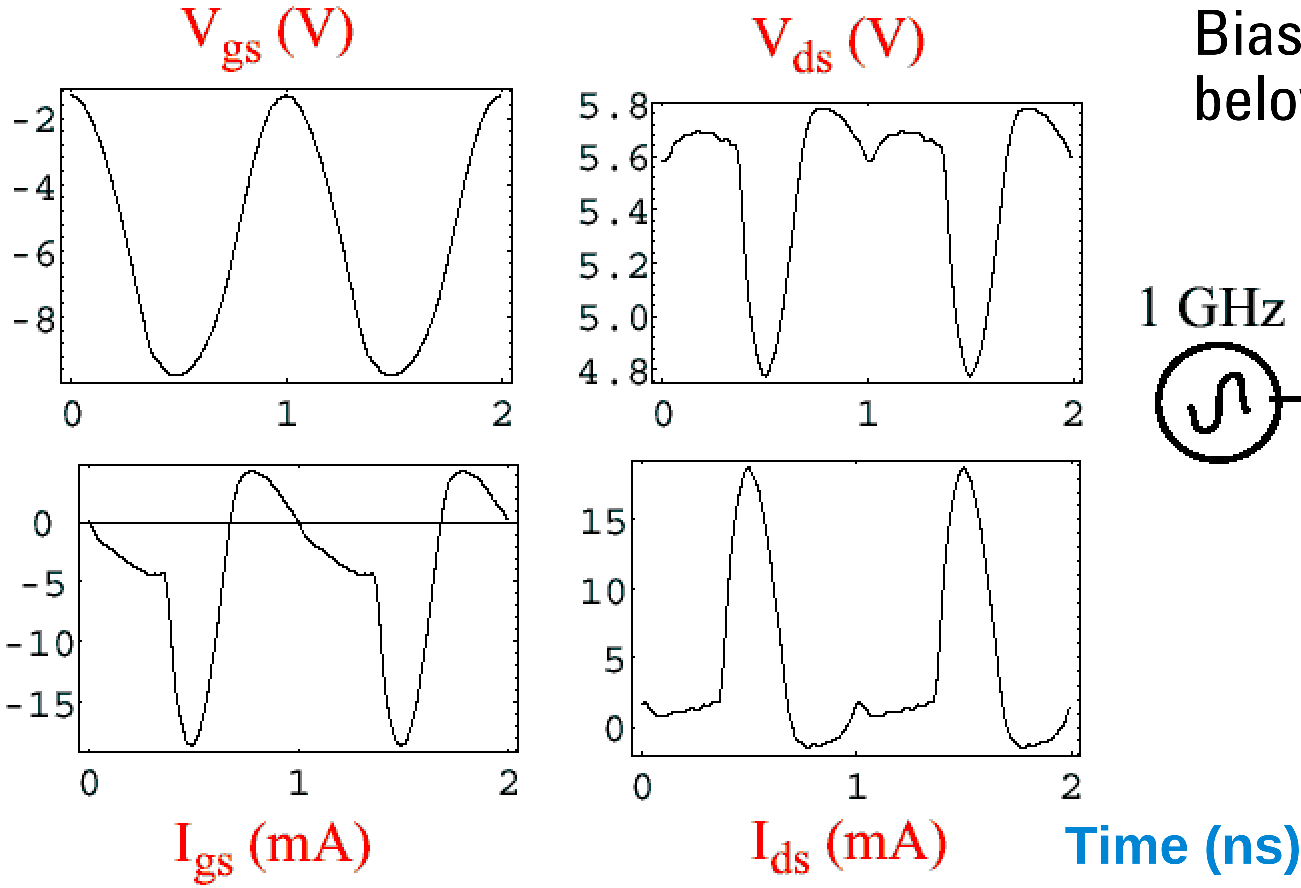




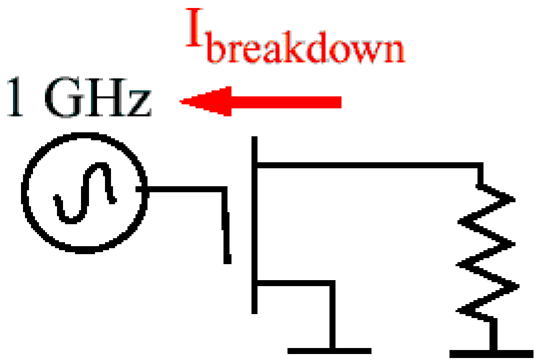
Soak time ~20 ms   Pulse width ~200 ns   "Iso-dynamic"

Can use to separate thermal and trapping effects

Vector Nonlinear Network Analyzer (VNNA) Measurements: *Breakdown Current*

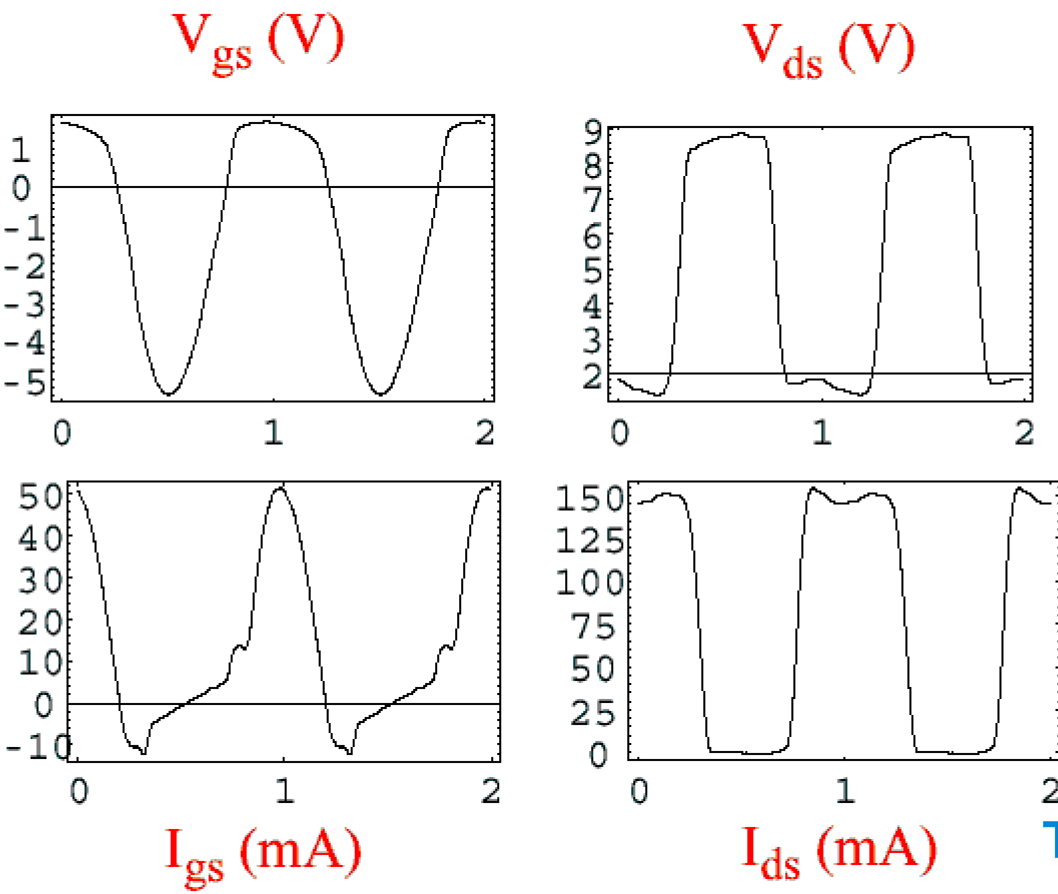


Biased well below pinch-off



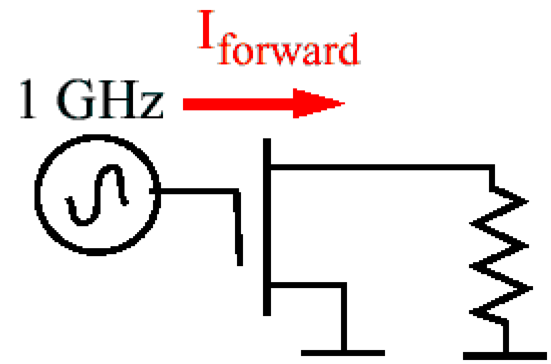
Measure device under conditions of actual use.
Examine reliability under these conditions.

Vector Nonlinear Network Analyzer (VNNA) Measurements:
Forward Gate Current



Time (ns)

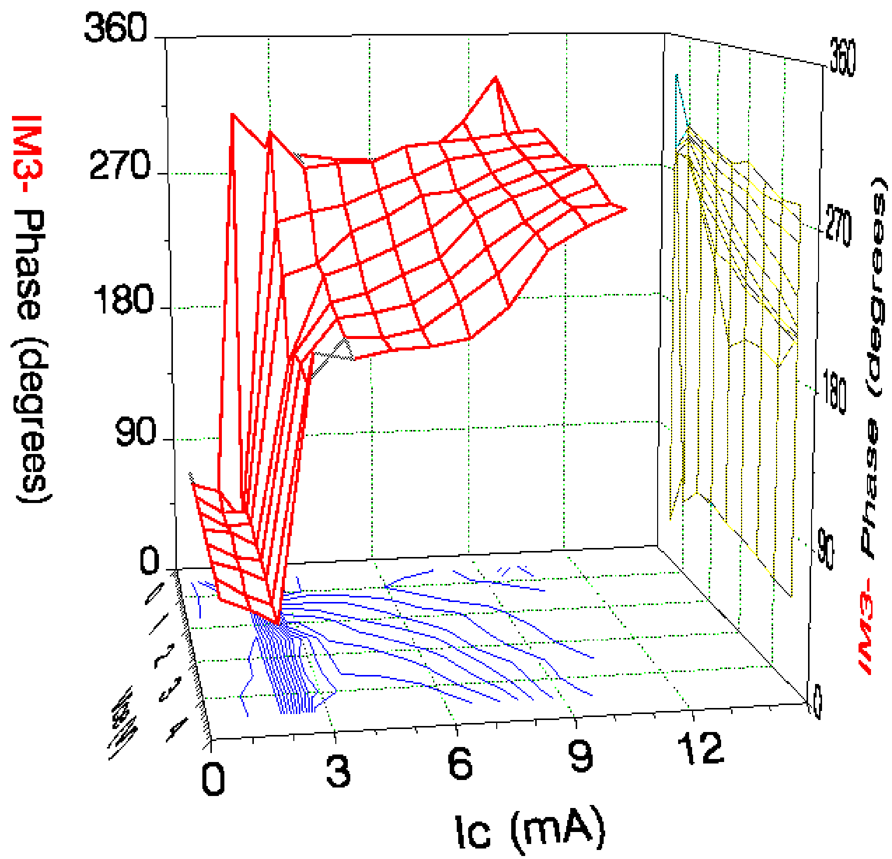
Biased less negatively than before



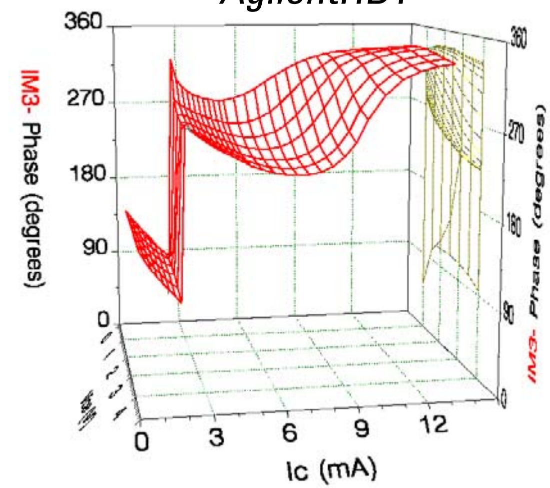
Measure device under conditions of actual use.
Forward gate current in pHEMTs is complicated.

Vector Nonlinear Network Analyzer (VNNA) Measurements: *Phase of device intermodulation* versus bias

measured



Simulated *AgilentHBT*

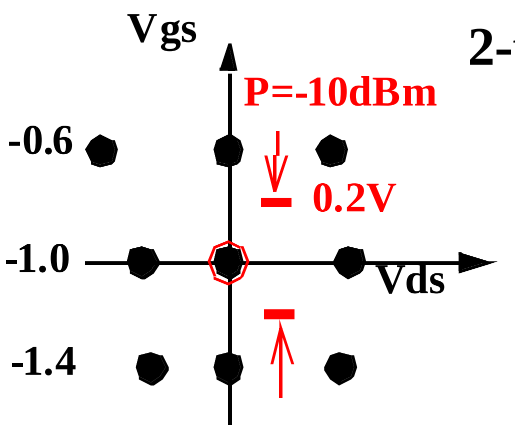


Presentation Outline

- Introduction
- Nonlinear Charge Modeling
- Electro-Thermal Modeling
- Advanced Measurements
- Mathematical CAD Techniques
- Summary & Conclusions

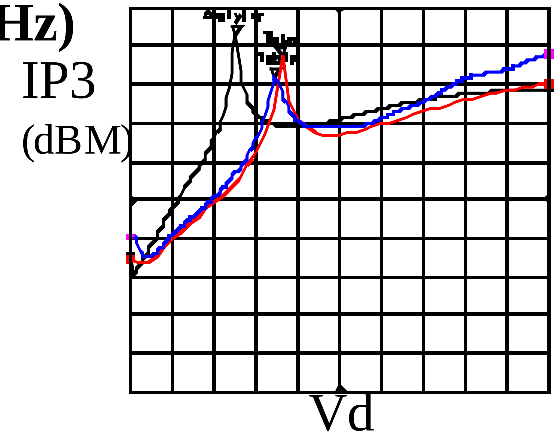
Table-Based Model Limitation

Naive simulator interpolation -> poor distortion

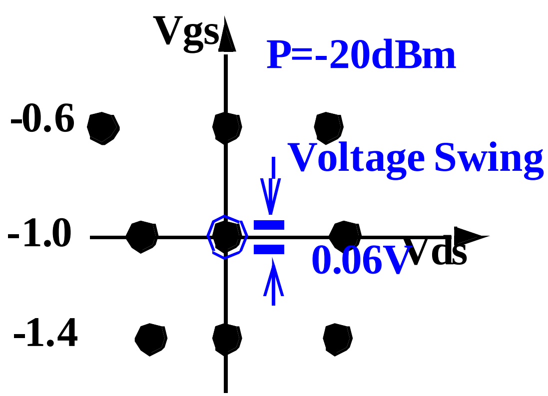


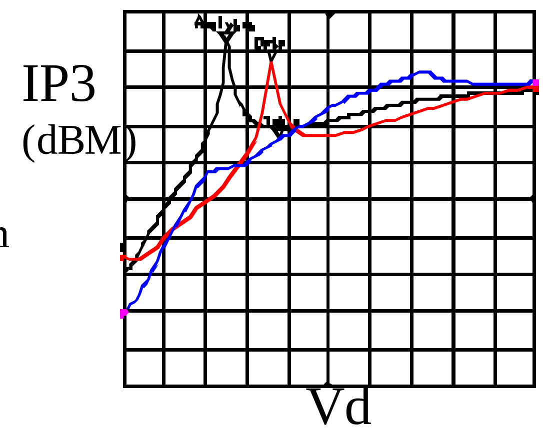
2-tones @ 100MHz (+1MHz)

Si NJFET
Table Model



(a) Vg=-1V Power=-10dBm





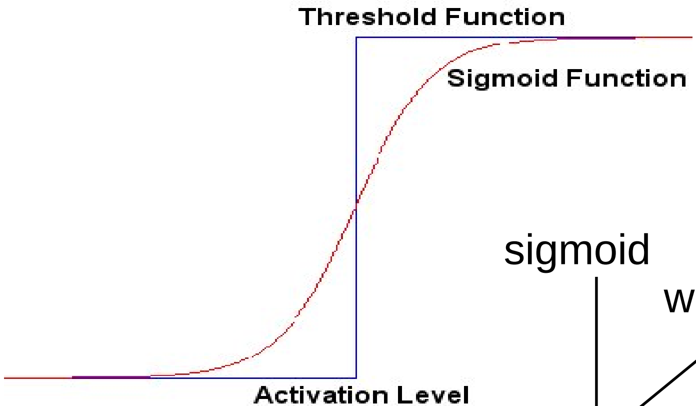
(b) Vg=-1V Power=-20dBm

Null in third derivative of spline w.r.t. Vgs (2^{nd} axis) with symmetrical data points

Interpolation model is better when signal size ~ data spacing

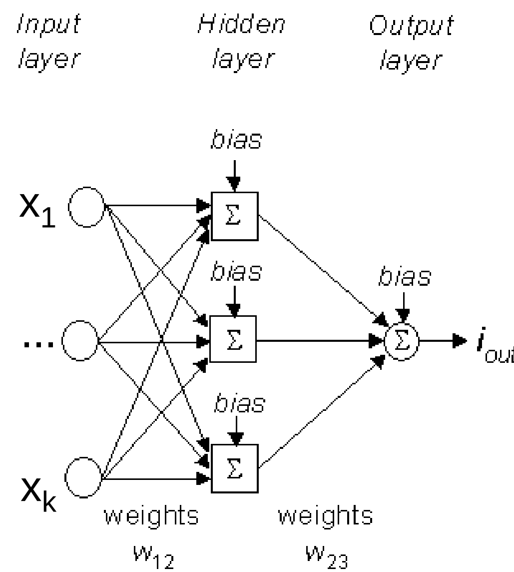
Artificial Neural Networks

A NN is a parallel processor made up of simple, interconnected processing units, called *neurons*, with weighted connections.



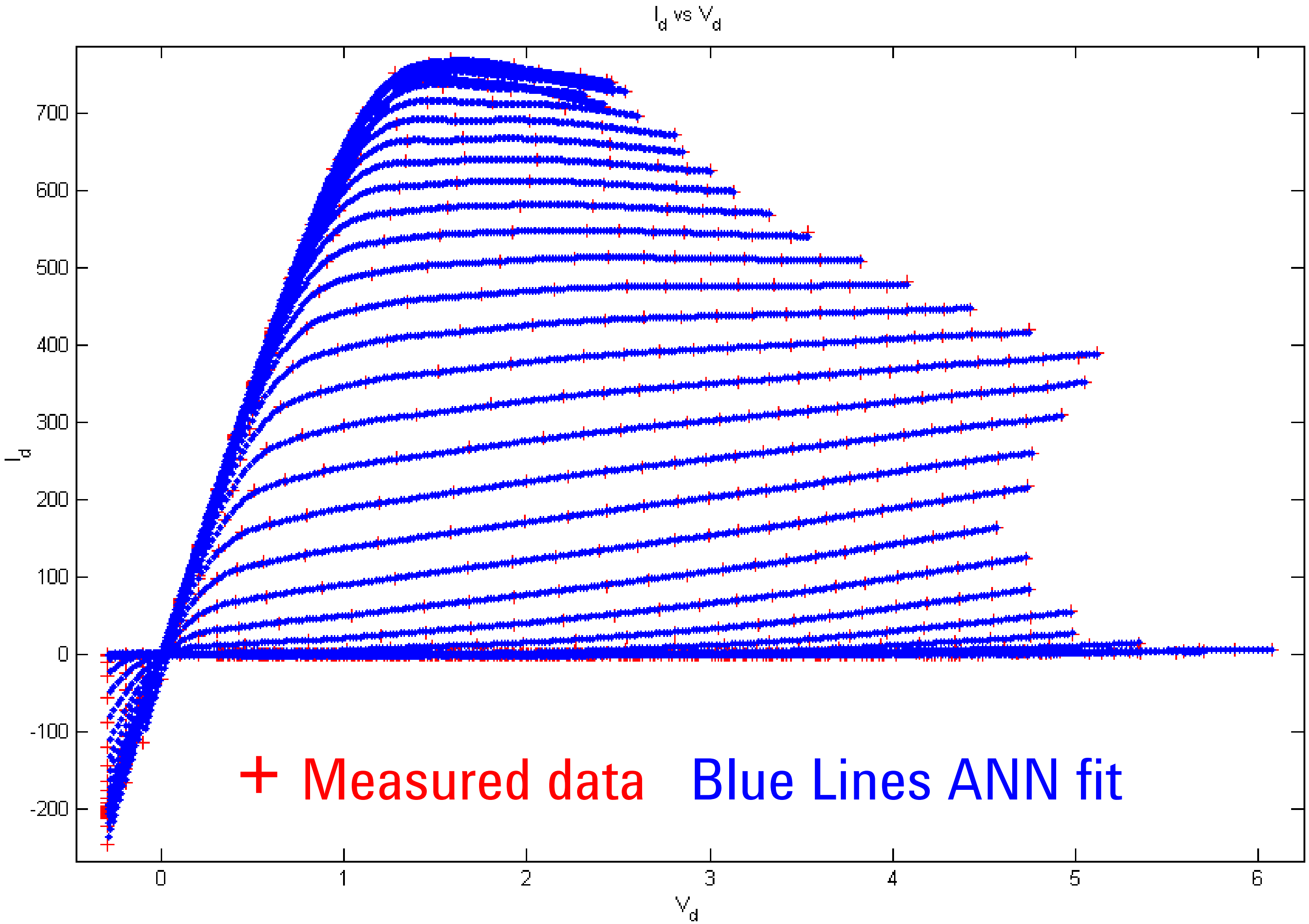
sigmoid   weights   biases

$$F(x_1,\ldots,x_K)=\sum_{i=1}^{I} v_i\, s\left(\sum_{k=1}^{K} w_{ki}x_k + a_i\right)+b$$



- Universal Approximation Theorem: Fit “any” nonlinear function of any # of variables
- Infinitely differentiable: good for distortion.
- Easy to train (fit) using standard third-party tools (MATLAB)

Artificial Neural Networks: Excellent, smooth fit. Better than simple table-based models



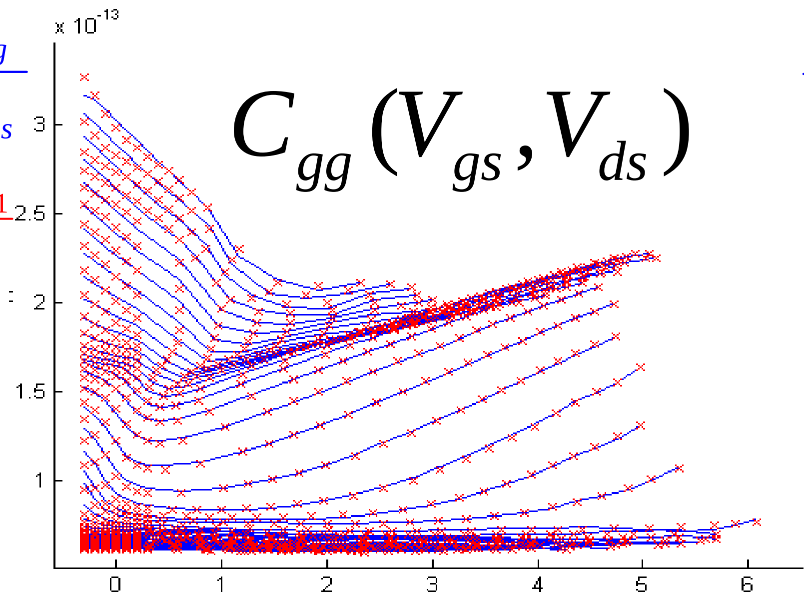
Adjoint Neural Network [21]

Constructing FET gate charge, Q_g, given

$$\left(\operatorname{Im} Y_{11}^{meas}, \operatorname{Im} Y_{12}^{meas}\right)$$

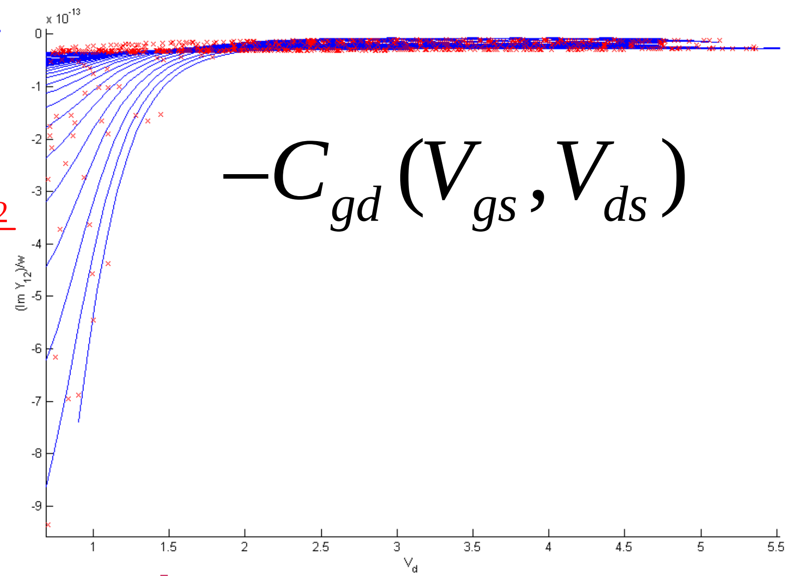
Experimental validation of *terminal charge conservation* at the gate for GaAs pHEMT

$$\frac{\partial Q_g}{\partial V_{gs}} \qquad \frac{\operatorname{Im} Y_{11}}{\omega}$$



V_{ds}

$$\frac{\partial Q_g}{\partial V_{ds}} \qquad \frac{\operatorname{Im} Y_{12}}{\omega}$$



V_{ds}

X measured

— modeled

Agilent Technologies

Summary and Conclusions

- Charge Modeling shown to be critical for simulating PA FoMs
- Terminal Charge Conservation modeling principle discussed in detail.
- Two-dimensional FET capacitances
- Voltage & Current dependent transit time and capacitance in III-V HBTs
- Electro-Thermal Effects shown to be important for PA simulation
- Static and dynamic self-heating necessary to fit device characteristics
- Technical issues with thermal equivalent circuit, thermal coupling, and thermal constitutive relations summarized
- Advanced Measurements shown to reveal rich device behavior
- Advanced CAD shown promising for better PA simulation models