Geometrical Effect Analysis on f_T and f_{max} of 0.18 μm SiGe HBT

By

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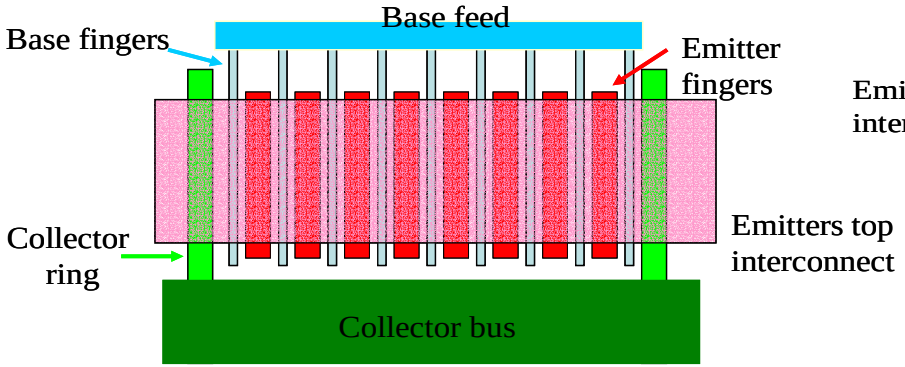
Outline

- 0.18 μm SiGe power cell design
- Power cell analysis
  - I_c- V_{CE} Curves
  - Forward Gummel plot
  - Parallel plate Capacitor on Dielectric substrate
  - Back-End 3D-EM simulation
  - Device f_T and f_{max}
  - Transit time extraction
  - Devices performance comparison
- Status
- Conclusion

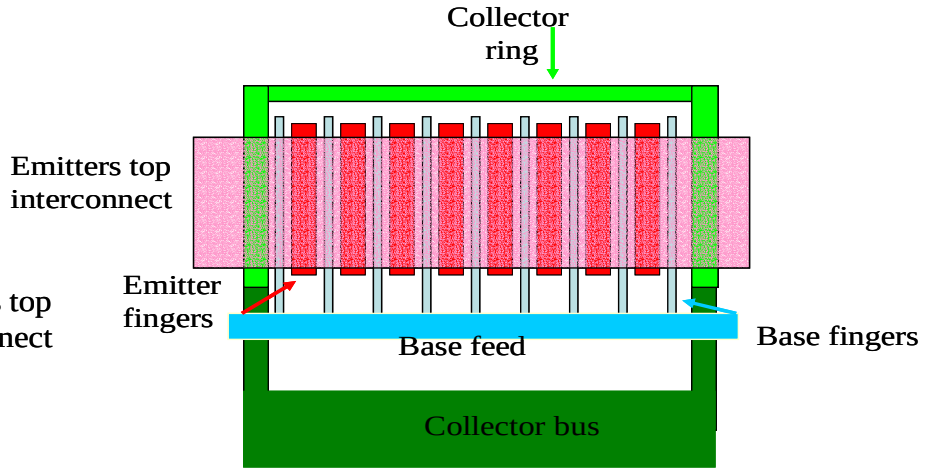
Purpose

- The purpose of this work is to analyze the geometrical effects of parameters f_T and f_{max} of 0.18 μm high speed SiGe HBTs technology.
- The three unit-cell layout design are proposed to investigated the geometrical effect in this study.
- The standard unit-cell can be applied in power cell for power amplifier design.

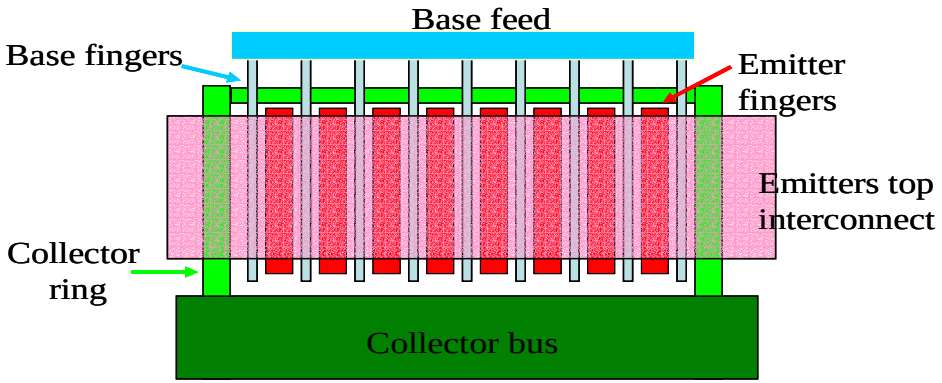
0.18 μm SiGe power cell design



A_1



C_1



B_1

In A_1 Structure, the base feed has no overlap with the collector trace

In B_1 Structure, the base fingers have overlap with the collector ring

Power cell analysis: I_c- V_{CE} Curves

I_b=30 μA–150 μA

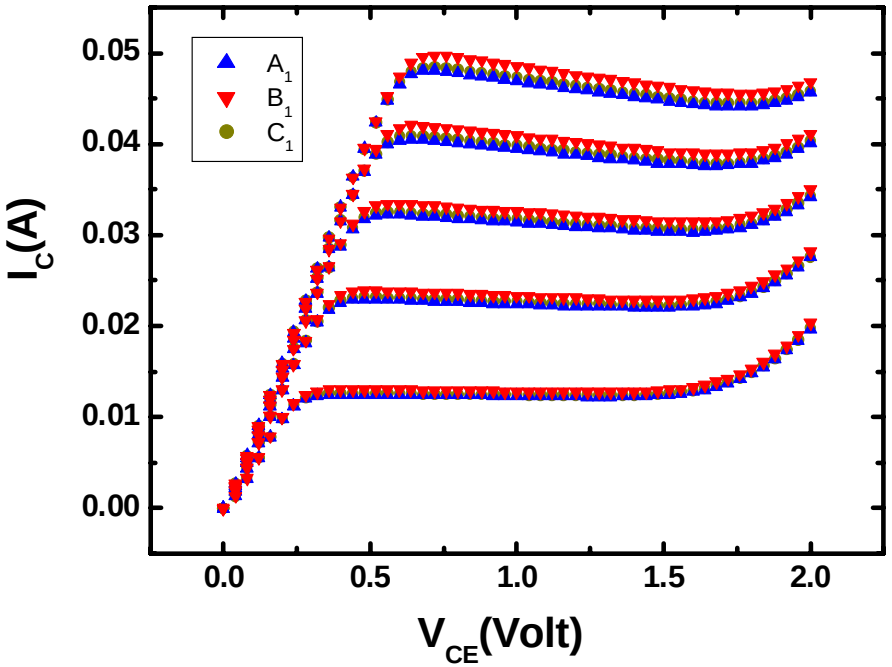


Fig. 1.

I_b=60 μA–300 μA

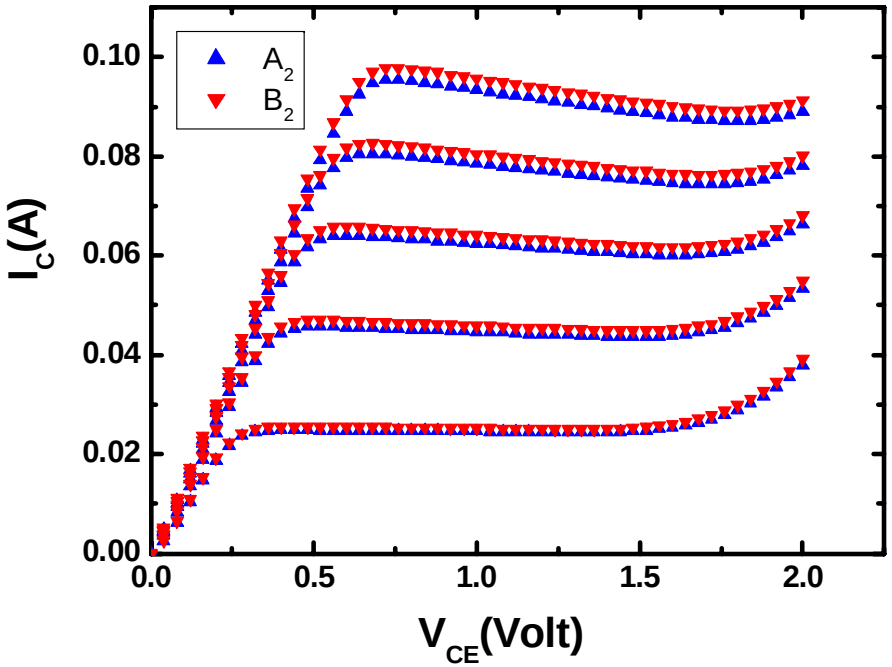


Fig. 2.

Measured I_V curves for three devices (A_1, B_1, and C_1) and two devices (A_2 and B_2) demonstrate the similar dc performance.

Forward Gummel plot

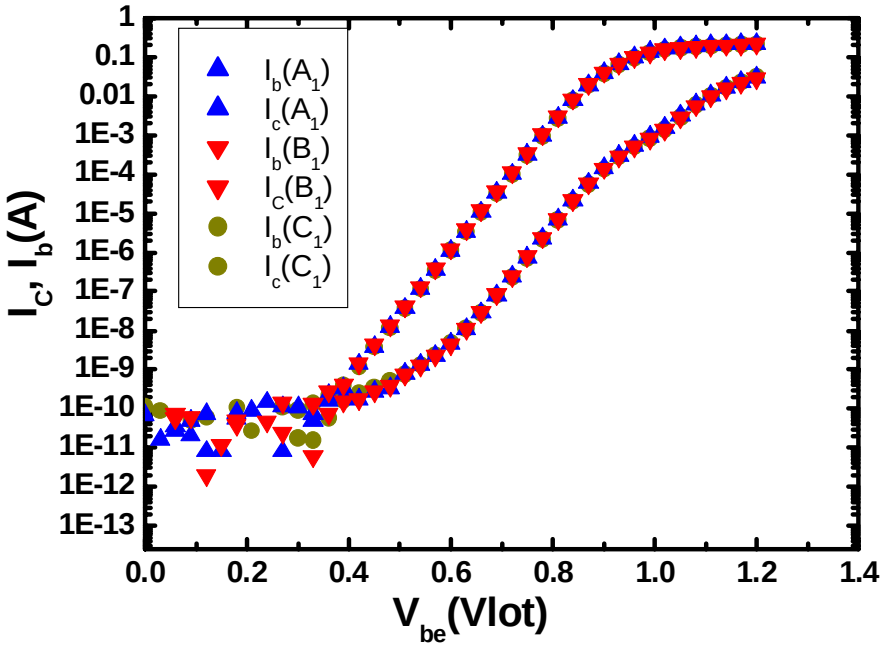


Fig. 1.

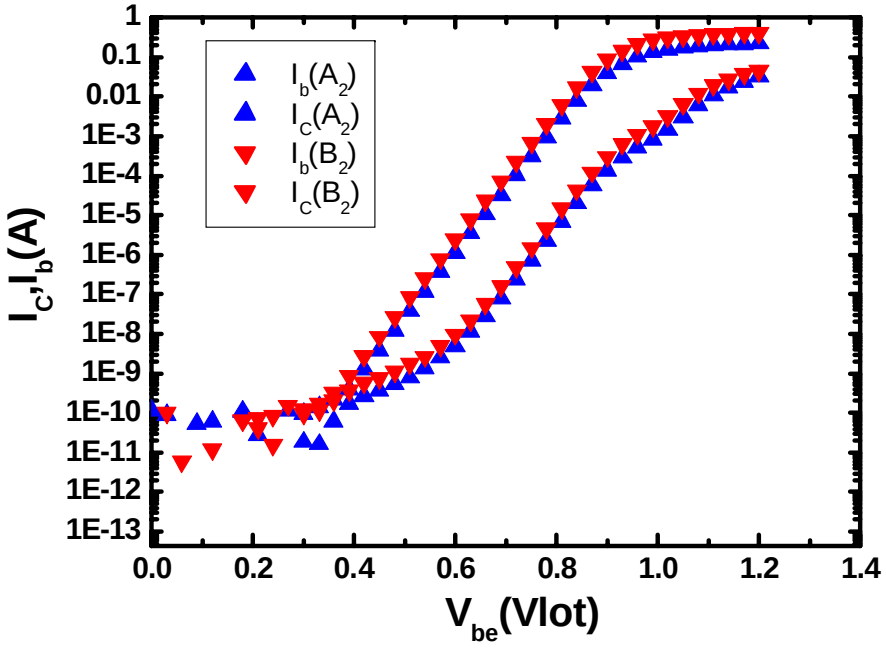
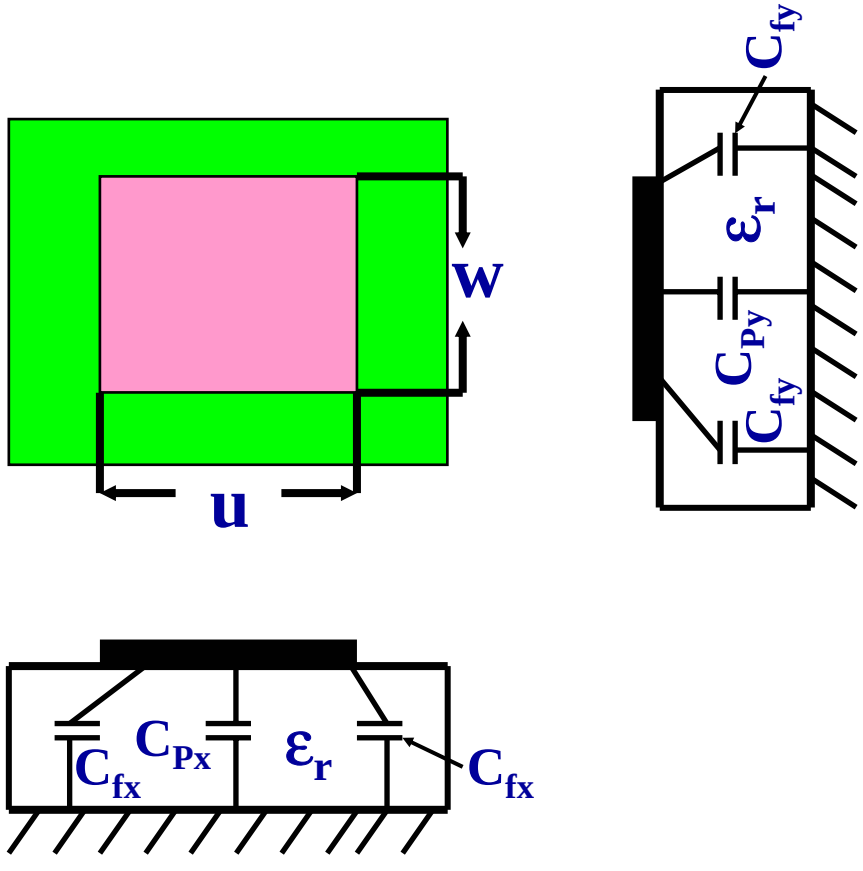


Fig. 2.

Measured Forward Gummel plots (V_{BC} = 0.5V) for three devices (A_1, B_1, and C_1) and two devices (A_2 and B_2) demonstrate the similar dc performance.

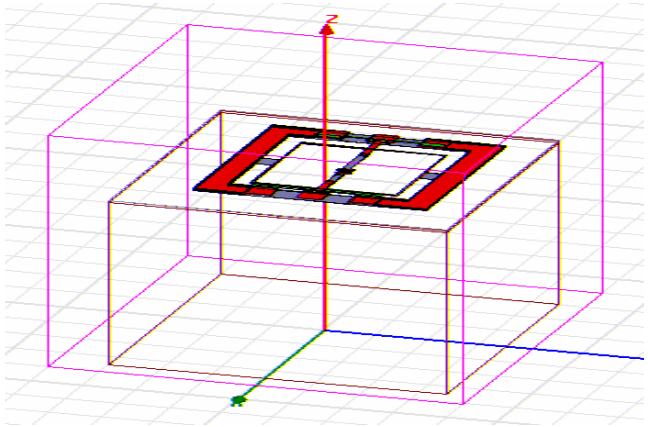
Parallel plate Capacitor on Dielectric substrate



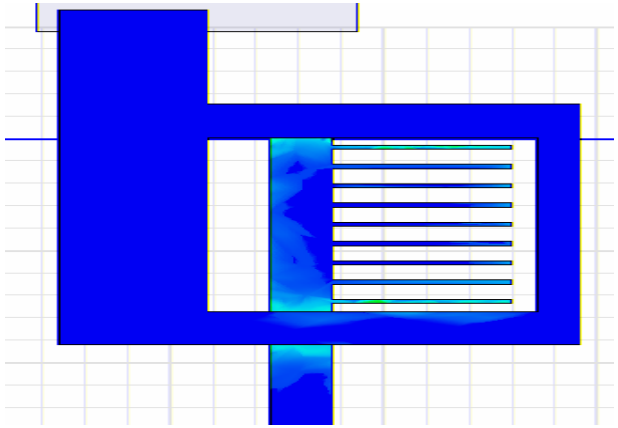
Total parallel plate capacitance

$$C_{Total} = C_P + 2C_{fx} \times W + 2C_{fy} \times u \qquad (1)$$

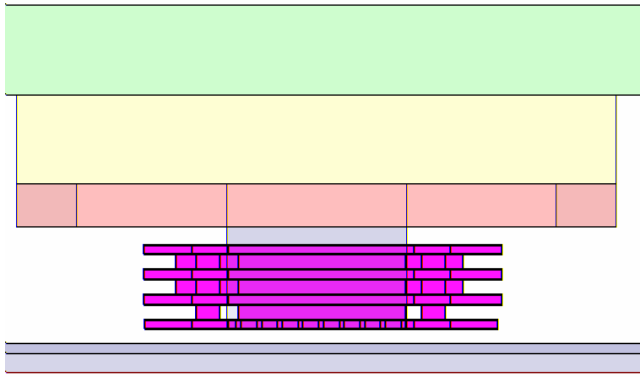
Back-End 3D-EM Simulation



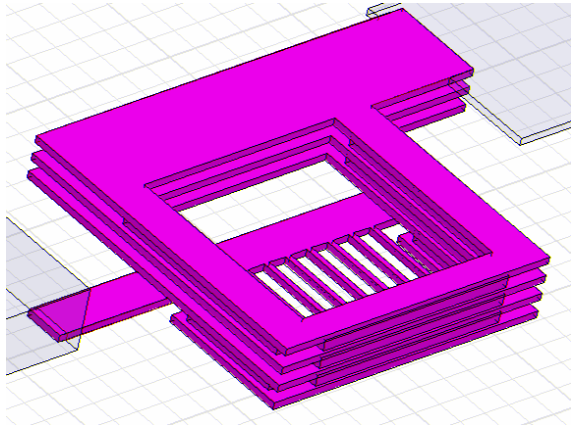
3D View



Top View

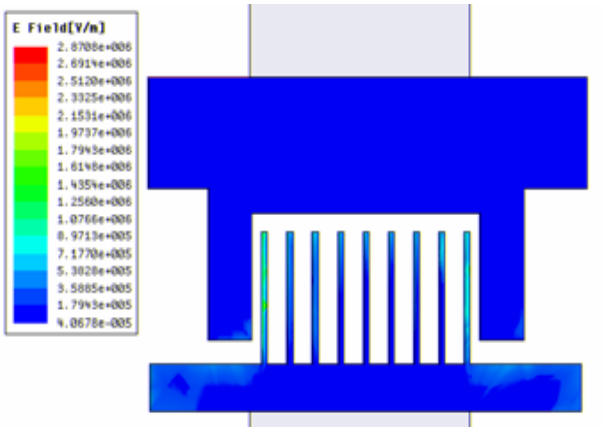


Side View

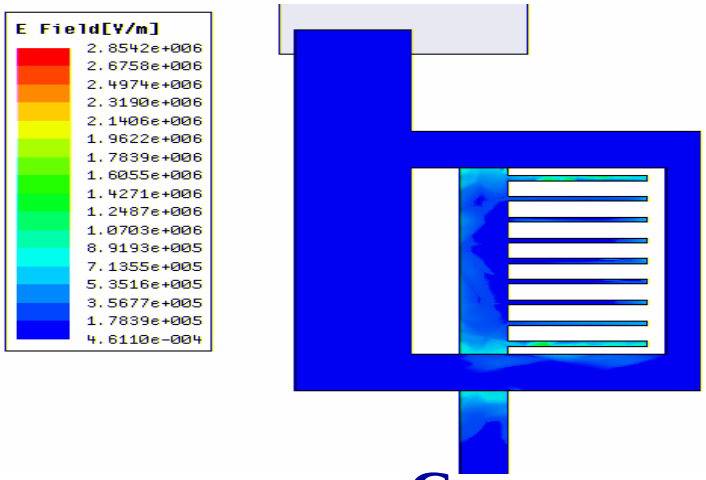


3D View

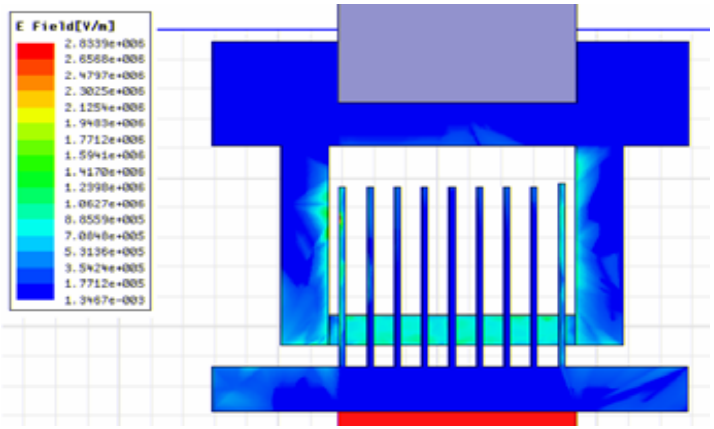
Back-End 3D-EM Simulation(cond't)



A_1



C_1



B_1

The parasitic effect between Base and Collector rounting in A_1 structure is insignificant.

The parasitic effect between Base and Collector rounting in B_1 structure is significant.

Device f_T and f_{max}

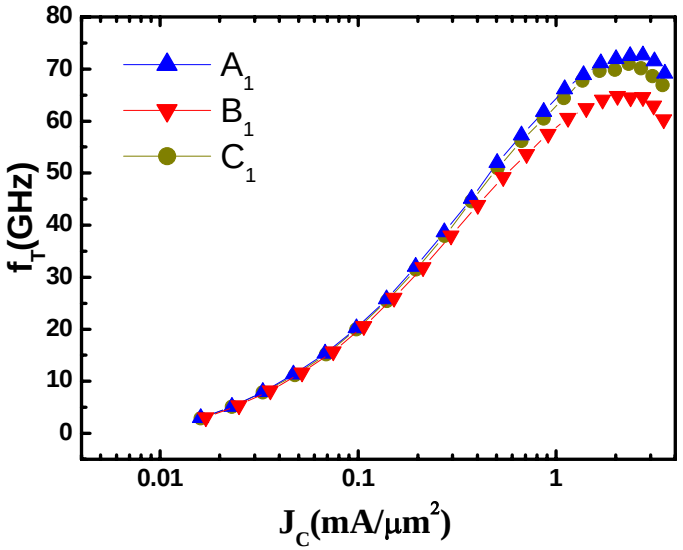
Total emitter-collector delay time

$$\tau_{ec} = \tau_b + \tau_c + \frac{\eta KT}{qI_C}(C_{BE} + C_{BC}) + (R_E + R_C)C_{BC} = 1/2\pi f_T \quad (1)$$

The well-known formula for maximum oscillation frequency

$$f_{\max} = \sqrt{\frac{f_T}{8\pi R_{BB} C_{BC}}} \quad (2)$$

Device f_T Performance



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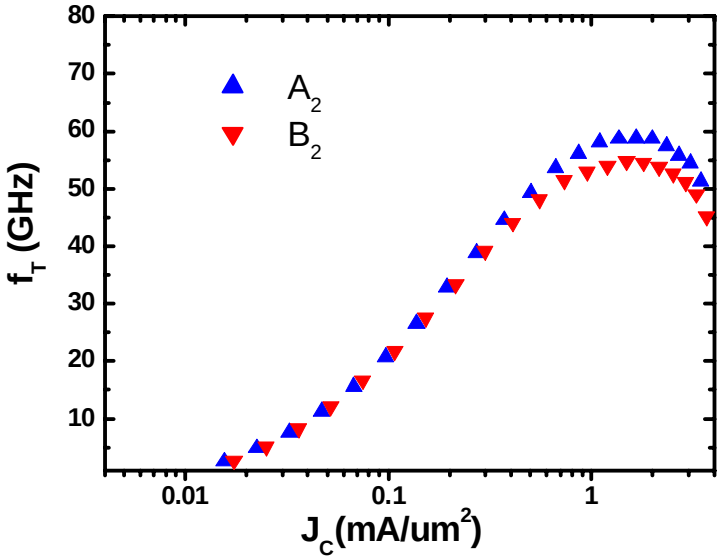


Fig. 2.

Measured cutoff-frequency vs. collector current density.

Device f_{max} Performance

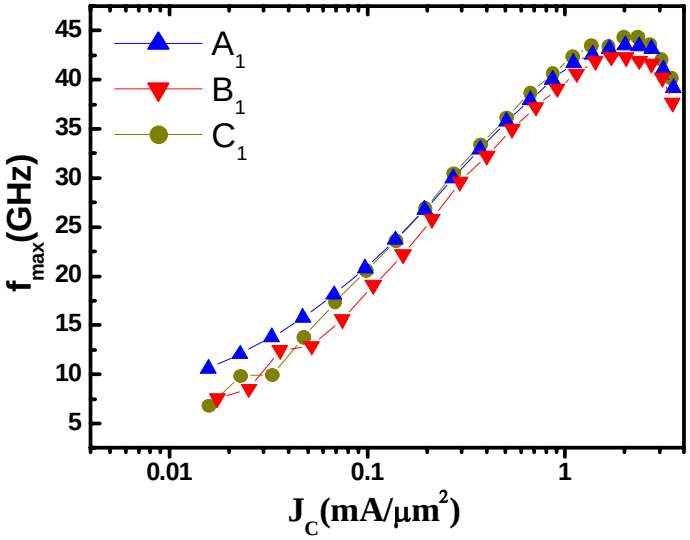


Fig. 1.

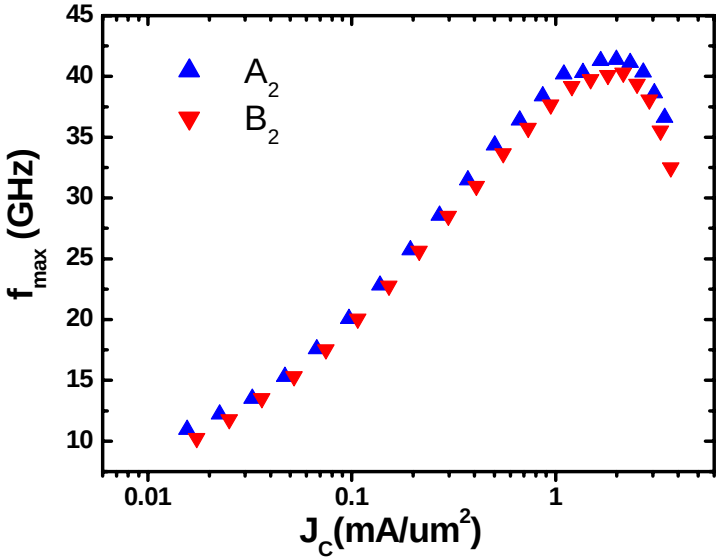
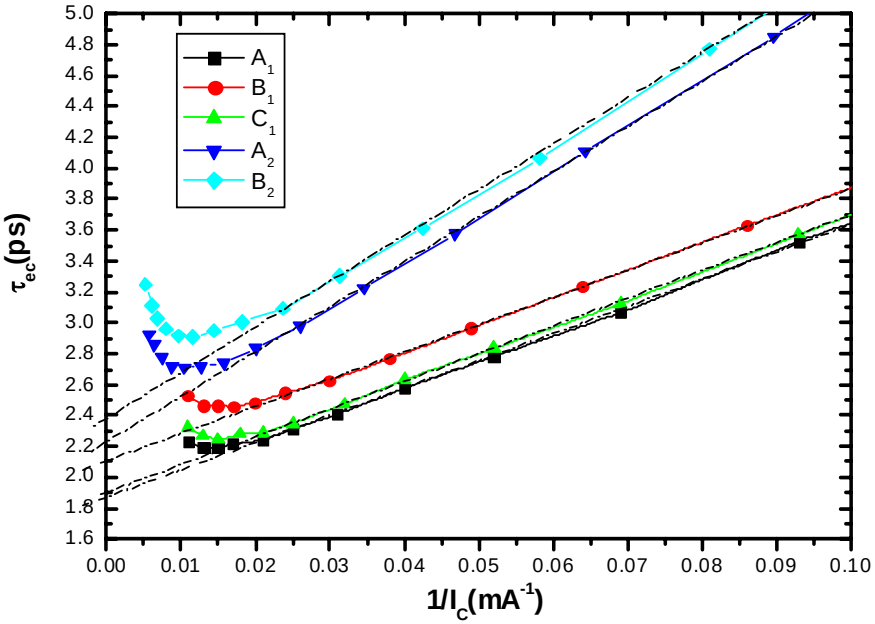


Fig. 2.

Measured maximum oscillation frequency vs. collector current density.

Device transit time extraction



SiGe HBTs	A_1	B_1	C_1	A_2	B_2
$\tau_b + \tau_c$ (psc)	0.946	1.063	0.935	1.153	1.374

Measured total emitter-collector delay time vs. inverse collector current.

$$\tau_b + \tau_c = \tau_{ec} - (R_E + R_C)C_{BC}$$ **At Intercept Point (1)**

RC Charging time

Performance summaries of SiGe HBTs with different layouts

SiGe HBTs	A_1	B_1	C_1	A_2	B_2
Emitter fingers	8	8	8	16	16
Base fingers	9	9	9	18	18
f_T(GHz)	73	65	71	59	55
f_{max} (GHz)	43	41	44	41	40

The perfromance of the f_T is significantly improved by 8 GHz higher for the slightly in layout arrangement.

Device equivalent components of SiGe HBTs with different layouts

SiGe HBTs	A_1	B_1	C_1	A_2	B_2
R_{BB} (Ohm)	11.68	11.09	11.36	6.31	6.45
R_C (Ohm)	5.53	5.68	5.58	3.53	3.46
R_E (Ohm)	1.19	1.23	1.27	0.73	0.68
C_{BC}(fF)	139.12	148.45	141.3	247.15	255.84

Both A_2 and B_2 structures are almost scalable with A_1 and B_1 structures.

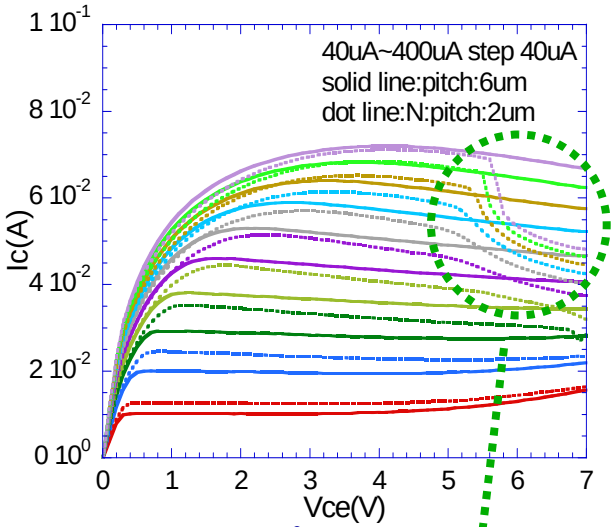
Transit time analysis of SiGe HBTs with different layouts

SiGe HBTs	A_1	B_1	C_1	A_2	B_2
Intercept (psec)	1.882	2.088	1.903	2.208	2.435
$(R_E+R_C)C_{BC}$ (psec)	0.936	1.025	0.968	1.055	1.061
$\tau_b + \tau_c$ (psc)	0.946	1.063	0.935	1.153	1.374

Status

The High Voltage standard unit-cell which can be applied in power cell for power amplifier design.

Multi-Emitter Thermal Simulation



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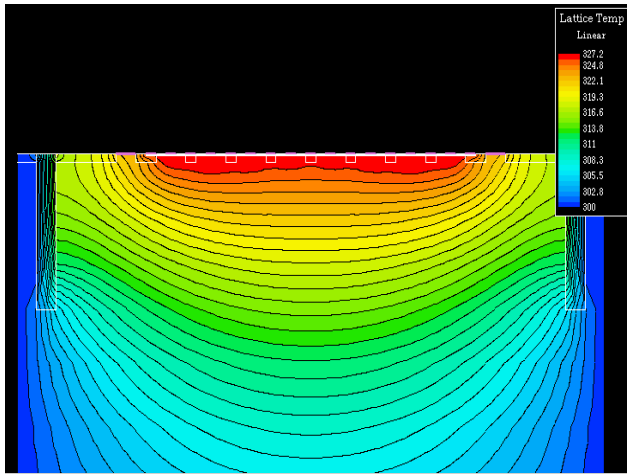

Fig. 2.

Current gain collapse for pitch=2μm device. Self-heating for device with pitch=2μm is much worse than that for device with pitch=6μm.

Conclusion

- We have analyzed the geometrical effects of parameters f_T and f_{max} of 0.18 μm high speed SiGe BiCMOS technology. The device scaling is feasible in the standard unit-cell.
- The key factor of the layout is the manner of overlap structure between the base fingers and collector traces. Although the smaller overlap of the base fingers in B_1, it gets proximity effect and eventually obtains more parasitic capacitances than those of C_1 and A_1.
- The high frequency performances are related with the associated parasitic junction capacitances C_{BC} and $\tau_b + \tau_c$. The significantly improvement in f_T is obtained by considering the routes in base and collector.
- The standard unit-cell can be applied in power cell for power amplifier design.