

# 28V High Efficiency High Linearity InGaP/GaAs Power HBT

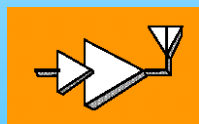
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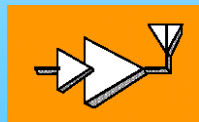
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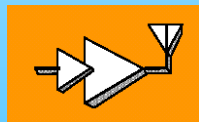


# Agenda

- Introduction
- 28V Operation InGaP/GaAs HBT Design
- Circuit Design and Assembly
- Experiment Results
- Conclusion



# Introduction



# 28V InGaP/GaAs HBT Power Transistor

## Background

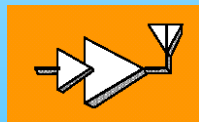
- The best InGaP/GaAs HBT designed for 3-8V operation achieved excellent linearity and  $10^{10}$  hours @  $T_j=150^\circ\text{C}$
- 28V HBT was demonstrated as a discrete device for higher power operation
- Flip chip was attempted to reduce thermal resistance

## EiC's Present Effort

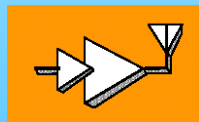
- Build MMIC compatible with existing assembly approach
- Design SOA (safe operation area) and ruggedness
- Provide high linearity

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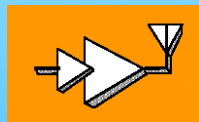


# 28V Operation InGaP/GaAs HBT Design

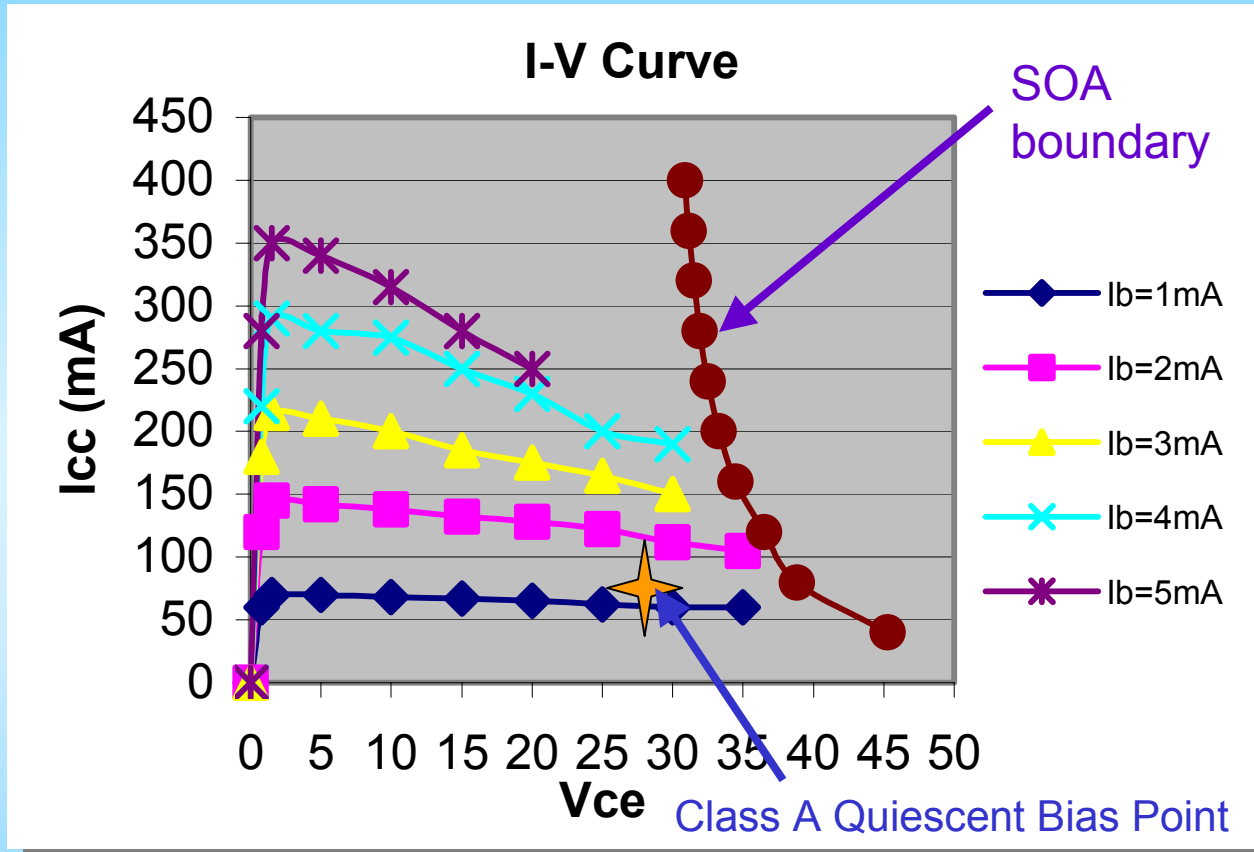


# Design of 28V InGaP/GaAs HBT

- $BV_{cbo} \sim 70V$ ,  $BV_{ceo} \sim 35V$
- Conventional 100 $\mu$ m thick substrate MMIC approach is adopted
- Thermal resistance design of HBT layout was done with proprietary program
- SOA (Safe Operation Area) through proper ballasting was designed with another proprietary program
- Initial “wafer level reliability” study result is very similar to the low voltage InGaP/GaAs HBT



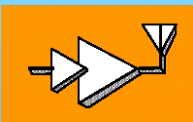
# Measured I-V Curve vs. Designed SOA for $A_e=1500\mu\text{m}^2$



Total Emitter Area  $1500\mu\text{m}^2$ . This is the building block for larger size HBT

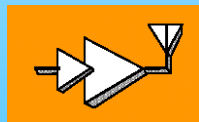
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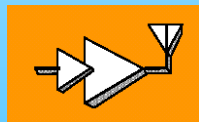
# Power HBT Design

- Multi-finger building block is paralleled in large size HBT
- Patented feed structure to provide minimum phase lag from the input feed to the HBT fingers and minimum variation of phase of RF signal at each finger



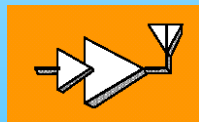


# Circuit Design and Assembly

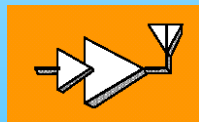
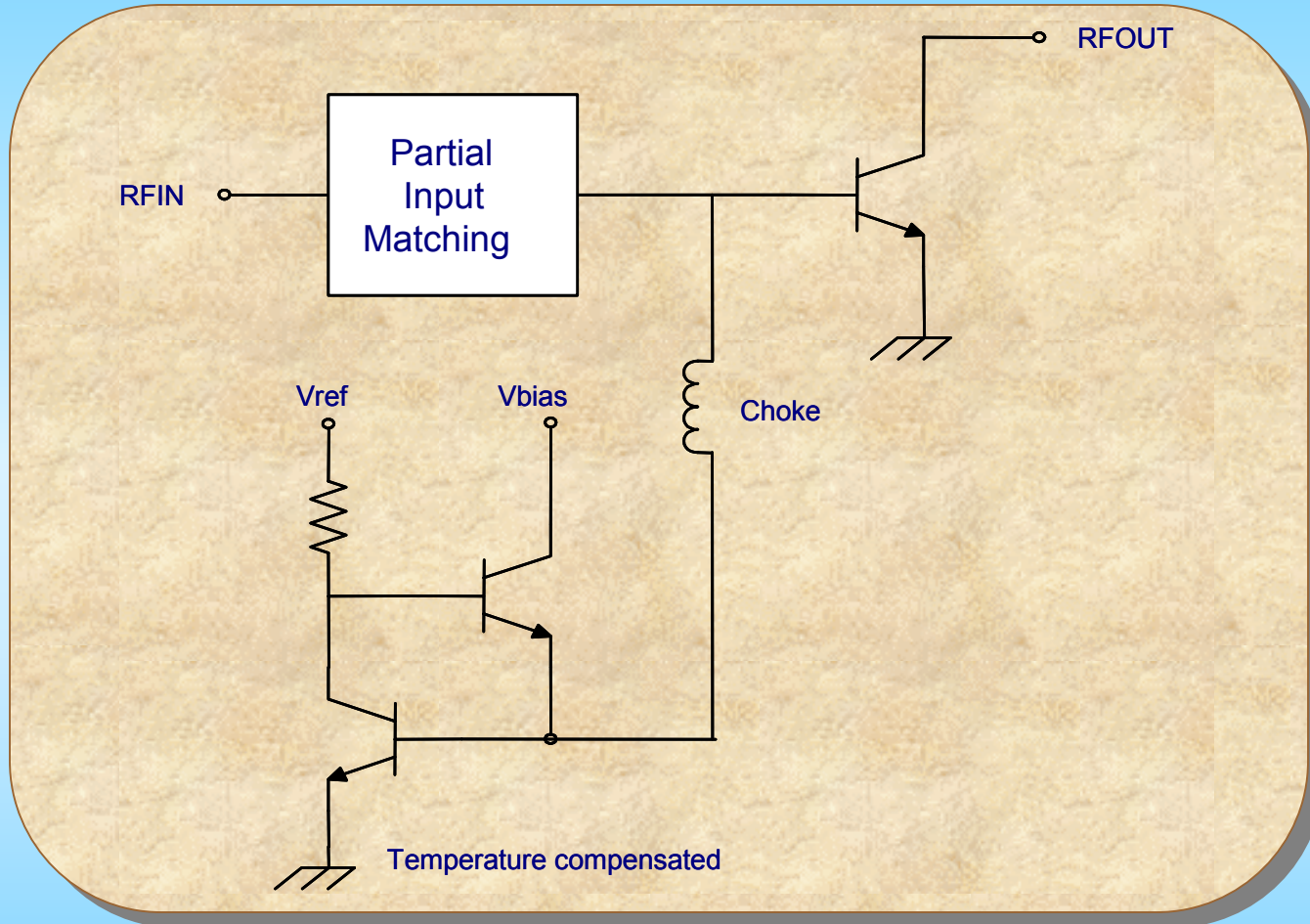


# On-chip Circuit Design

- Bias circuit (based on current mirror), RF choke and input pre-match circuit are designed on the same chip with the power HBT
- Temperature compensation is achieved through the current mirror
- Output matching is done off-chip
- Input matching is completed by off-chip matching

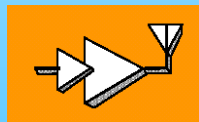


# Basic Circuit Design

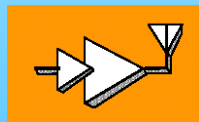


# Assembly

- Standard MMIC assembly procedure is followed:
  - The IC die is 4 mil thick
  - AuSn eutectic attachment is used
  - 1mil gold wire bond connects the die to the hybrid circuit
- No reliability concern about the assembly approach

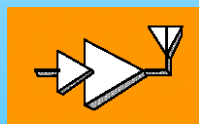


# Experiment Results



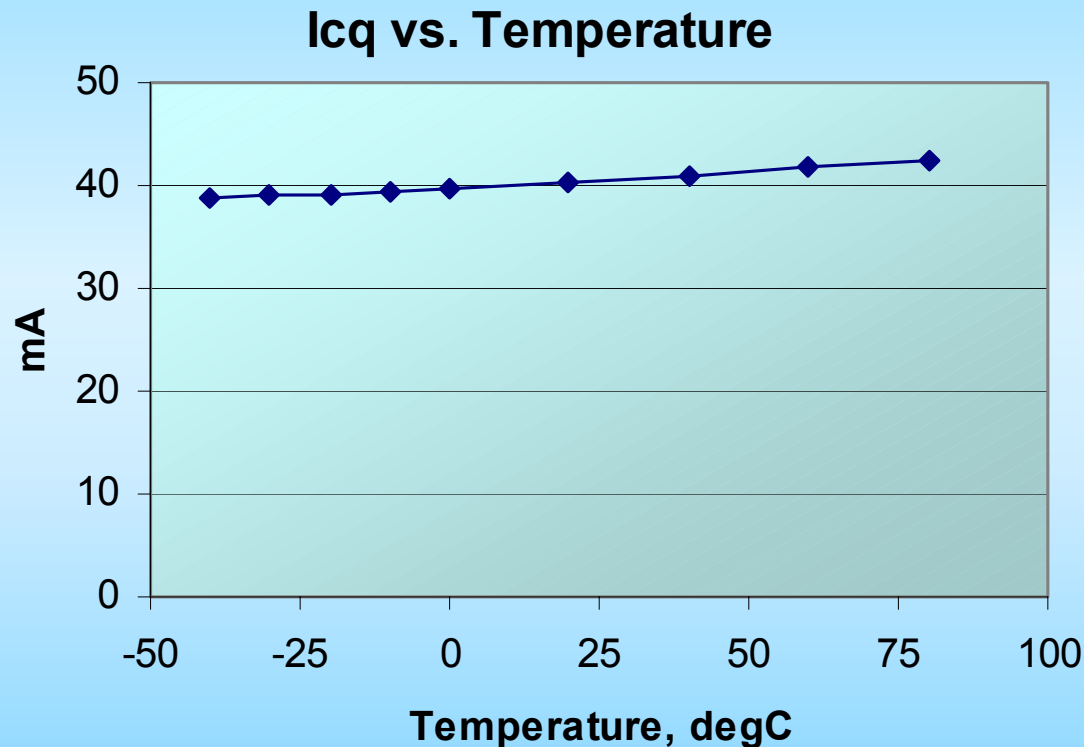
# Highlights

- Thermal resistance of 30-35°C/W was measured for the building block of  $A_e=1500 \mu\text{m}^2$  HBT
- Output power scales with HBT size to 25W at 900MHz, while maintaining the efficiency over 60%.
- Two tone test IMD3 maintains below -40dBc until reaching saturation power.
- At 900MHz under CDMA2000 9 fwr ch condition, 4.5W with  $\eta_c=42\%$  was measured with ACLR1=-45dBc / ACLR2=-58dBc, and 35% at ACLR1=-50dBc
- At 2GHz under CDMA2000 9fwr ch condition, 0.5W with  $\eta_c=32\%$  is achieved at ACLR1=-50dBc
- At 2GHz under WCDMA, 23dBm with  $\eta_c=18\%$  at ACLR1=-45dBc



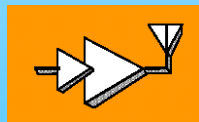
# Temperature Compensated Bias Circuit

❖ <9% change of  $I_{cQ}$  over  $-45$  to  $+85^{\circ}\text{C}$  range

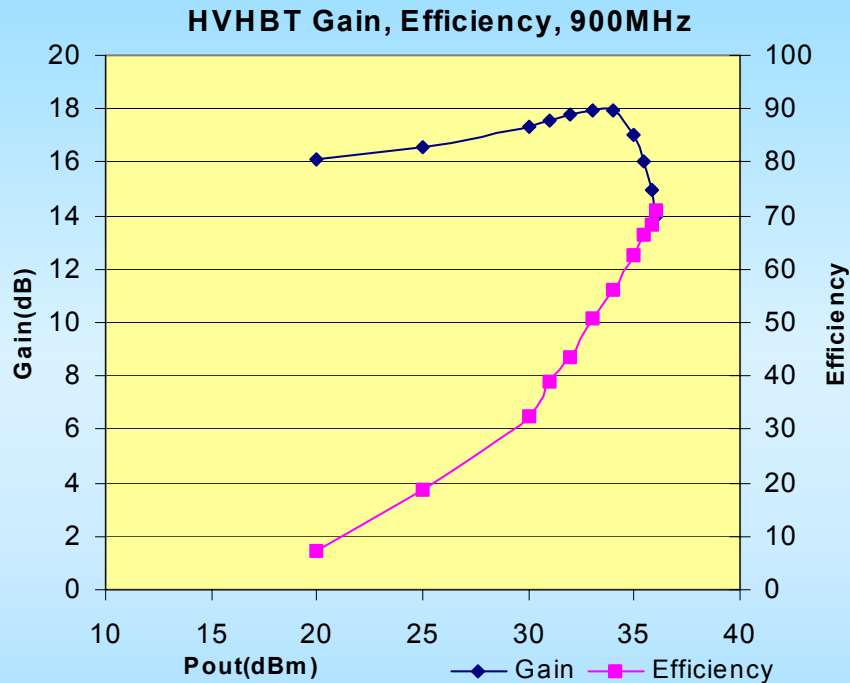


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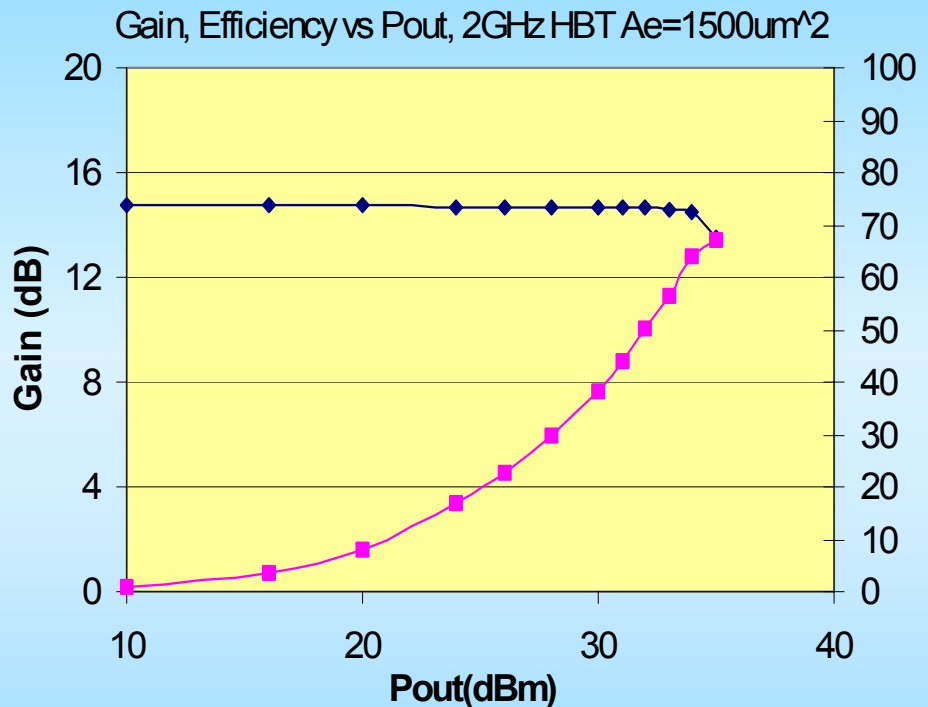
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# Gain / Efficiency of HBT with $A_e=1500 \mu\text{m}^2$



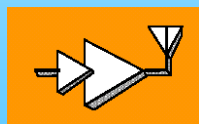
$P_{\text{out}}=36\text{dBm}$ ,  $G=14\text{dB}$ ,  $\eta_c=71\%$



$P_{\text{out}}=35\text{dBm}$ ,  $G=13.5\text{dB}$ ,  $\eta_c=67\%$

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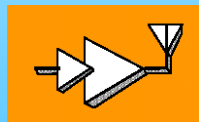
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# Thermal Resistance

- 30 to 35°C/W thermal resistance is measured from the HBT of  $A_e=1500\mu\text{m}^2$
- Measurement relies on the  $V_{be}$  vs. Temperature relationship
- At full power operation, temperature rise is 50°C

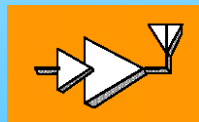


# Output Power vs. HBT Size @900MHz

Emitter size	1500	3000	6000	12000
Pout(dBm)	35	38	41	44
Gain(dB)	16.8	15.34	13.18	9.92
$\eta_c$ %	70	71	68	61

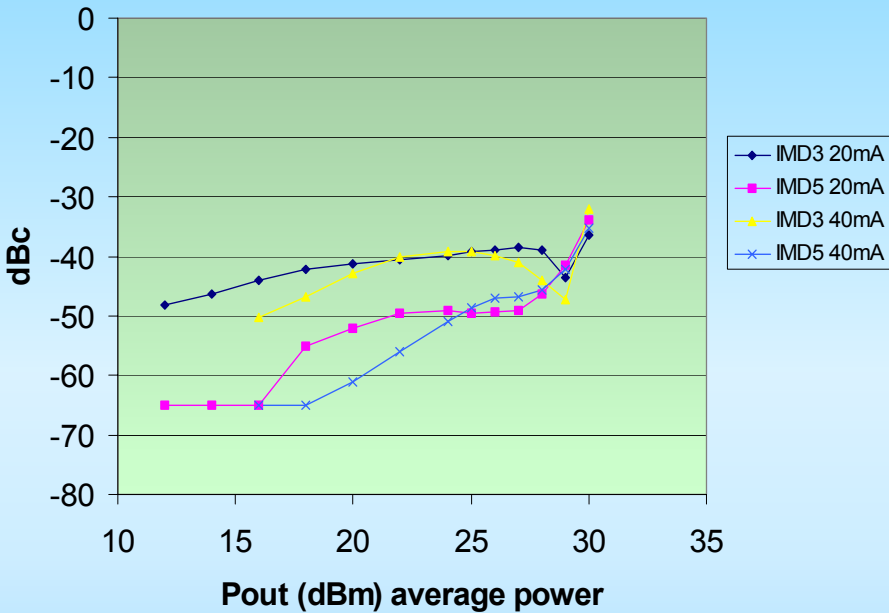
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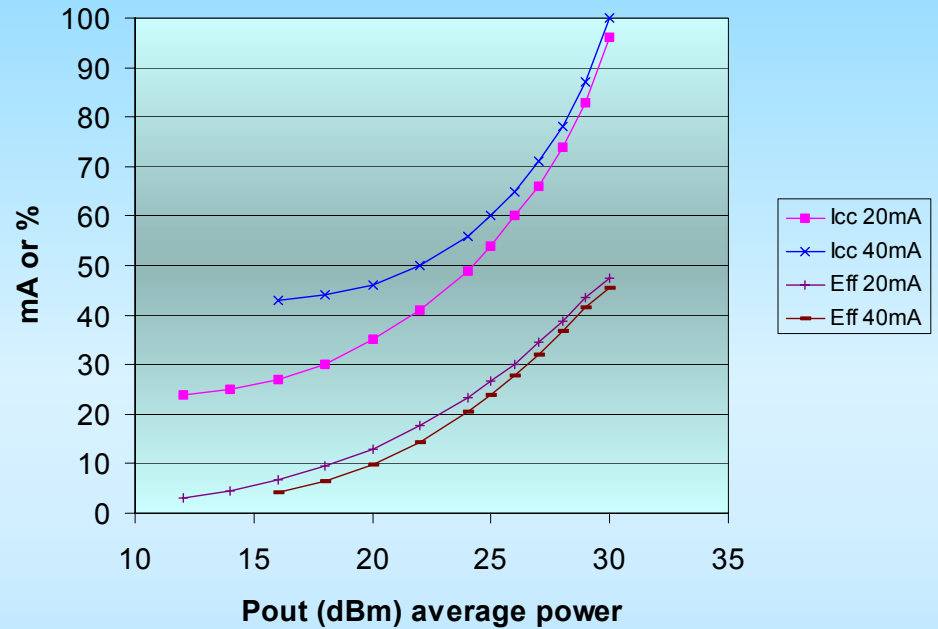


# Two Tone Test Result @ 2GHz

Two Tone Test @ 2GHz HBT Ae=1500



Two Tone Test @ 2GHz HBT Ae=1500



Single tone CW P1dB is 32.5dBm; Gss=13.2dB

Output power is average. Each tone power is 3dB lower; PEP is 3dB higher

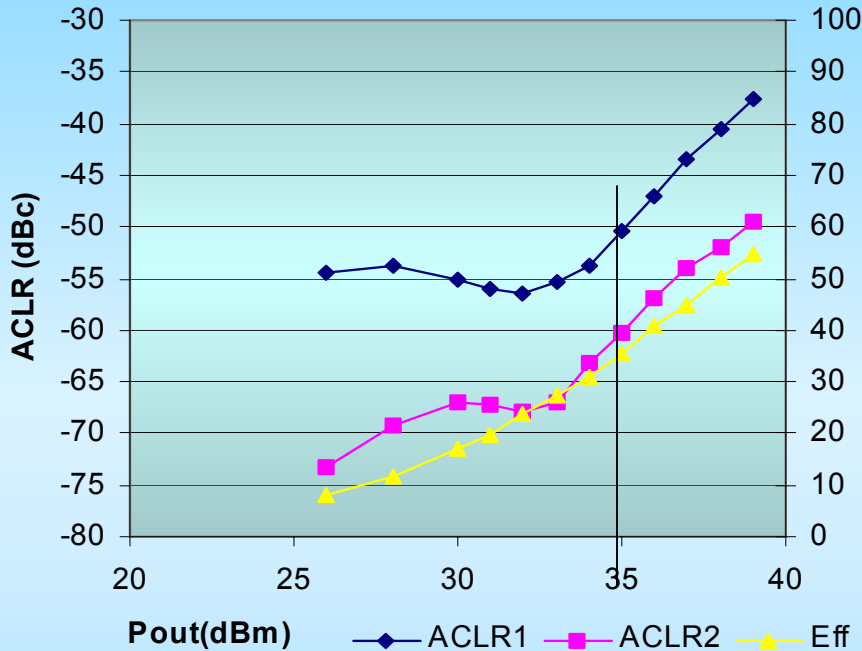
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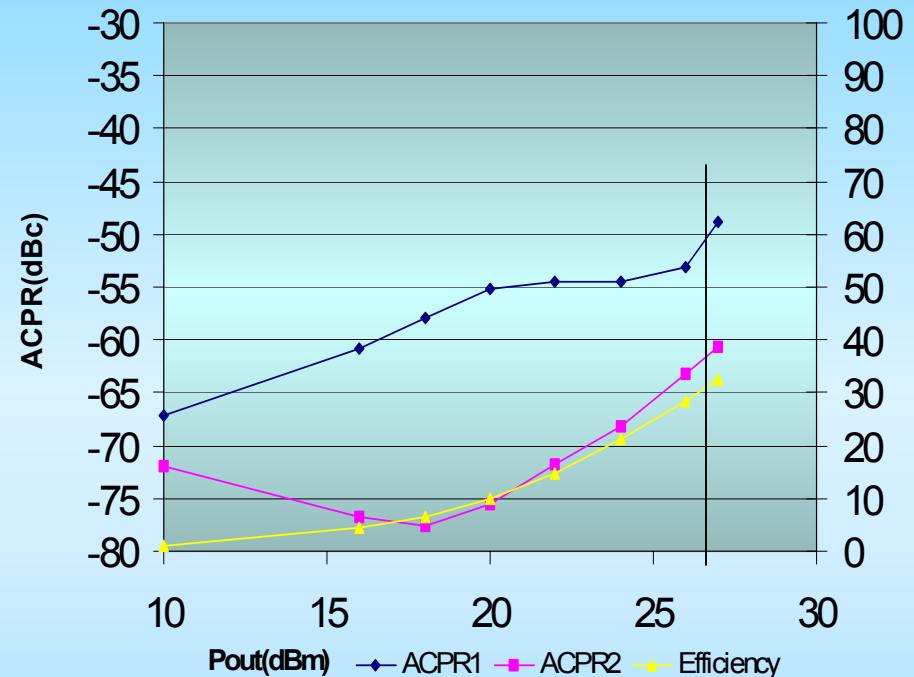


# CDMA2000 Test Result

HVHBT ACLR vs. Pout, Ae=6000, 900MHz



CDMA2000 ACPR vs Pout, 2GHz, HBT Ae=1500



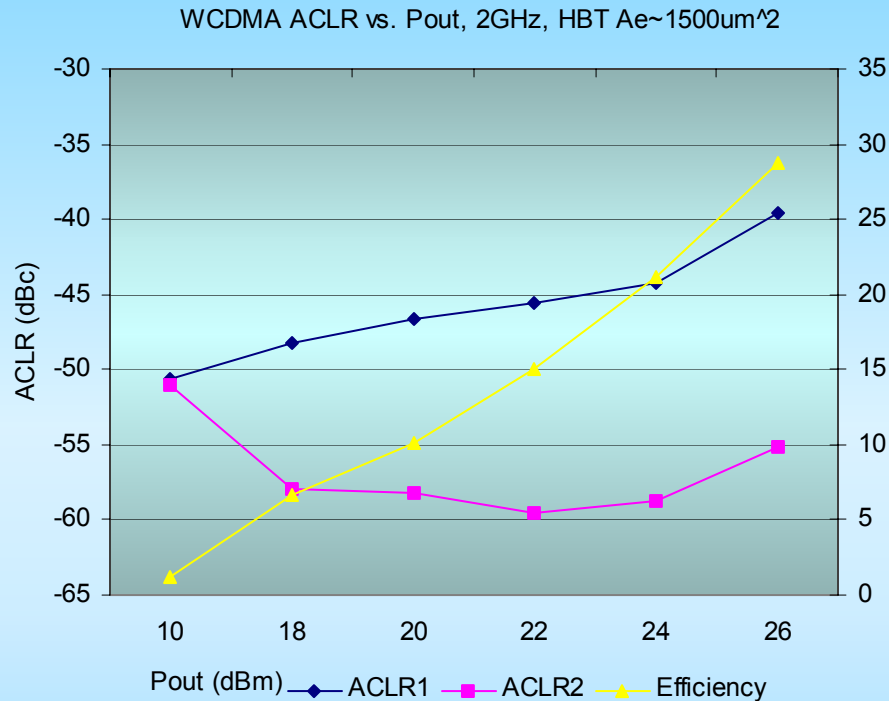
- Efficiency is 32 to 35% at ACLR1=-50dBc
- At 900MHz, 36.5dBm is achieved at ACLR1=-45dBc with 42% efficiency. 35dBm is achieved at ACLR1=-50dBc. HBT size is 4 building blocks.
- At 2000MHz, 27dBm is achieved with ACLR1=-50dBc from 1 building block.

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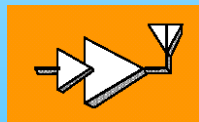
# WCDMA Test Method 1



- Peak to average ratio is 9.8dB
- P1dB is 32.5dBm
- At ACLR1=-45dBc, Pout is 23dBm with 18% efficiency

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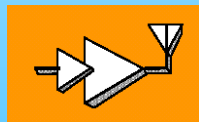
# Conclusion

## Key Advantages

- InGaP/GaAs HBT achieves high efficiency: over 60% at 2GHz
- Excellent linearity under modulated signals
- Long lifetime and stable gain is expected from the standard InGaP/GaAs HBT result

## Major Achievement

- 25W is achieved in the standard MMIC approach
- InGaP/GaAs HBT can be further developed to serve the high power / high reliability applications



# Acknowledgment

- The authors like to thank Mr. Jerry Curtis for his encouragement
- Many colleagues' invaluable support on this project is also acknowledged here

