Advanced Architectures for Predistortion Linearization of RF Power Amplifiers

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Presented at
The IEEE Topical Workshop on Power Amplifiers
September 9, 2002
La Jolla, CA

Acknowledgement

- This work was supported in part by Danam USA, San Jose, CA.

  and by

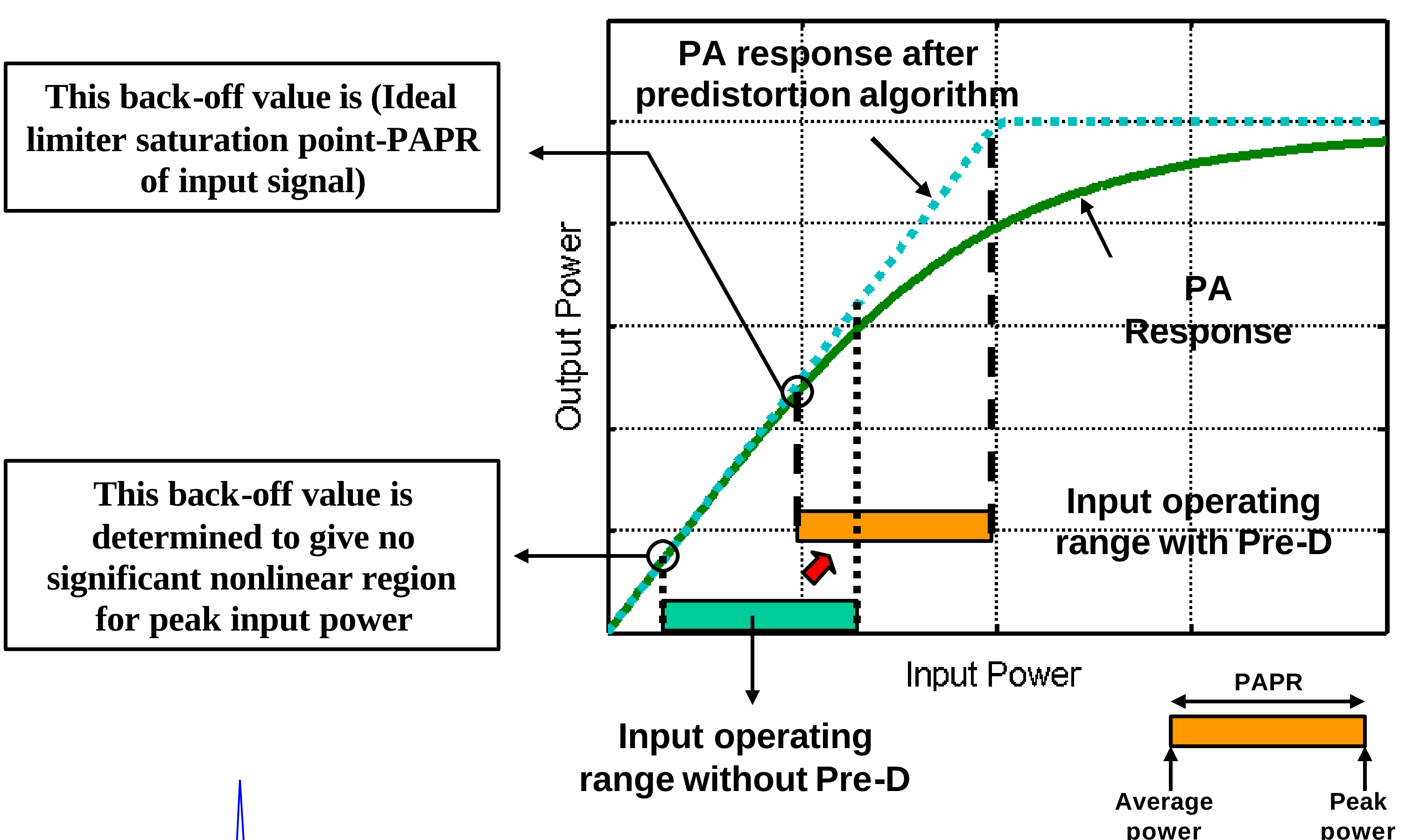
- The Yamacraw Design Center, an economic development project funded by the State of Georgia.

- Thanks also to Sirenza Microdevices, and Ericsson USA for donating the power amplifiers used in this study.

Outline

- Introduction to Predistortion
- LUT Updates using Sub-sampling Receivers
- RF Envelope Predistortion
- Summary and Conclusions

Predistortion Concept



Correction Techniques for Cellular Base Stations

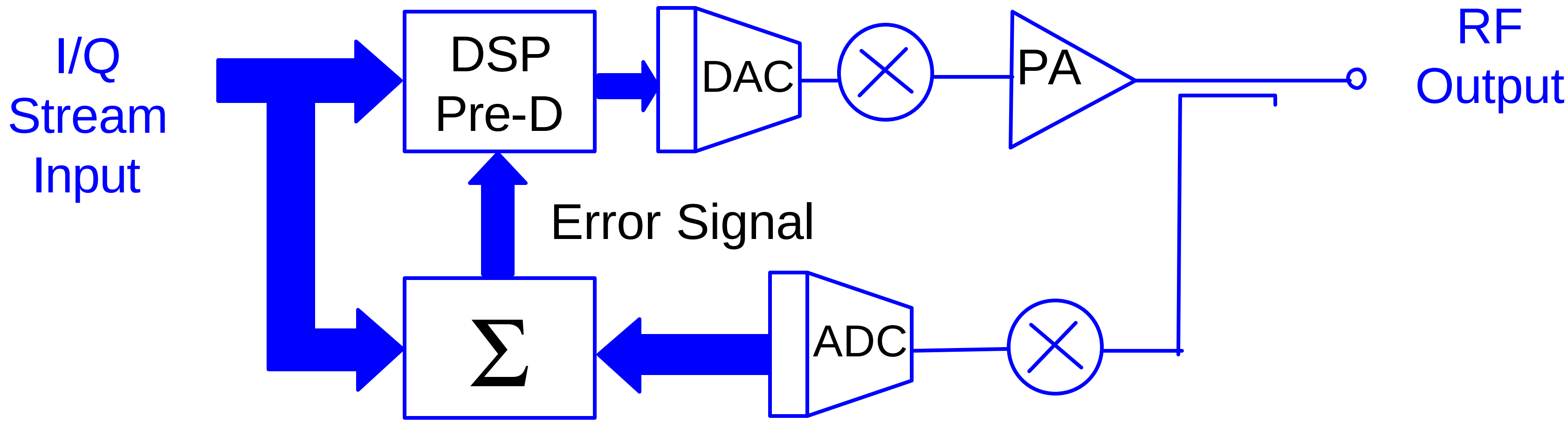
Correction Technologies	Correction Capability*	Correction Bandwidth	Relative Cost
Feed Forward	25-35 dB	> 100 MHz	High
Envelope Feedback	10-20 dB	< 5 MHz	Med
Analog Pre-Distortion	5-10 dB	> 25 MHz	Low
Adaptive Pre-D	10-20 dB	> 50 MHz	Med

* IMD Correction based on 8-Tone Continuous Random Phase

Predistortion Linearization

Predistortion Technology	Bandwidth	Relative IMD Correction	Comments
Open Loop Analog Pre-D	High	Low	Simple Implementation
Adaptive Analog Pre-D (Work function)	Moderate	Moderate	No I/Q stream required
Digital Baseband Pre-D	Moderate	Good	Depends on DSP computational capability

Baseband Pre-Distortion



- Adaptive Filter to Minimize MSE
- ADC/DAC Requirements:
  - 20 MHz BW $\Rightarrow$ 100 MHz with 5th order IMD
  - 3X over sample $\Rightarrow$ 300 Msps (on both I and Q)
- DSP Speed: >6·10^8 MAC/sec
  - 0.18 µm CMOS: ~1.5 nW/MAC
  - $\Rightarrow$ ~1W DC power
  - LUT update must also be performed

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Trends in Analog-to-Digital Converter Technology

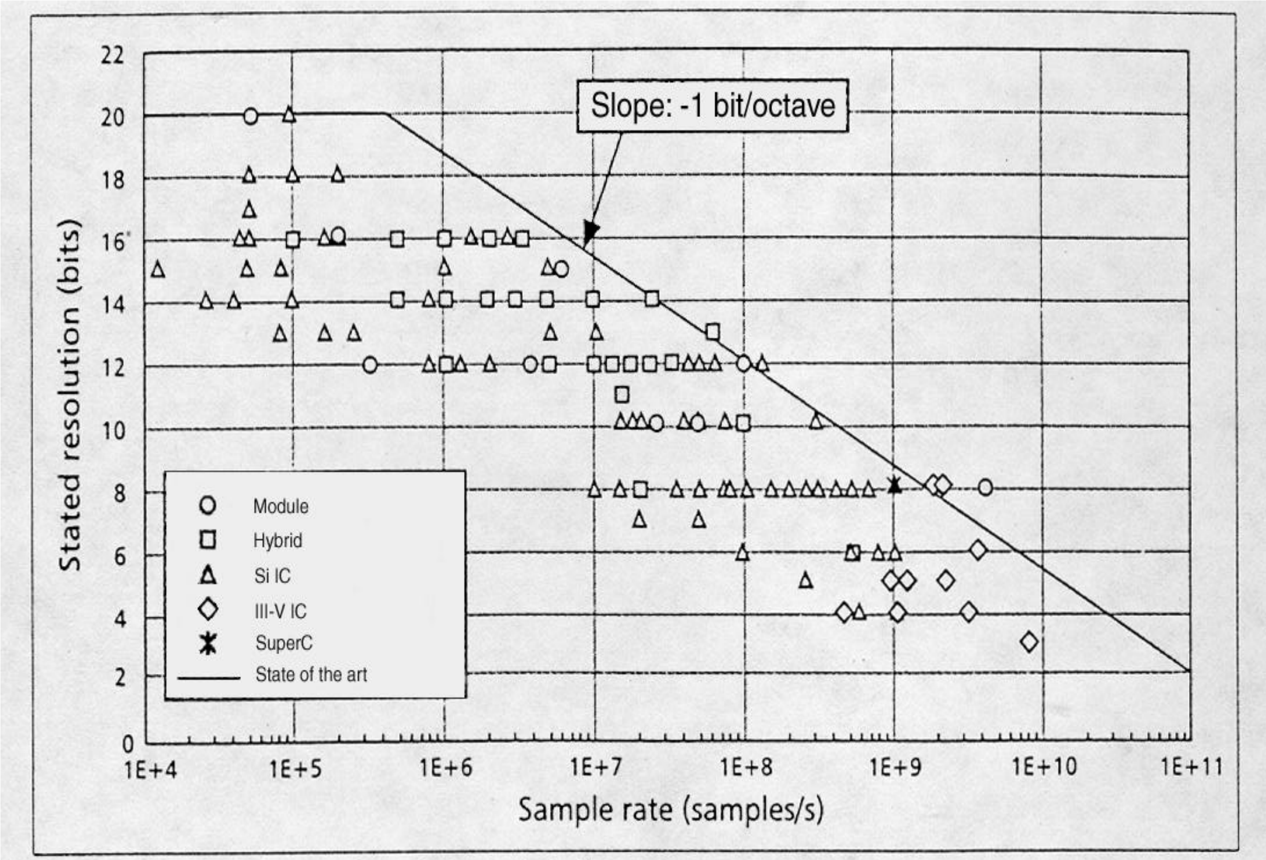
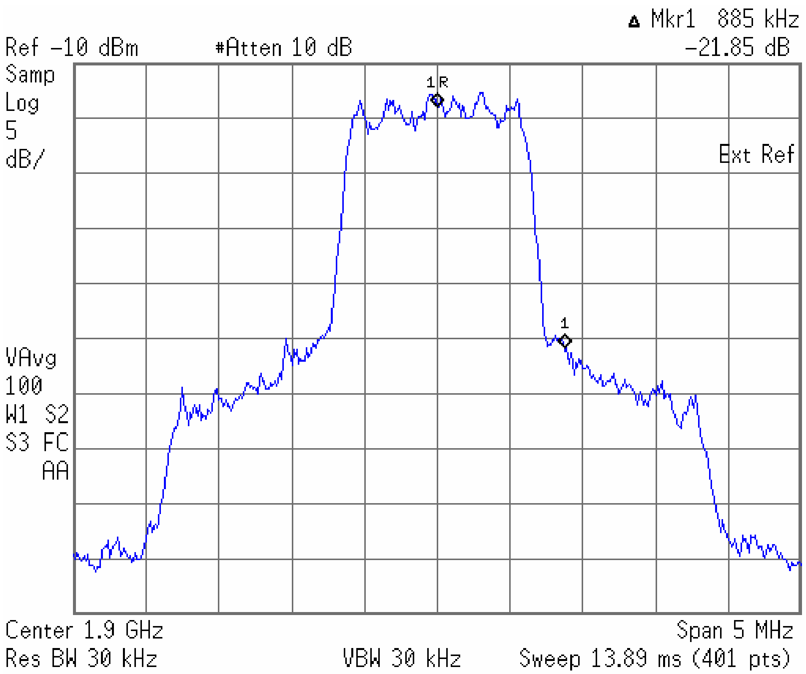


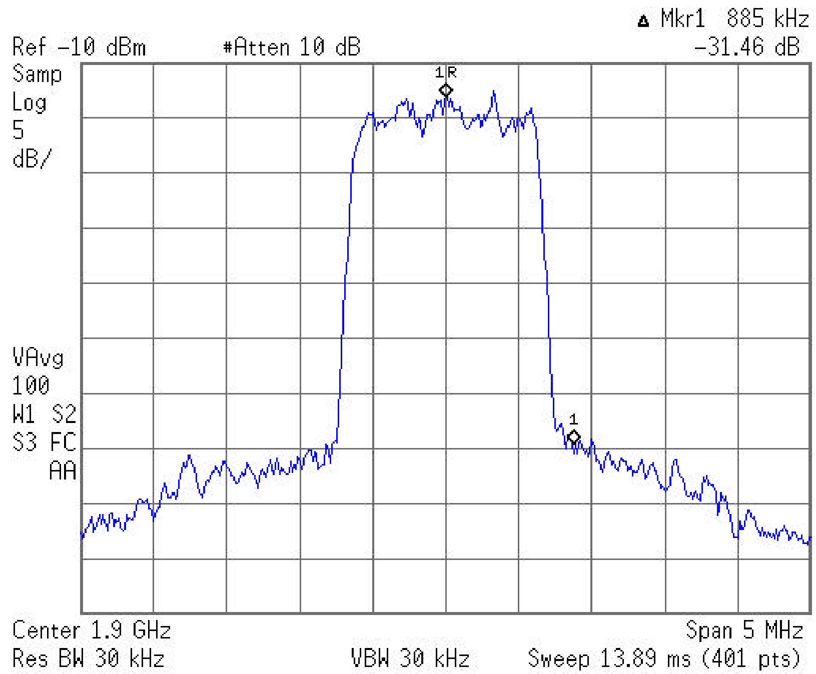
Figure 1. *A survey of analog-to-digital converters.*

Adapted from R. H. Walden, *Performance Trends for Analog-to-Digital Converters*, IEEE Communications Magazine, February 1999, pp. 96 - 101.

Pre-D Results with Low Power Amplifier
(0.5W Class-AB GaAs HFET)



Without Pre-D



With Pre-D

Disadvantages of Baseband Pre-D

- Sampling Requirements
- DSP speed (power)
- Digital I/Q input stream required
- LUT update must be performed in background

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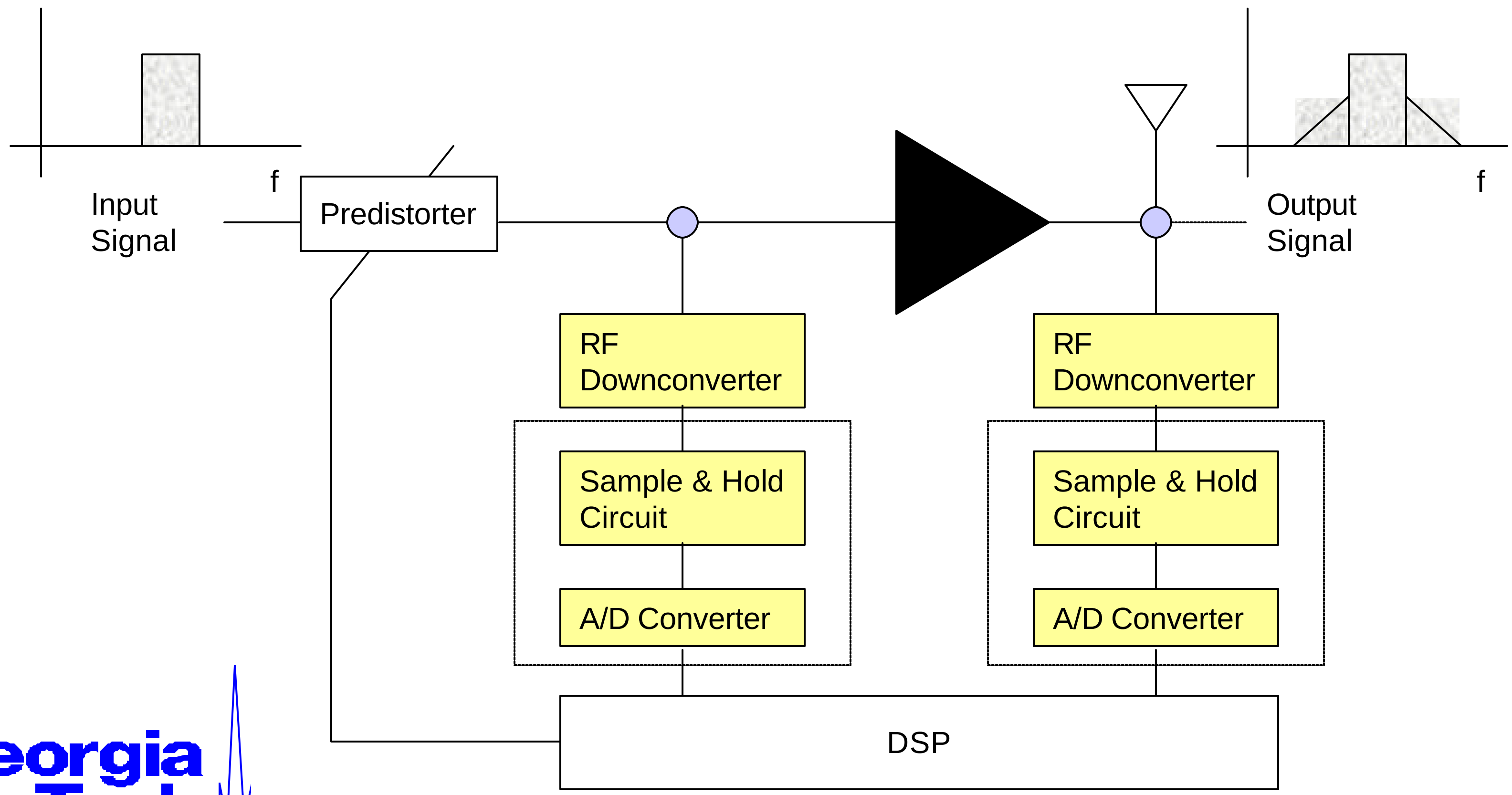
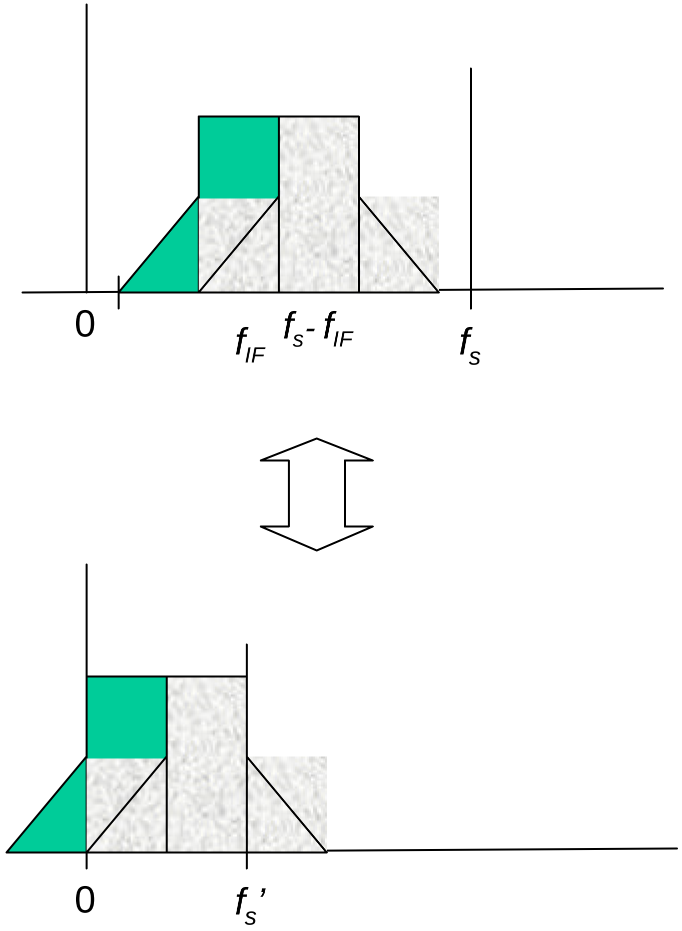
Sampling in Predistorters

- A predistorter samples signals at the input and output of a power amplifier to identify its AM-AM, AM-PM characteristics.



Input Nyquist Rate

- Input Nyquist rate is when
  f_{IF} +BW/2=f_s-f_{IF} – BW/2
- Again, this is equivalent to the second figure in terms of aliasing
- Therefore, this is 33% of the output Nyquist Rate, considering 3rd order IMD.

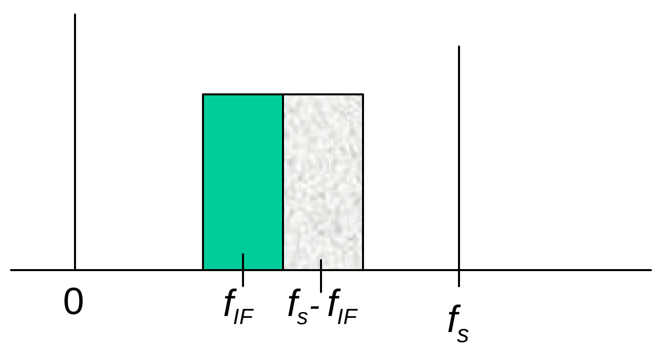


Input Nyquist Rate

- The original signal can be reconstructed from the sampled signal if the signal is sampled so that its spectrum is not overlapped in frequency domain.

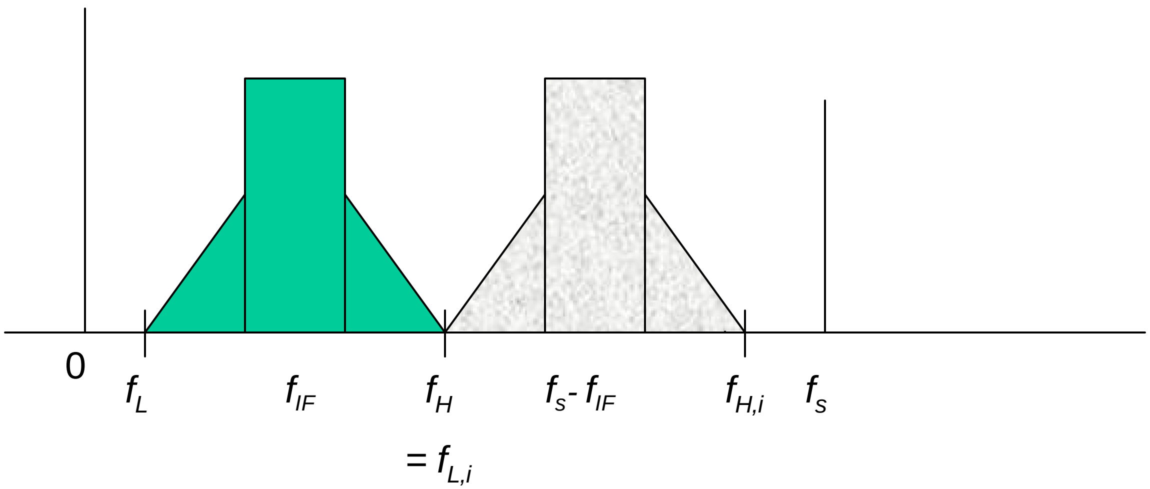
$$x(t) = \sum_{k=-\infty}^{\infty} x(kT_s)\frac{\sin[p(t-kT_s)/T_s]}{p(t-kT_s)/T_s} \qquad \text{where} \qquad \frac{1}{T_s} = F_s \geq 2F_o$$

- Input Nyquist rate is the sampling frequency when the highest frequency of the input signal coincides with the lowest frequency of the image signal.

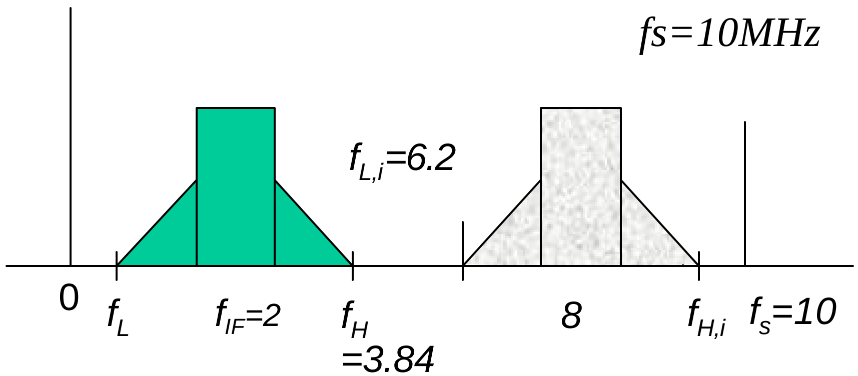


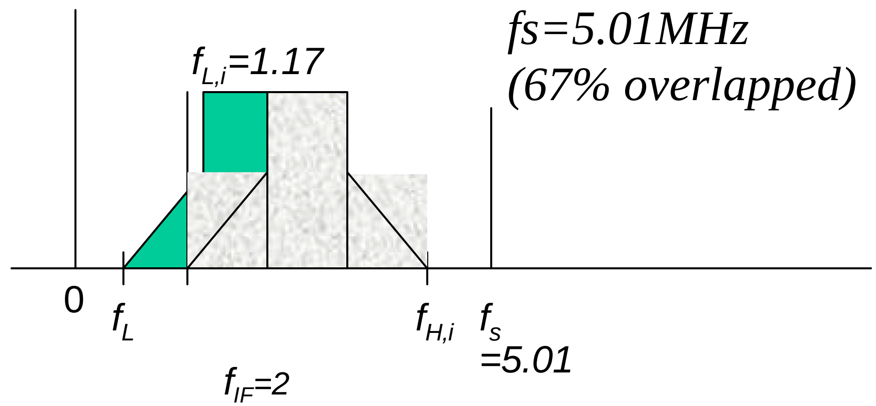
Output Nyquist Rate

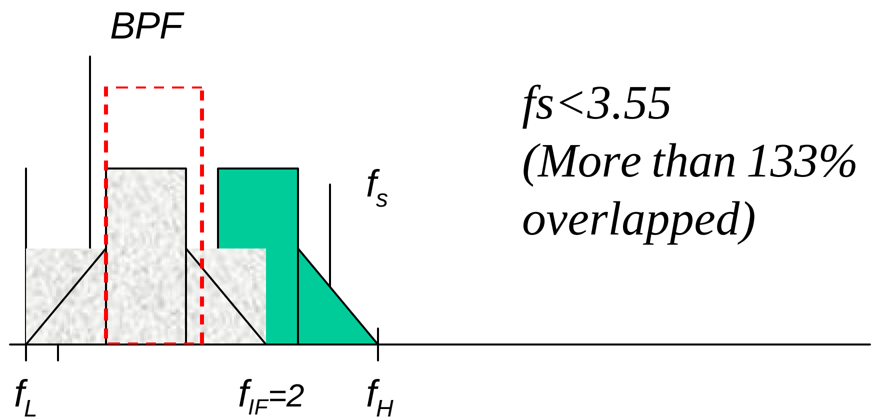
- With predistortion systems, the analog-to-digital conversion at the output of a PA is traditionally done with 'above' Output-Nyquist rate in order to avoid the aliasing at the output spectrum.



Sub-sampling





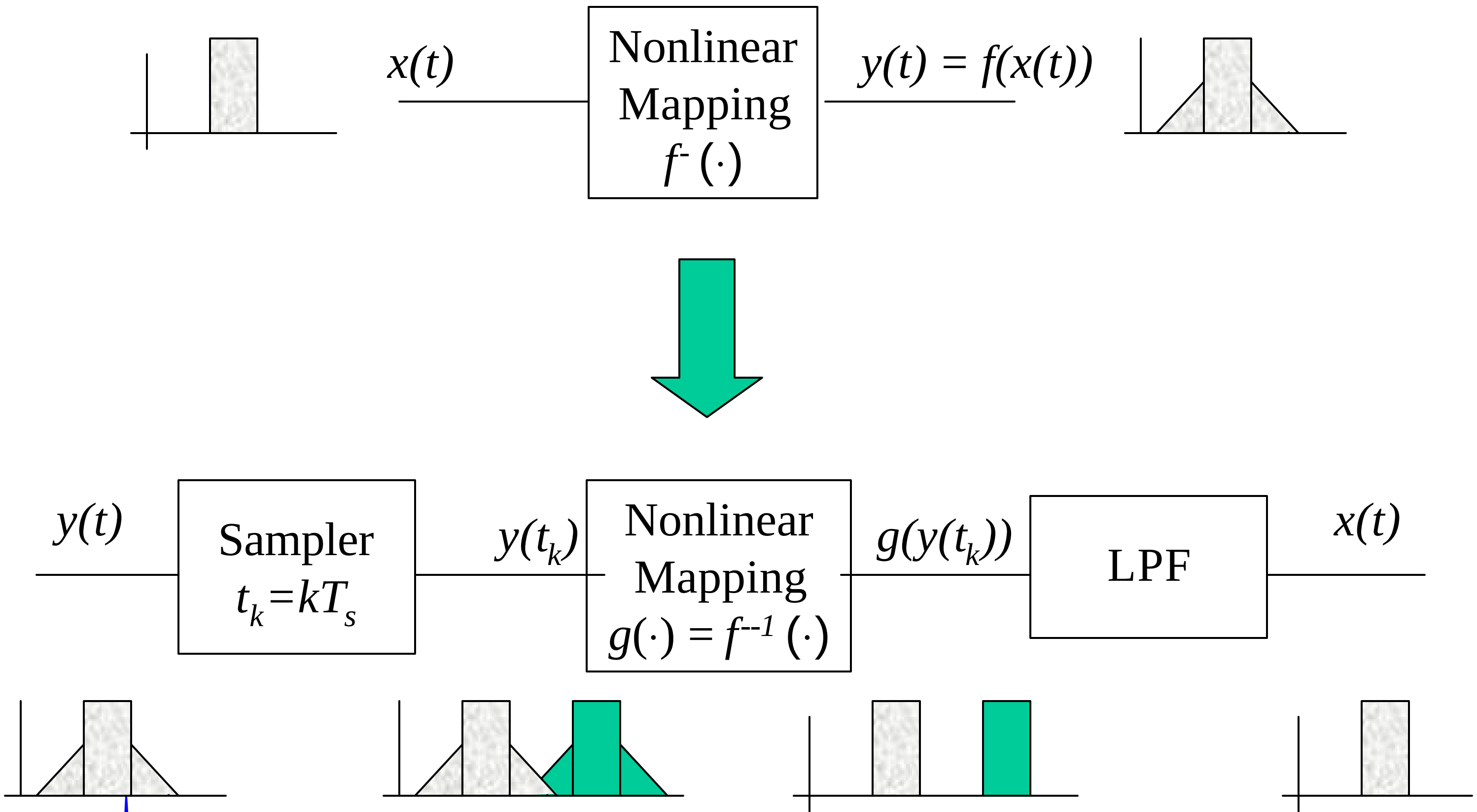


Sampling Requirements for Nonlinear System Identification

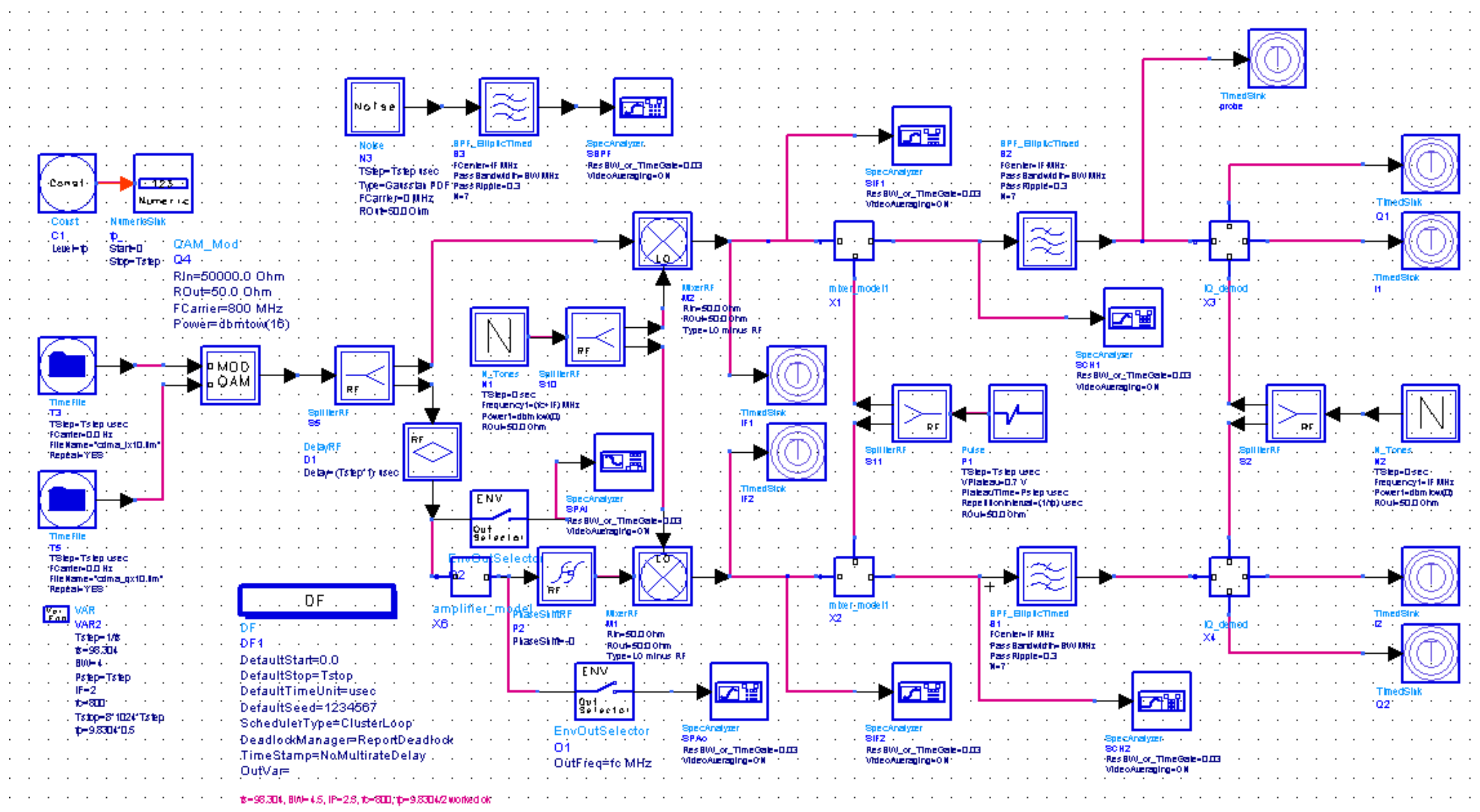
- The goal of the sampling system is the pre-D system is not to reconstruct signals, but to identify the nonlinear distortion.
- Therefore, it is not necessary to do Nyquist rate sampling.
- According to the Generalized Sampling Theorem*, a nonlinear system may be accurately identified if the output signal is sampled at the *input* Nyquist rate.

*John Tsimbinos, and Kenneth V. Lever, "Sampling Frequency Requirements for Identification and Compensation of Nonlinear Systems," *in Proc. ICASSP*, vol. III, 1994, pp. 513-516.

Basic Operation of the Generalized Sampling Theorem



Sub-Sampling Architecture
ADS Simulation



Sub-Sampling Architecture
ADS Simulations (cont.)

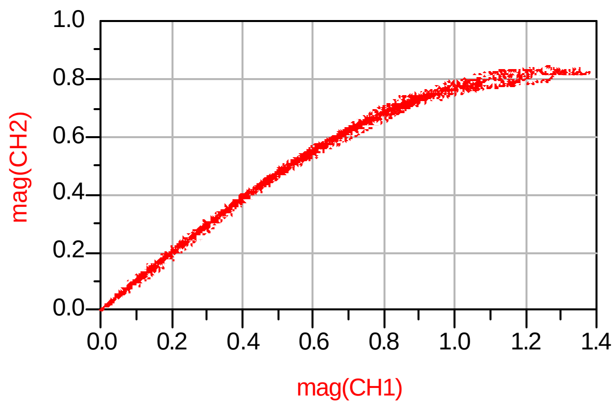


Figure 1: Simulated AM-AM Characteristic when f_s = 10 MHz (includes 3[rd] order distortions).

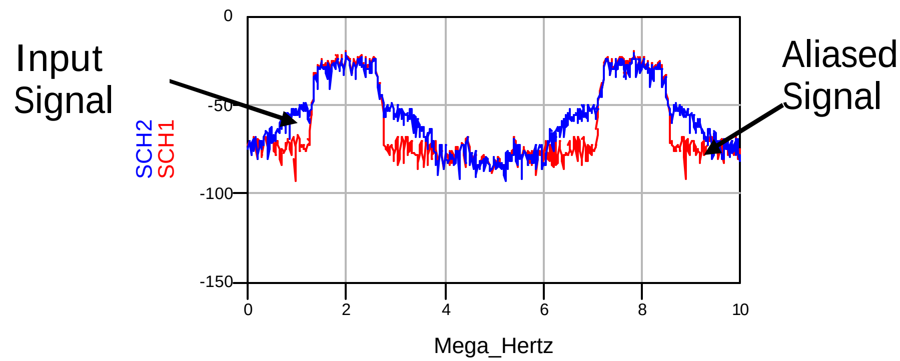


Figure 2: Frequency Spectrum when f_s = 10 MHz (includes 3[rd] order distortions).

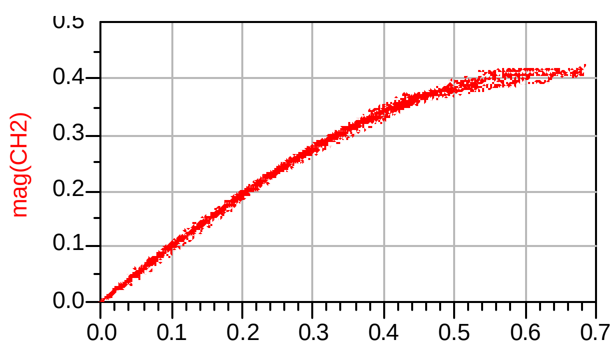


Figure 3: Simulated AM-AM Characteristic when f_s = 5 MHz (70% of output spectrum is overlapped).

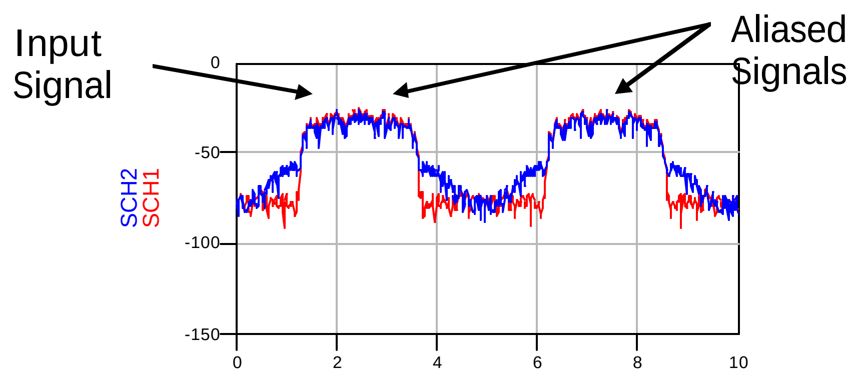
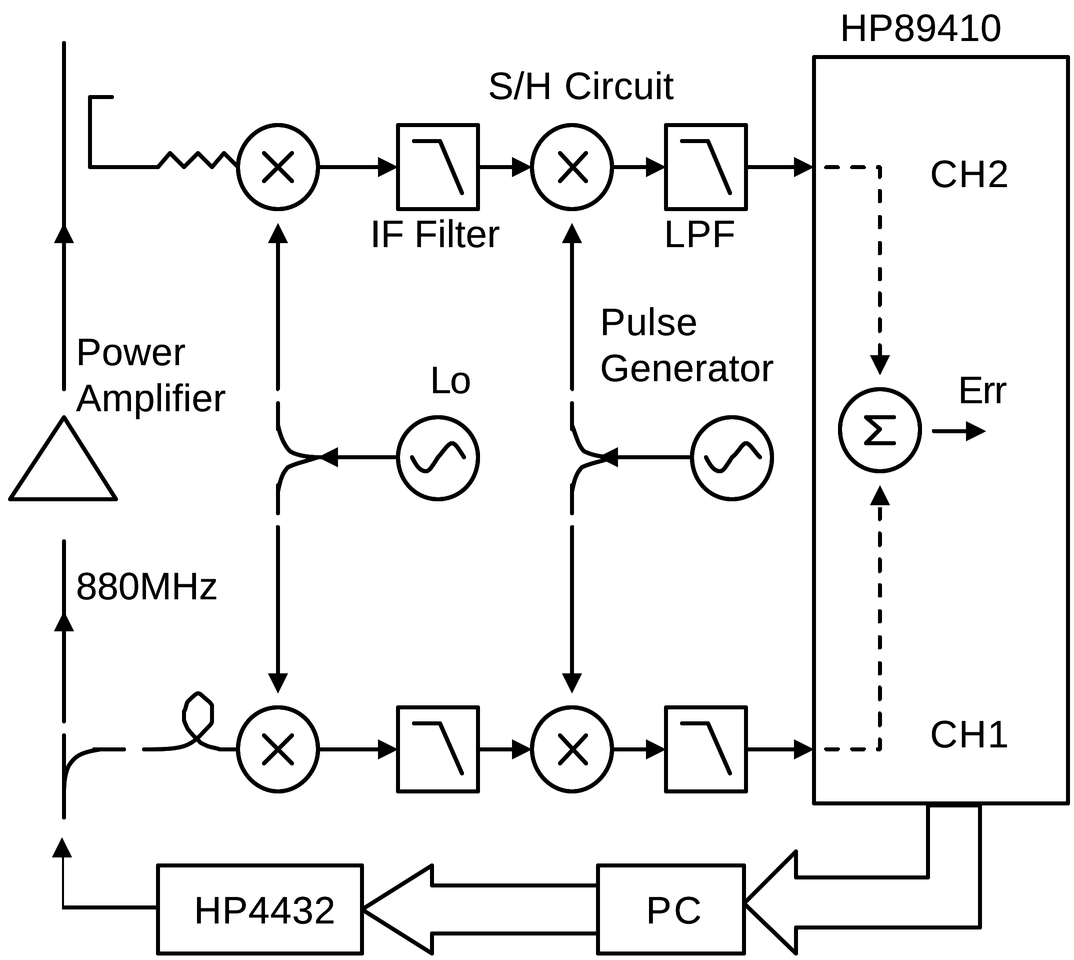


Figure 4: Frequency Spectrum when f_s = 5 MHz (70% of output spectrum is overlapped).

Sub-sampling Architecture Test Bed



Measurement Results

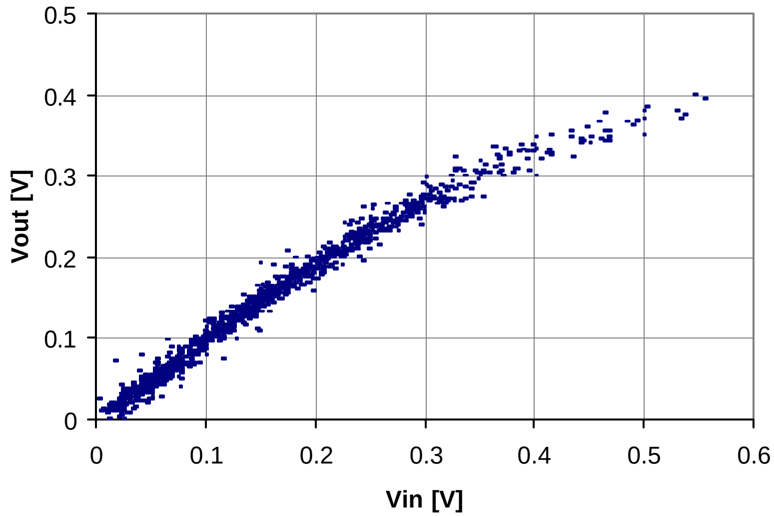


Figure 6: Measured AM-AM Characteristic of SHF-0189 when f_s = 10 MHz (includes 3rd order distortions).

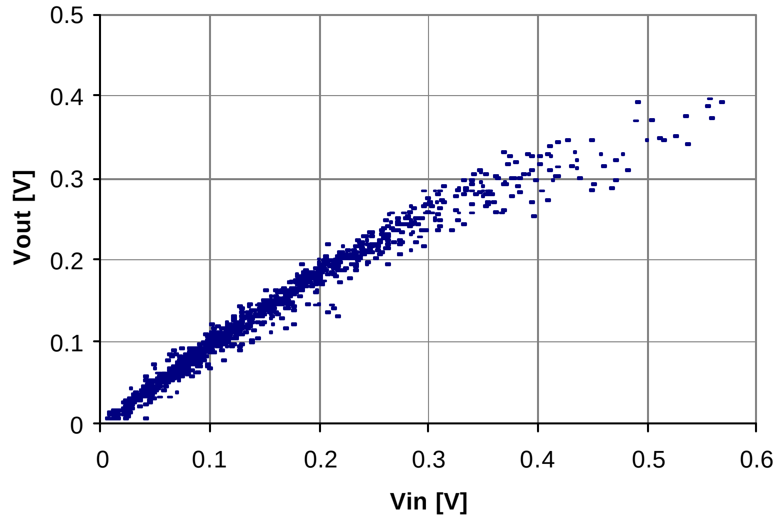
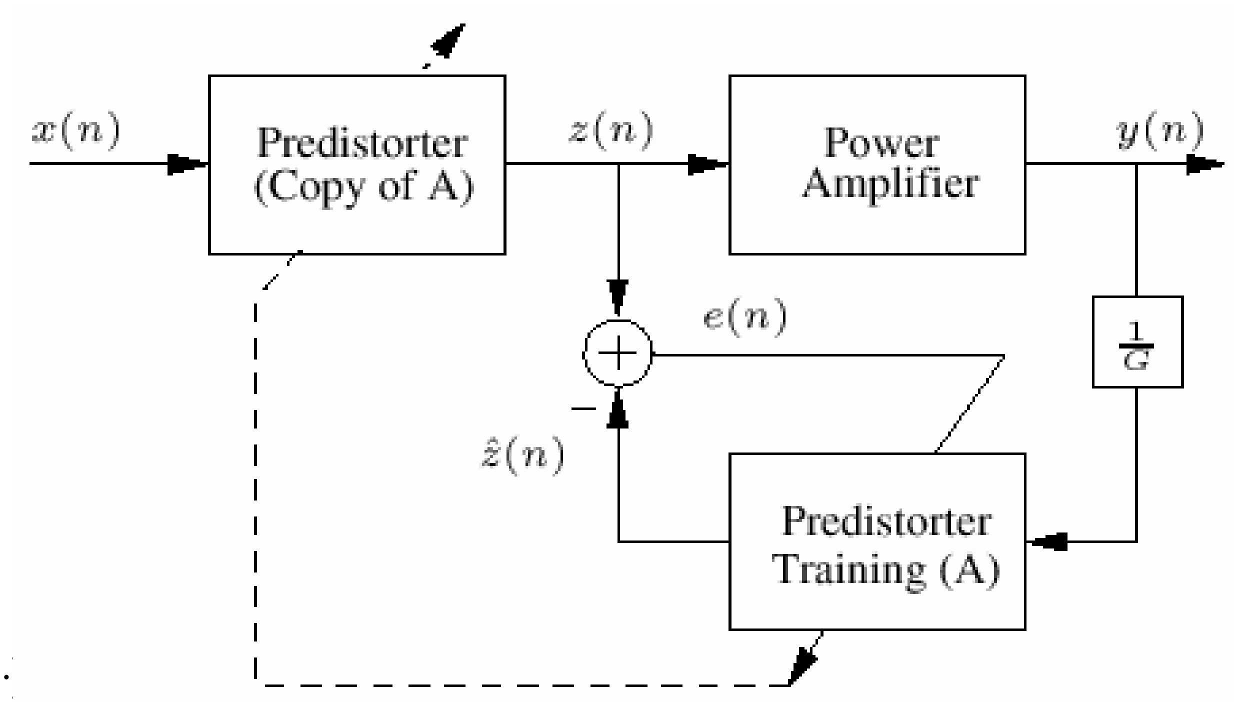


Figure 7: Measured AM-AM Characteristic of SHF-0189 when f_s = 5.3 MHz (67% of output spectrum is overlapped).

Indirect Learning Predistortion Architecture



Basic Algorithm :

$y(n) = f(z(n))$,

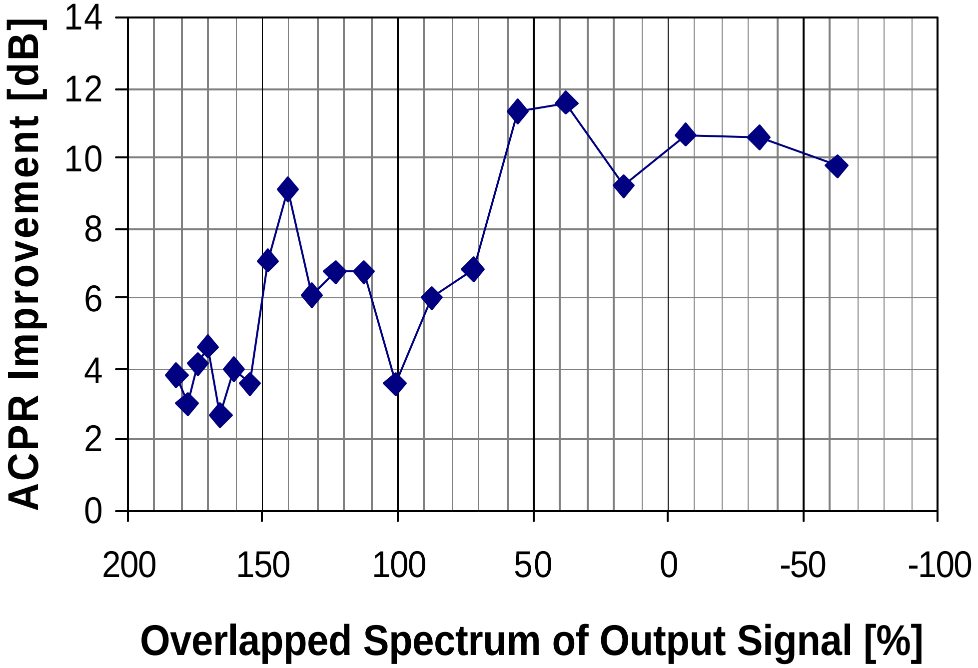
$e(n) = z(n) - g(y(n))$,

where $f(\cdot)$ is the nonlinear transfer function of PA,

and $g(\cdot)$ is an estimate of $f^{-1}(\cdot$

calculated by method of Least Squares

Predistortion Results



ACPR Improvement Using Subsampling Predistortion Architecture (Negative values in x-axis indicates sampling above Nyquist rate of the output signal)

Predistortion Results (cont.)

Sirenza SHF-0589: 2W GaAs HFET PA

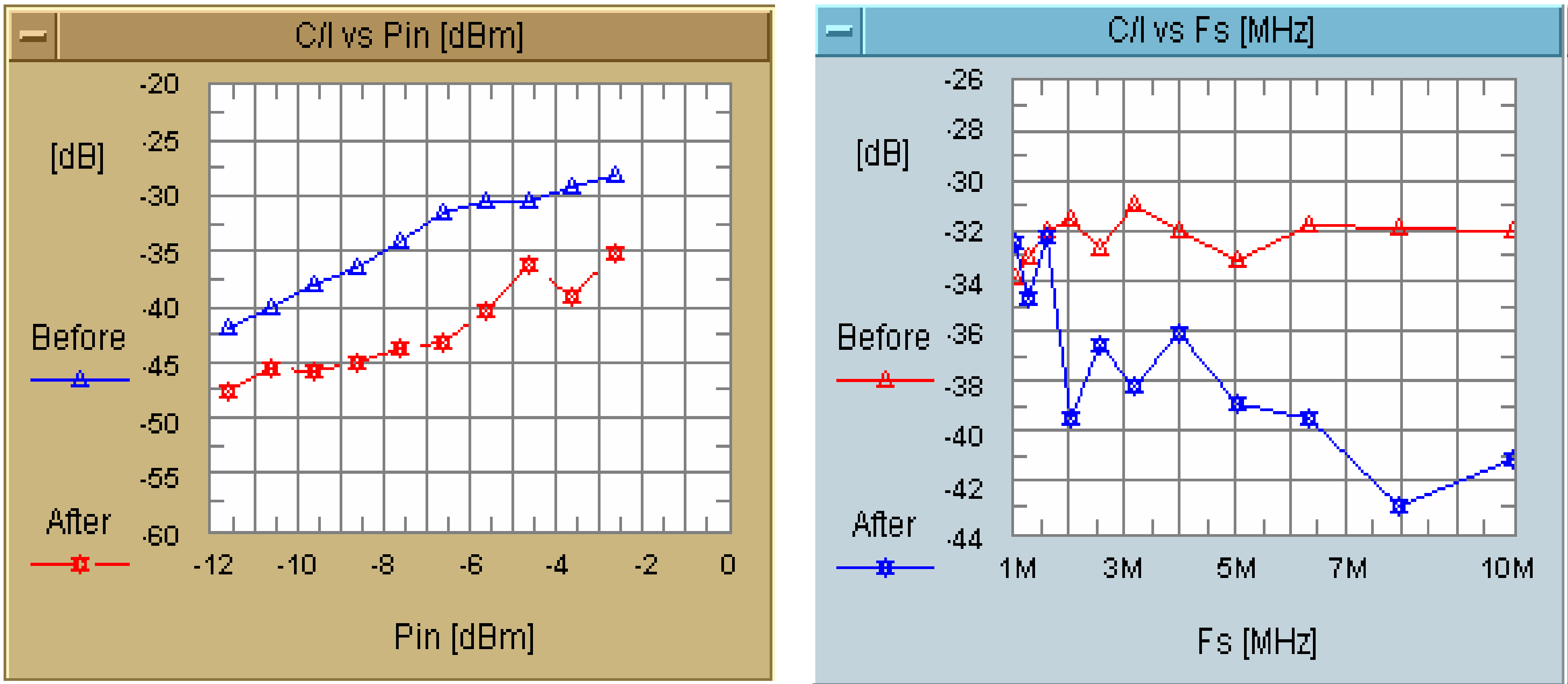
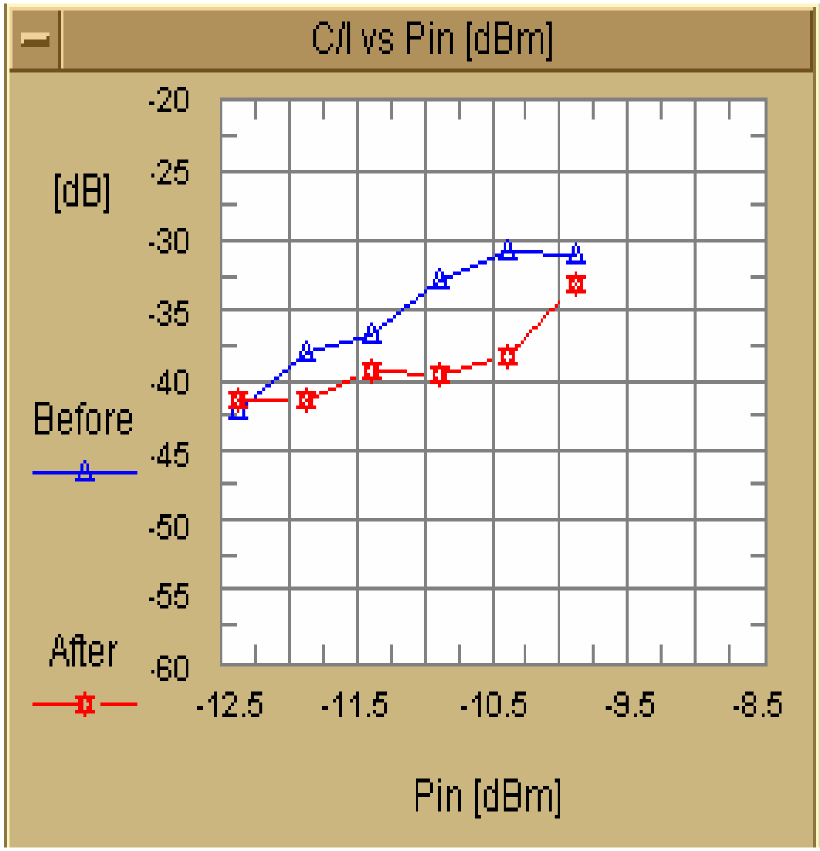
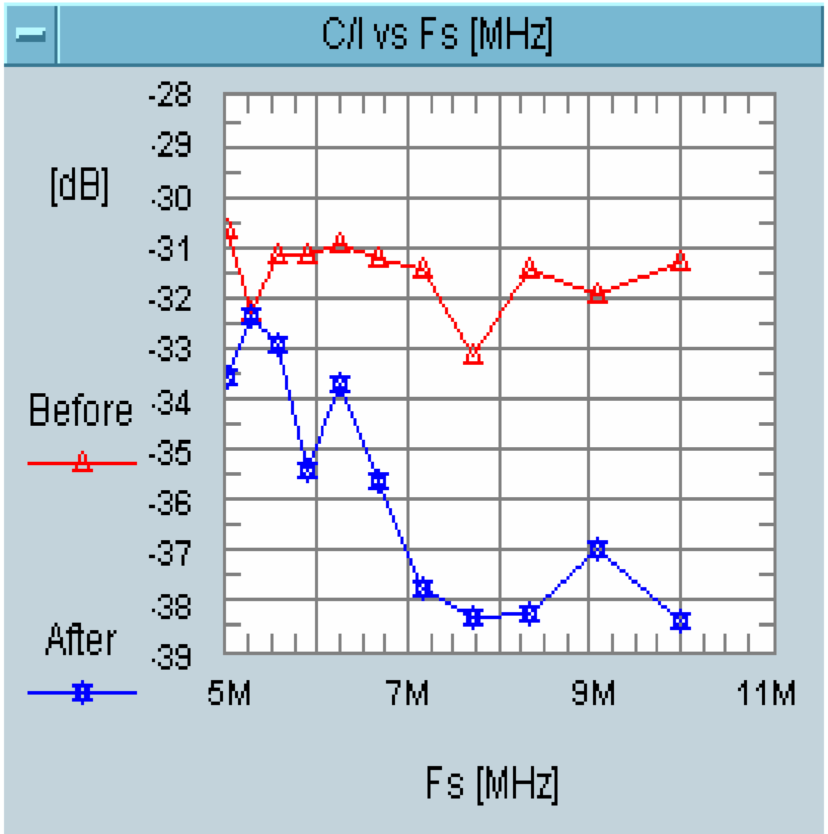


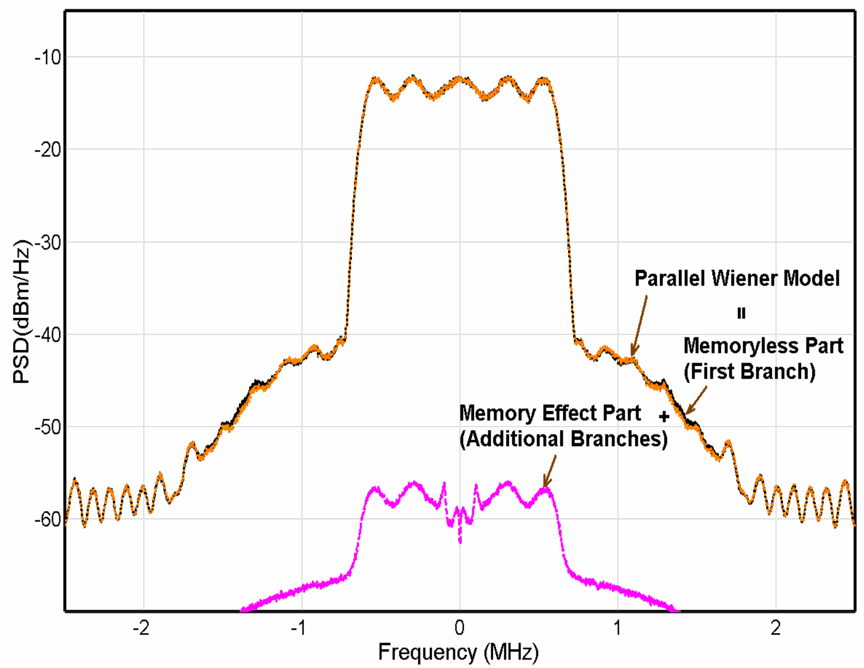
Figure: ACPR@885kHz measurements over P_{in} variations.

Predistortion Results (cont.)
Motorola MRF-9180 170W Si LDMOS

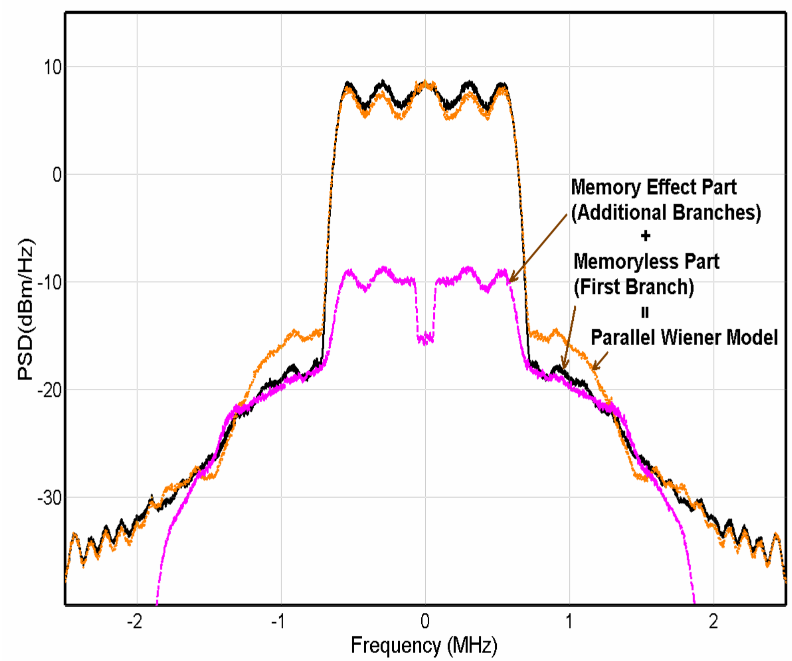




Impact of Memory Effects



"Memoryless" PA



PA with Strong Memory Effects

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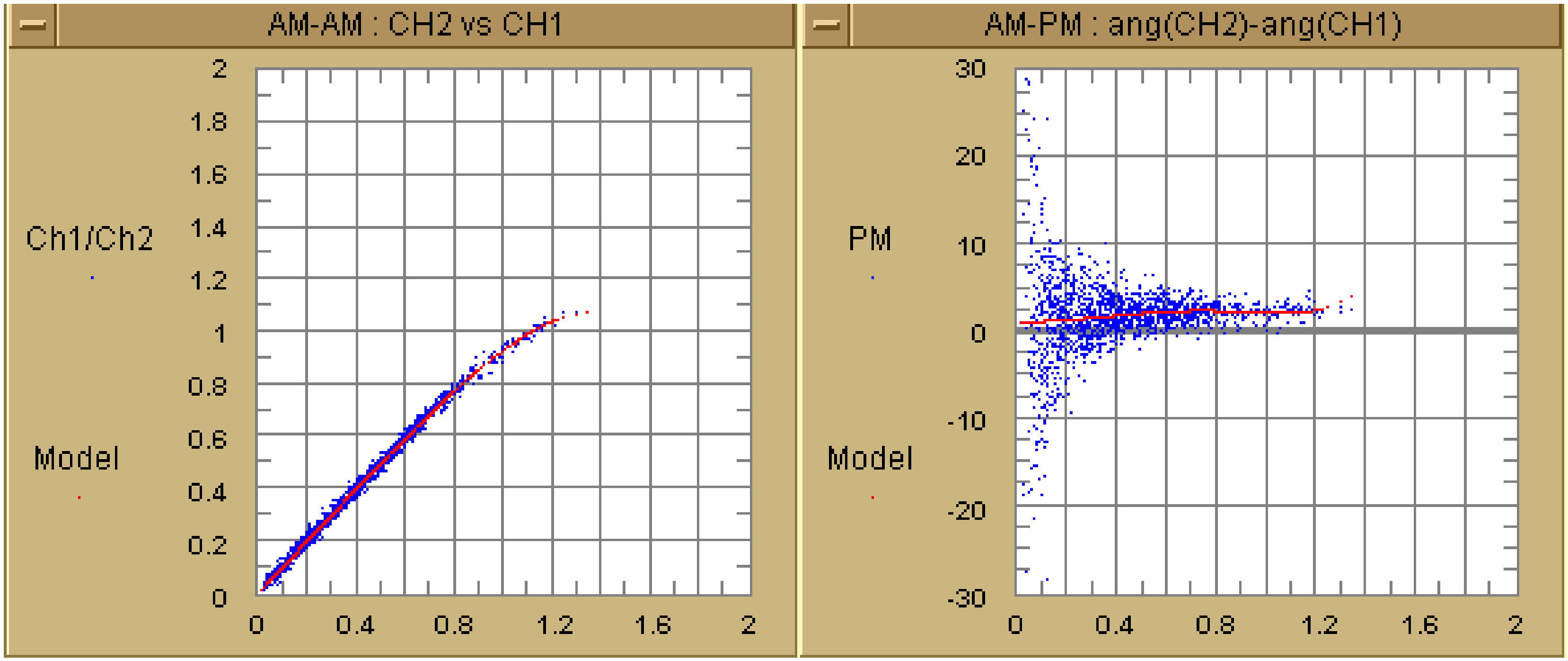
Impact of Memory Effects (cont.)



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September 9, 2002

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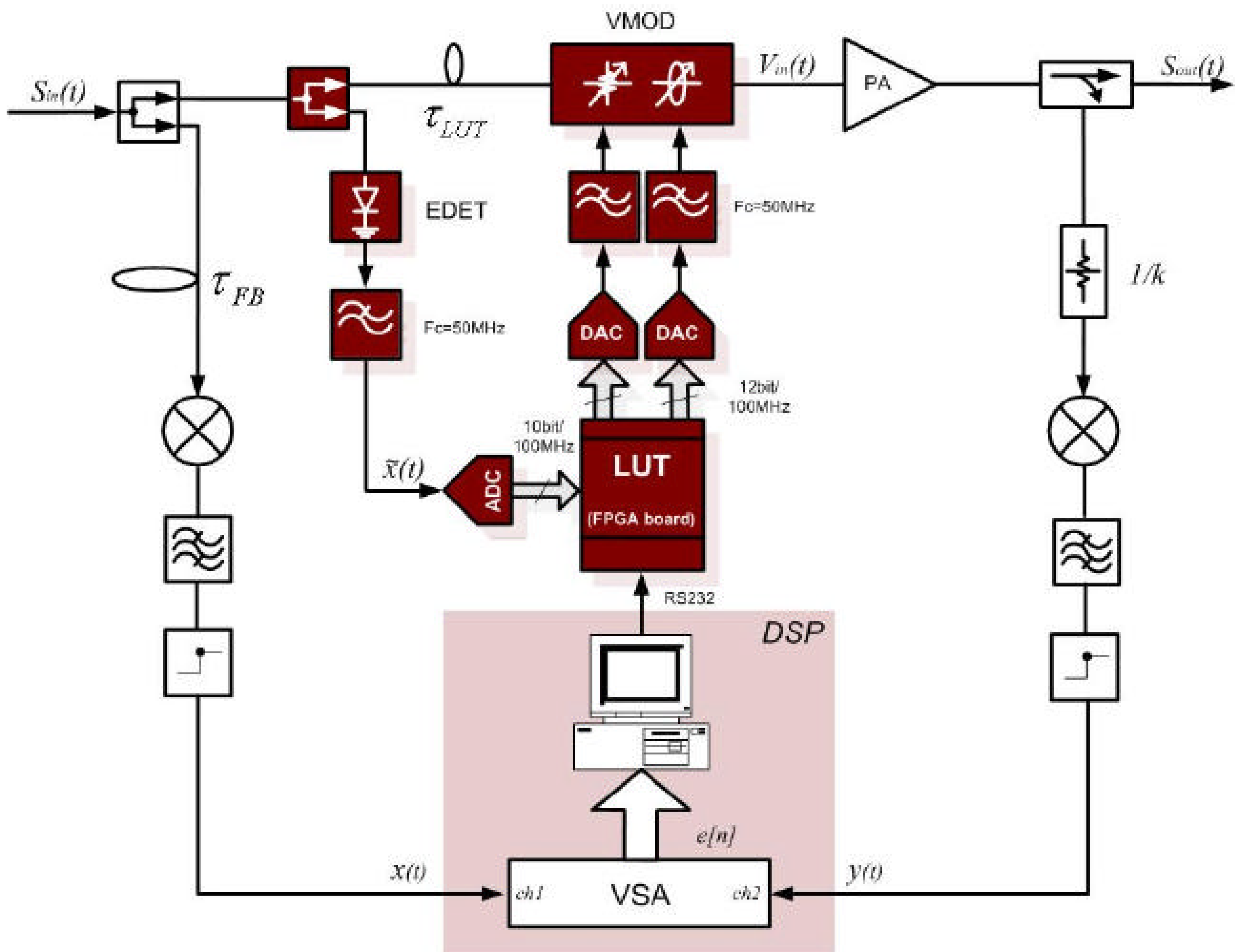
RF Envelope Predistortion

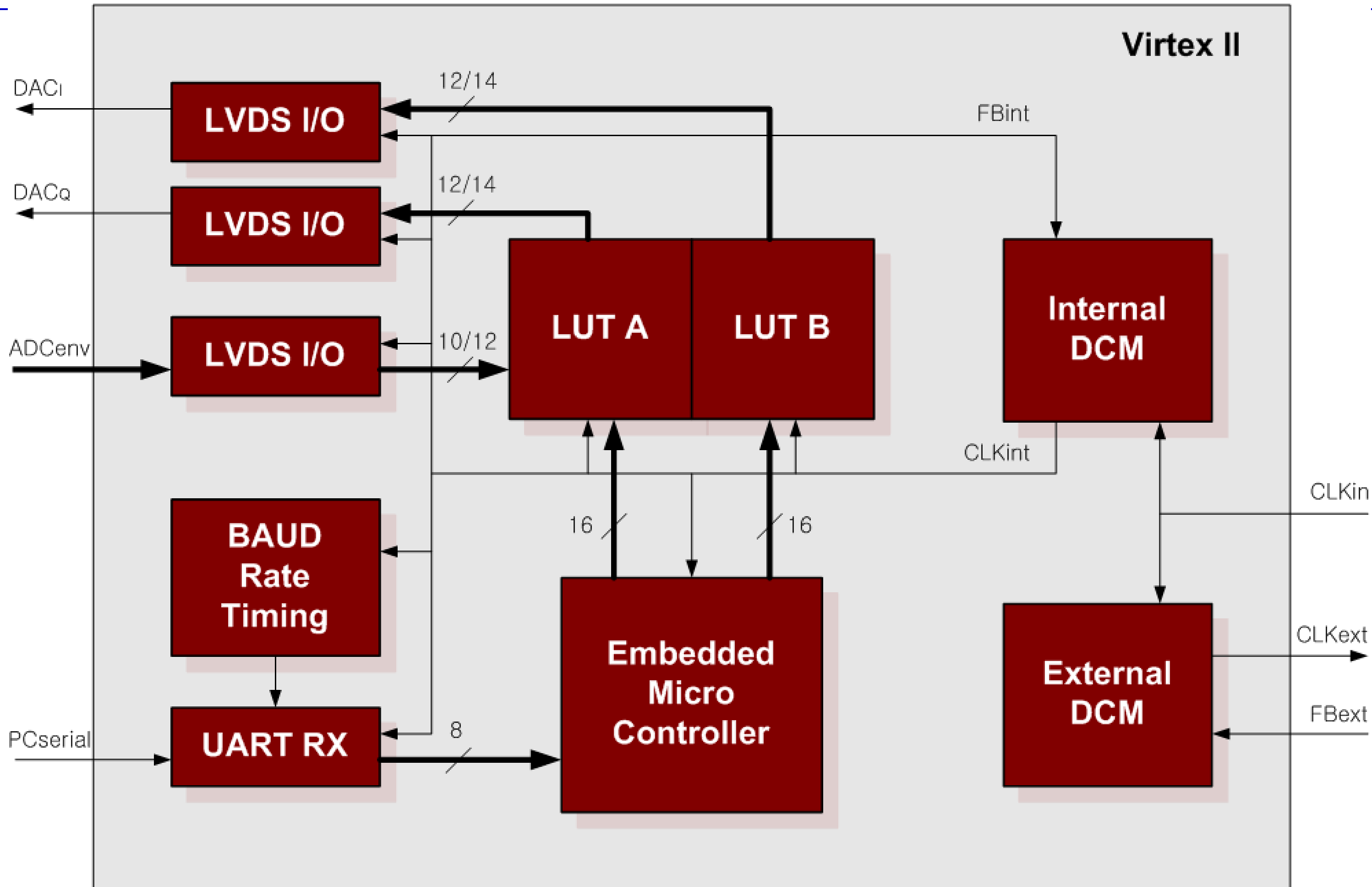
- Predistortion is performed directly on the modulated RF carrier using a high-speed vector modulator
- VMOD is driven by a look-up table (LUT) that is indexed by the instantaneous input power level
- Kusunoki, *et al.*, demonstrated 6-7 dB ACPR improvement without adaptive feedback*

*S.Kusunoki, *et al.*, “Power Amplifier Module with Digital Adaptive Predistortion for Cellular Phone, *2002 IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 765-8, Seattle, WA, June 4-6, 2002.

Adaptive RF Envelope Pre-Distortion Test Bed

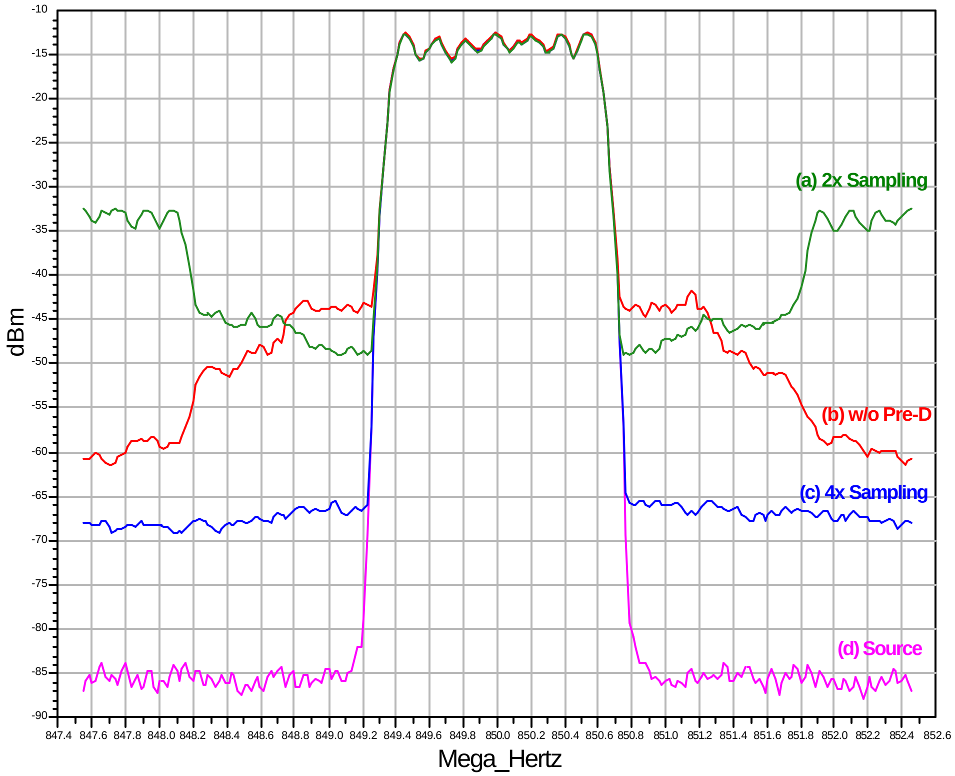


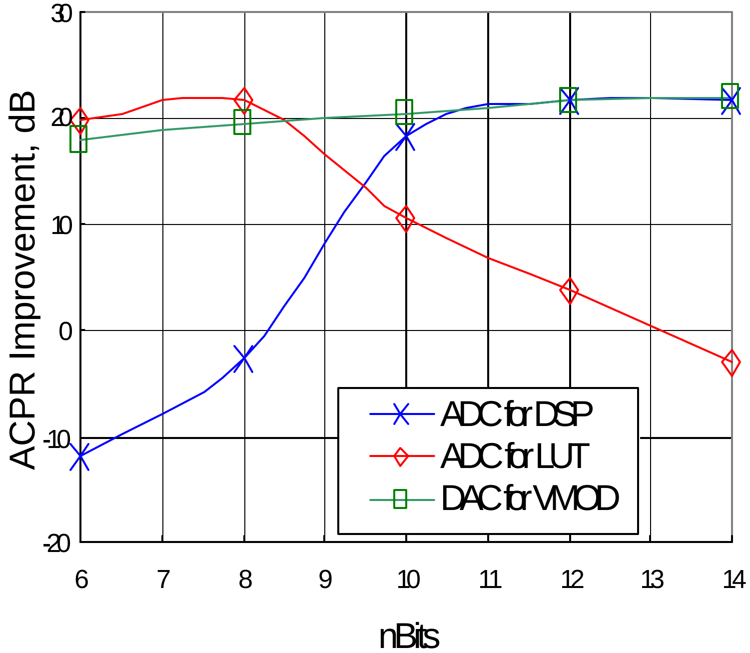
FPGA LUT Implementation
(Xilinx Vertex-II)



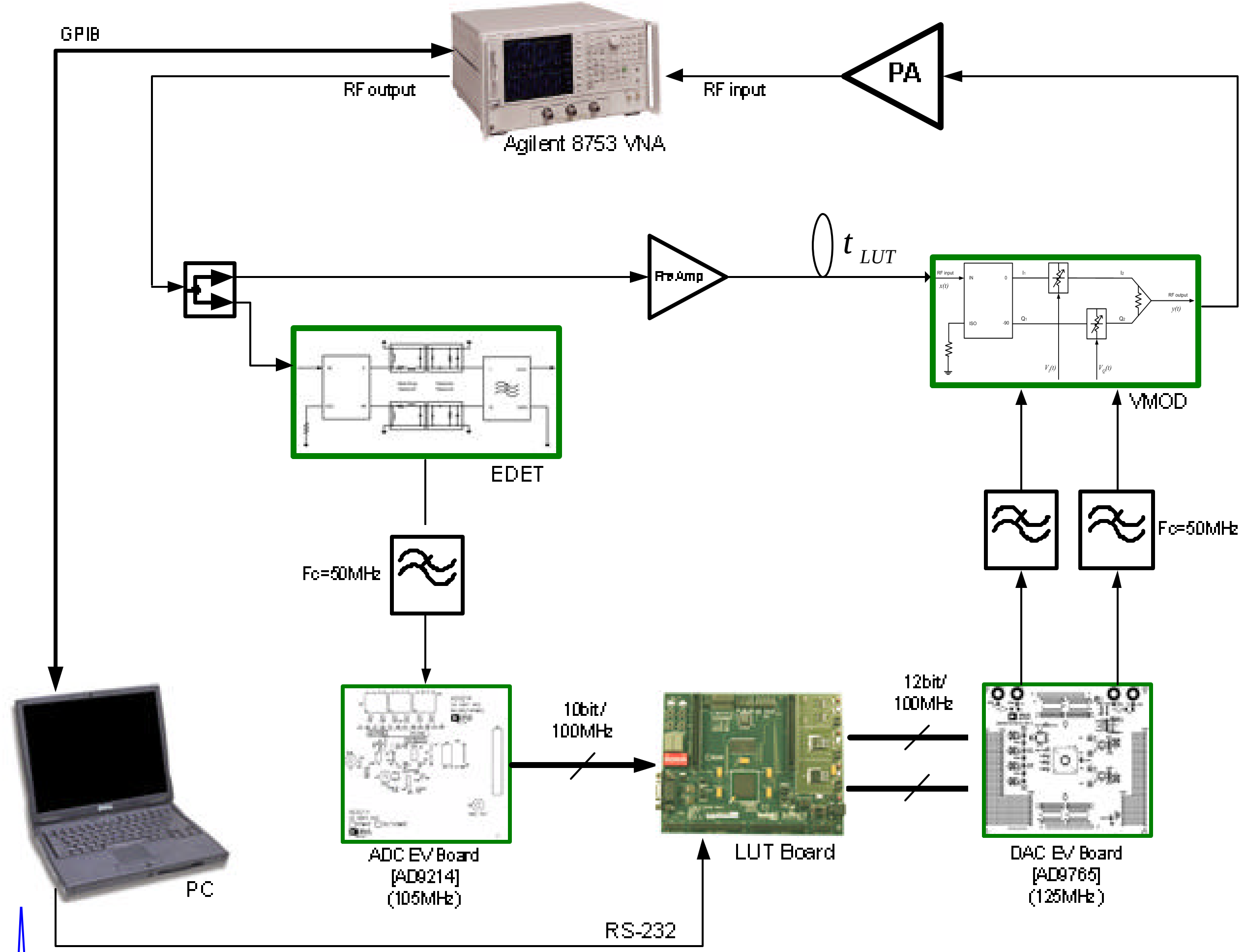
- LVDS: Low Voltage Differential Signaling
- UART: Universal Asynchronous Receiver Transmitter
- DCM: Digital Clock Manager

RF Envelope Pre-Distortion
ADS Simulations





RF Envelope Pre-D Test Bed



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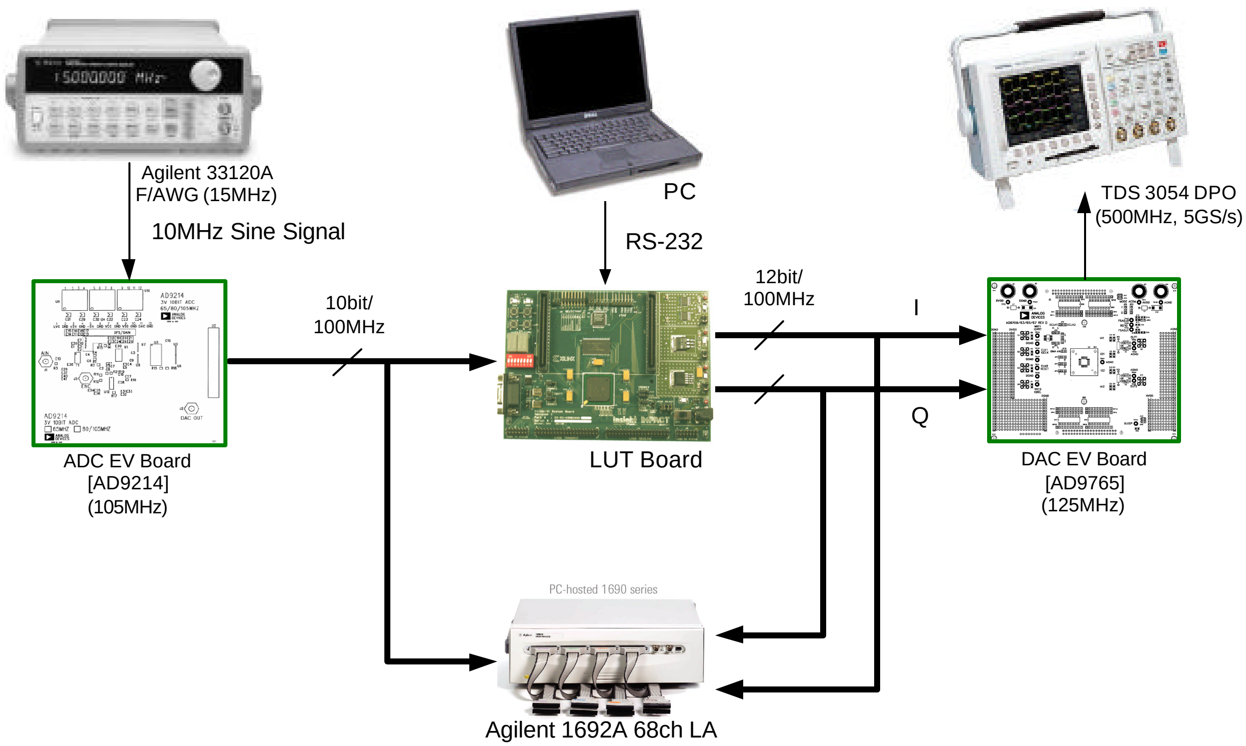
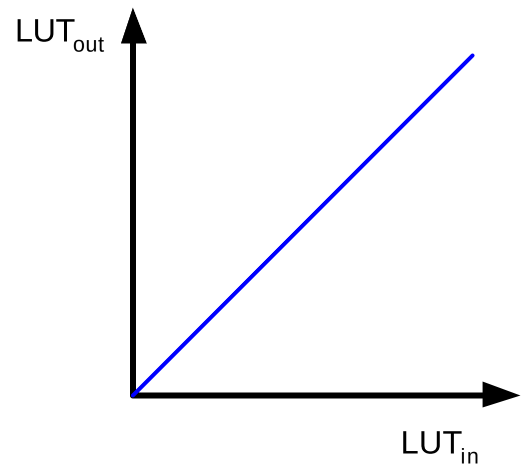
Signal Integrity ADC-LUT-DAC Path

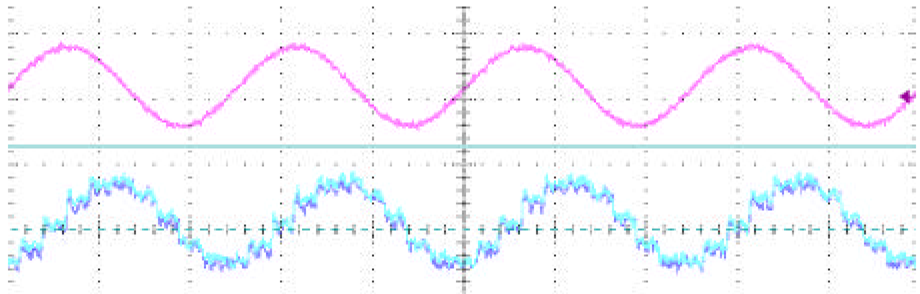


Testbed diagram

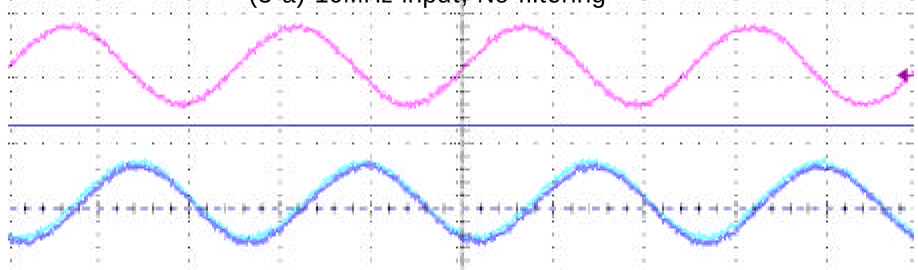


Linear function loaded into LUT

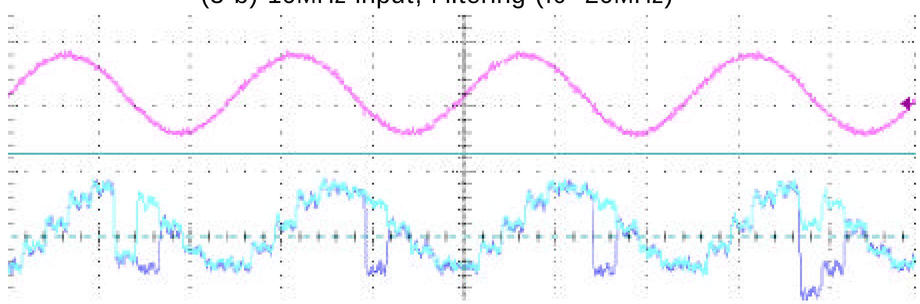
Signal Integrity ADC-LUT-DAC Path (cont.)



(3-a) 10MHz input, No filtering



(3-b) 10MHz input, Filtering (fc=20MHz)



(3-c) Glitch due to the crosstalk of data lines and overflow

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Summary and Conclusions

- Sub-sampling architecture developed to reduce sampling and processing requirements
  - Sample rate $\geq$ 2 x BW of input signal
  - Memory effects may increase this
- RF Envelope pre-D is an alternative to baseband digital pre-D
  - No digital I/Q stream required
  - Lower power, high BW