The Path to Efficient-yet-Linear Watt-class mmWave CMOS PAs: Device Stacking, Switch-mode Operation, Power Combining and Linearization

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Outline

- Motivation
- Stacking and Switch-mode Operation
- Large-scale Power Combining
- Linearized High Backoff-Efficiency Power DAC employing Supply Switching and Dynamic Load Modulation
- Conclusion
**Motivation**

- Operation at mmWave frequencies requires scaled technologies with low breakdown voltages, limiting the output power that can be generated from a single PA.
- Efficiency is limited by active and passive losses.
Motivation

- Output power and PAE degrade drastically at mmwave.
- Efficient unit cell PA design with high output power is challenging.

Can we get a watt of output power in CMOS at mmWave?
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Device Stacking in mmWave CMOS PAs

- Stacking increases output swing, eliminates the need for output matching to reach a desired output power level.
- Gain increases, thereby improving PAE

Can stacking be employed with switching class PAs?
Conventional Class-E PA Design

Conventional Class E design enforces Zero Voltage Switching (ZVS) and Zero-Derivative of Voltage (ZdVS) for ideally 100% efficiency.

This approach is sub-optimal when the switch and passive components contribute significant loss.

For $\eta=100\%$ when $R_{on} \approx 0$. 

$ZVS: V_S(T/2) = 0$

$ZDVS: \left. \frac{dV_S}{dt} \right|_{T/2} = 0$
The stacked devices are assumed to behave like a single switching device with a linearly larger $R_{on}$ and $V_{dd}$. 
HIGHLIGHTS OF ANALYTICAL FORMULATION*

- Takes finite choke inductance ($L_s$) into account.
- Takes the effect of switch $R_{ON}$ into account formally (but assumes $R_{ON} << 1/\omega C_{out}$).
- Takes into account passive loss.
- Takes into account input drive power.
- Load impedance is not chosen for Class E switching conditions (ZVS/ZdVS) but rather are varied to optimize PAE.
- Analytical equivalent to load-pull simulations.
- Provides a starting point for design optimization.

*Anandaroop Chakrabarti and Harish Krishnaswamy, “An Improved Analysis and Design Methodology for RF Class-E Power Amplifiers with Finite DC-feed Inductance and Switch On-Resistance,” 2012 IEEE ISCAS.

Loss-Aware mmWave stacked Class-E design methodology formally takes into account several mmWave non-idealities (device loss, input drive power, passive loss).
Device Stacking in 45nm SOI at 45GHz

- $P_{out} > 20$dBm can be achieved by stacking without drastic penalty in PAE.
- Device size and current stress determine the maximum number of devices that can be stacked.
- The graphs represent fundamental limits on achievable performance in stacked CMOS Class-E-like PAs.

• Series stacking is compared with the power combining of multiple 2-stack Class-E-like PAs using a tree of 2-way 50Ω Wilkinson combiners.
• Series stacking enables significantly higher efficiency for the same output power level.

Stacking vs. Impedance Transformation

- Series stacking is compared with the use of LC impedance transformers in conjunction with scaled 2-stack Class-E-like PAs.
- Series stacking enables significantly higher efficiency for the same output power level.

Pseudo-differential, 2-stacked unit PA is designed based on the finite-choke, Class E design methodology.

\[ P_{\text{sat}} = 18.2 \text{dBm} \]
\[ \text{PAE}_{\text{max}} = 28\% \]
Single-Ended 2-stacked Class E PA designed based on the Loss-Aware Millimeter-Wave Stacked-Class-E design methodology.

4-stacked 45nm SOI Class E PA

Single-Ended 4-stacked Class E PA designed based on the Loss-Aware Millimeter-Wave Stacked-Class-E design methodology.

Packaged and connectorized Q-band stacked 45nm SOI CMOS Class-E-like PA has been transitioned to Northrop Grumman for insertion into a SATCOM demo.
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On-Chip Power Combining Challenges

Transformer Combining

- Asymmetric input impedance due to parasitics results in destructive combining and stability challenges.

Current Combining

- Increased load reduces power generated by each PA – no power combining benefit.

Wilkinson Combining

- Cascading 2:1 Wilkinson's results in increased loss.
- N:1 Wilkinson's are challenging due to high $Z_0$ required.
8-way Lumped $\lambda/4$ Power Combiner

• Large-scale 8-way power combining is used to enhance output power.

• Lumped equivalents of quarter-wave lines are used to easily achieve the necessary high $Z_o$. 

\[
Z_o(n) = 50\sqrt{n} \\
Z_o(8) = 141.421\Omega
\]

\[
Z_o(n) = \sqrt{\frac{L(n)}{C(n)}}; \quad \omega = \frac{1}{\sqrt{L(n)C(n)}} \\
L(8)|_{45\text{GHz}} = 0.5nH; \quad C(8)|_{45\text{GHz}} = 25fF
\]
Combiner Performance

- Measurements closely correspond with EM simulations.
- Achieves **78%** peak efficiency in contrast to an 8-way 2:1 Wilkinson cascade which achieves only 63% at 45GHz.
Eight unit cells (a two-stacked driver + a four-stacked main PA) power-combined using the eight-way lumped-element λ/4 combiner.

\[ Z_{\text{in}} = \frac{Z_0^2}{50 \times N} = 50\Omega \text{ for } N=8 \text{ & } Z_0 = 141\Omega \]

\[ L = \frac{Z_0}{\omega_0}, \quad C = \frac{1}{\omega_0 Z_0} \]

\[ L_1 + L_2 = 3\frac{\lambda}{4} \]

[Diagram of the power combiner system with various components and connections.]
Watt-class PA S-Parameter Measurement

Peak $S_{21} = 19.4\text{dB}$ at 50GHz with a 3dB BW of 13GHz.

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Watt-Class PA Large-Signal Performance

Peak output power of >27dBm and -1dB flatness is observed in $P_{\text{out,\,sat}}$ and $P_{\text{out,-1dB}}$ from 33-46GHz.
The PA is driven at the $P_{\text{out,sat}}$ drive level for 12.5 hours on a probe station.

Variations seen in output power and efficiency are small.
Comparison with CMOS mmWave PAs

PAE (%) vs Output Power (dBm)

- 65nm CMOS
- 90nm CMOS
- 45nm SOI CMOS
- This Work
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Power amplifiers have a linearity vs. efficiency tradeoff.

High efficiency under back-off is essential to support complex modulation schemes.

Can linearity, large-scale power combining and better than Class B back-off efficiency co-exist?
Power DAC Approach

- Supply-switched power-combined DAC for multi-bit resolution & high average efficiency.
- Load modulation using non-isolating combiner facilitates linear DAC profile.
First linearizing PA architecture at mmWave frequencies that simultaneously employs large-scale power combining for higher $P_{out}$, PA supply switching for higher efficiency under back-off, and load-modulation for linearization of switching PAs.
Supply-switched Class-E-like PA

- 1-bit supply-switched power DAC cell in 45nm SOI CMOS.
- 2-stacked Class-E PA unit cell augmented with digital switches to facilitate high-speed turn-on/turn-off.

Anandaroop Chakrabarti and Harish Krishnaswamy, “Design Considerations for Stacked Class-E-like mmWave HighSpeed Power DACs in CMOS,” 2013 IEEE International Microwave Symposium.
1-bit Cell 1Gbps OOK Meas. @ 47GHz

Supply-switched unit cell can be turned on and off at ~1GHz rate.

Anandaroop Chakrabarti and Harish Krishnaswamy, “Design Considerations for Stacked Class-E-like mmWave HighSpeed Power DACs in CMOS,” 2013 IEEE International Microwave Symposium.
Operation of the Architecture

\[ Z_{\text{in}} = \frac{Z_0^2}{(50 \times m)} = 25\Omega \]
Operation of the Architecture

\[ Z_{in} = Z_0^2/(50 \times m) = 28.57\Omega \]

\[ P_{out,unit} \propto \frac{V_{DD}^2}{R_L} \]

\[ P_{out,total} \propto m \times \frac{V_{DD}^2}{Z_0^2/(mR_0)} \propto m^2 \frac{V_{DD}^2}{Z_0^2/(R_0)} \]
Operation of the Architecture

\[ Z_{in} = Z_0^2/(50x m) = 33.33\Omega \]

\[ P_{out,unit} \propto \frac{V_{DD}^2}{R_L} \]

\[ P_{out,total} \propto m \times \frac{V_{DD}^2}{Z_0^2/l(mR_0)} \propto m^2 \frac{V_{DD}^2}{Z_0^2/l(R_0)} \]
Operation of the Architecture

\[ Z_{\text{in}} = Z_0^2/(50\times m) = 40\Omega \]

\[ P_{\text{out,unit}} \propto \frac{V_{DD}^2}{R_L} \]

\[ P_{\text{out,total}} \propto m \times \frac{V_{DD}^2}{Z_0^2/(mR_0)} \propto m^2 \frac{V_{DD}^2}{Z_0^2/(R_0)} \]
Operation of the Architecture

\[ Z_{in} = Z_0^2/(50 \times m) = 50 \Omega \]

\[ P_{out,unit} \propto \frac{V_{DD}^2}{R_L} \]

\[ P_{out,total} \propto m \times \frac{V_{DD}^2}{Z_0^2/(mR_0)} \propto m^2 \frac{V_{DD}^2}{Z_0^2/(R_0)} \]
Operation of the Architecture

\[ Z_{in} = Z_0^2/(50\times m) = 66.66\Omega \]

\[ P_{out,unit} \propto \frac{V_{DD}^2}{R_L} \]

\[ P_{out,total} \propto m \times \frac{V_{DD}^2}{Z_0^2/(mR_0)} \propto m^2 \frac{V_{DD}^2}{Z_0^2/(R_0)} \]
Operation of the Architecture

$Z_{in} = Z_0^2/(50x_m) = 100\Omega$

$P_{out,unit} \propto \frac{V_{DD}^2}{R_L}$

$P_{out,total} \propto m \times \frac{V_{DD}^2}{Z_0^2 / (mR_0)} \propto m^2 \frac{V_{DD}^2}{Z_0^2 / (R_0)}$
Operation of the Architecture

\[ Z_{in} = Z_0^2/(50 \times m) = 200 \Omega \]

\[ P_{out,unit} \propto \frac{V_{DD}^2}{R_L} \]

\[ P_{out,total} \propto m \times \frac{V_{DD}^2}{Z_0^2/(mR_0)} \propto m^2 \frac{V_{DD}^2}{Z_0^2/(R_0)} \]
Power DAC Output Power and Amplitude

- Input Power (dBm)
- Output Power (dBm)
- Output Amplitude (V)

Graphs showing the relationship between input power and output power/amplitude for different values of m (2 to 8).

- INL (fraction of LSB)
- DNL (fraction of LSB)

Graphs showing the INL and DNL for different values of m (0 to 8).
• Measurements show 8.2% peak DE and 6.2% peak PAE.
• A 2.5x improvement in drain efficiency and a 2x improvement in PAE at 6dB backoff over the baseline case where all PAs are always kept on.
Comparison to $>20\text{dBm}$/Linearized CMOS mmWave PAs

- Agah, IMS `12
- Wicks, RFIC `08
- Law, ISSCC `10
- This work

PAE-6dB/PAEmax(%) vs. Output power (dBm)
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Conclusion

• A comprehensive design methodology for stacked mmWave class-E PAs has been demonstrated.
• A low-loss power combining technique is shown which is used in conjunction with stacking to achieve watt-class output power at mmWave in CMOS.
• A direct digital-to-mmWave power DAC architecture which achieves high output power, linearity and back-off efficiency has been developed.
• Future work involving coexistence of high-resolution, linearity, high-power and high-efficiency under back-off is an exciting area of research.
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