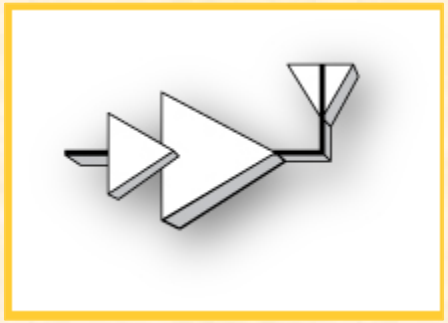
2014 Power Amplifier Symposium



BROADBAND PA TECHNIQUES FOR EFFICIENCY ENHANCEMENT

Dr. Andrei Grebennikov

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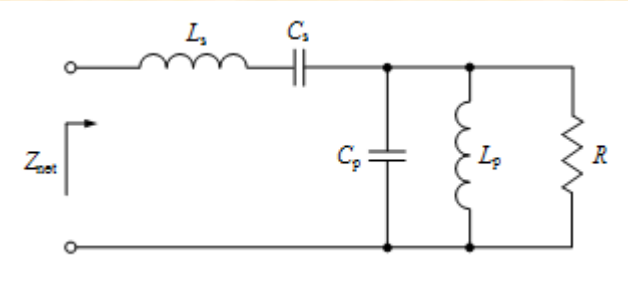
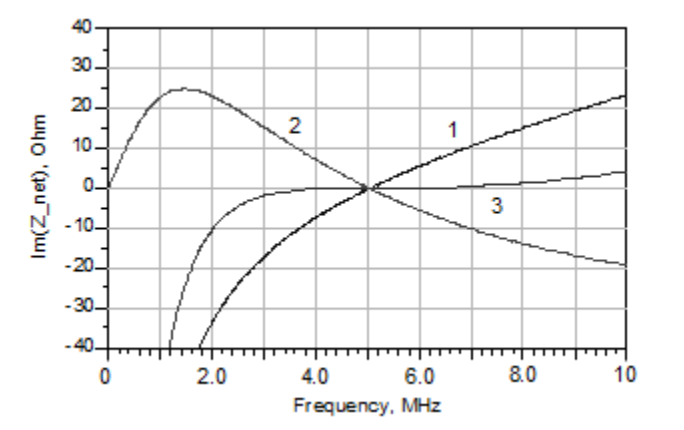
BROADBAND POWER AMPLIFIER TECHNIQUES FOR EFFICIENCY ENHANCEMENT

1. Reactance compensation technique with series and parallel resonant circuits
2. Broadband parallel-circuit Class-E power amplifier
3. Fully integrated broadband CMOS Class-E power amplifier
4. Broadband Class-E power amplifier with series inductance
5. Broadband parallel Doherty amplifier
6. Inverted Doherty amplifier architecture
7. Broadband inverted GaN HEMT Doherty amplifier

1. Reactance compensation technique

Reactance compensation load networks with series and parallel resonant circuits





Input load-network reactance

$$\mathrm{Im}Z_{\mathrm{net}}(\omega) = \omega L_s - \frac{1}{\omega C_s} - \frac{\omega' C_p}{(1/R)^2 + (\omega' C_p)^2}$$

$$\omega' = \omega\left(1 - \frac{\omega_0^2}{\omega^2}\right)$$

$$\omega_0 = 1/\sqrt{L_s C_s} = 1/\sqrt{L_p C_p}$$

To maximize frequency bandwidth:

$$\left.\frac{d\,\mathrm{Im}Z_{\mathrm{net}}(\omega)}{d\omega}\right|_{\omega=\omega_0} = 0$$

$$C_p + \frac{1}{\omega_0^2 L_p} - \frac{2L_s}{R^2} = 0$$

1 - reactance provided by series resonant circuit

2 - reactance provided by parallel resonant circuit

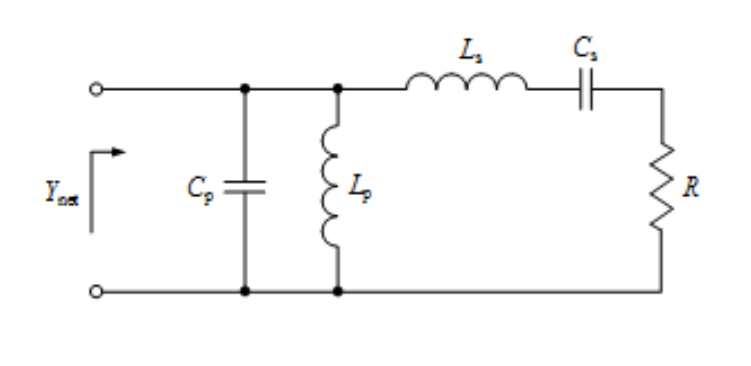
3 – summation of both reactances with opposite slopes

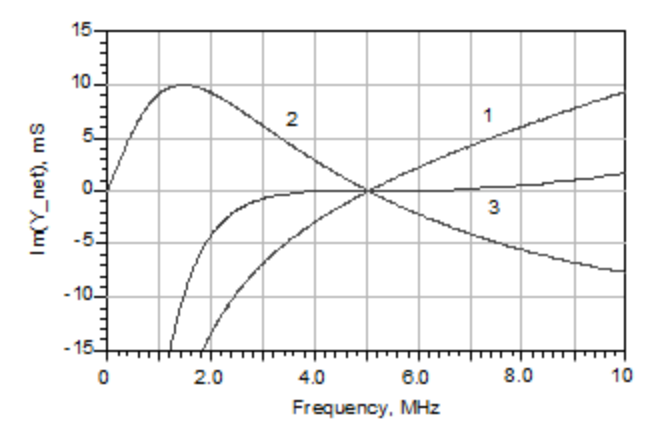
Equal loaded quality factors

$$Q_L = \omega_0 C_p R = \omega_0 L_s / R$$

1. Reactance compensation technique

Reactance compensation load networks with parallel and series resonant circuits





Input load-network admittance

$$Y_{\text{net}}(\omega) = \left(j\omega C_{\text{p}} + \frac{1}{j\omega L_{\text{p}}} + \frac{1}{R + j\omega' L_{\text{s}}} \right)$$

$$\omega' = \omega\left(1 - \frac{\omega_0^2}{\omega^2}\right)$$

$$\omega_0 = 1/\sqrt{L_{\text{s}} C_{\text{s}}} = 1/\sqrt{L_{\text{p}} C_{\text{p}}}$$

To maximize frequency bandwidth:

$$\left.\frac{d\,\text{Im}Y_{\text{net}}(\omega)}{d\omega}\right|_{\omega=\omega_0} = 0$$

$$C_{\text{p}} + \frac{1}{\omega_0^2 L_{\text{p}}} - \frac{2L_{\text{s}}}{R^2} = 0$$

Equal loaded quality factors

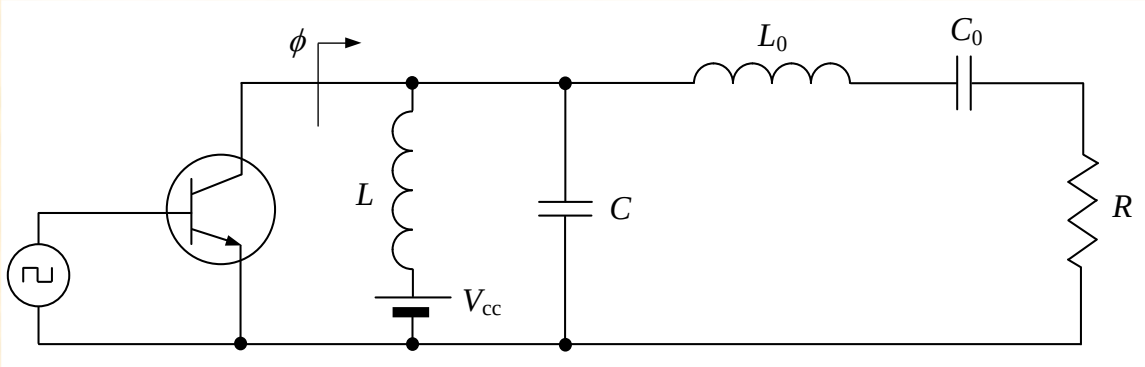
$$Q_{\text{L}} = \omega_0 C_{\text{p}} R = \omega_0 L_{\text{s}} / R$$

1 - susceptance provided by parallel resonant circuit

2 - susceptance provided by series resonant circuit

3 – summation of both susceptances with opposite slopes

2. Broadband parallel-circuit Class E power amplifier



$$v(\omega t)\Big|_{\omega t = 2\pi} = 0 \qquad \frac{dv(\omega t)}{d\omega t}\Big|_{\omega t = 2\pi} = 0$$

Inductive impedance at fundamental:

$$\phi = \tan^{-1}\left(\frac{R}{\omega L} - \omega RC\right) = 34.244°$$

Optimum circuit parameters:

$$L = 0.732\frac{R}{\omega}$$ ***- parallel inductance***

$$C = \frac{0.685}{\omega R}$$ ***- shunt capacitance***

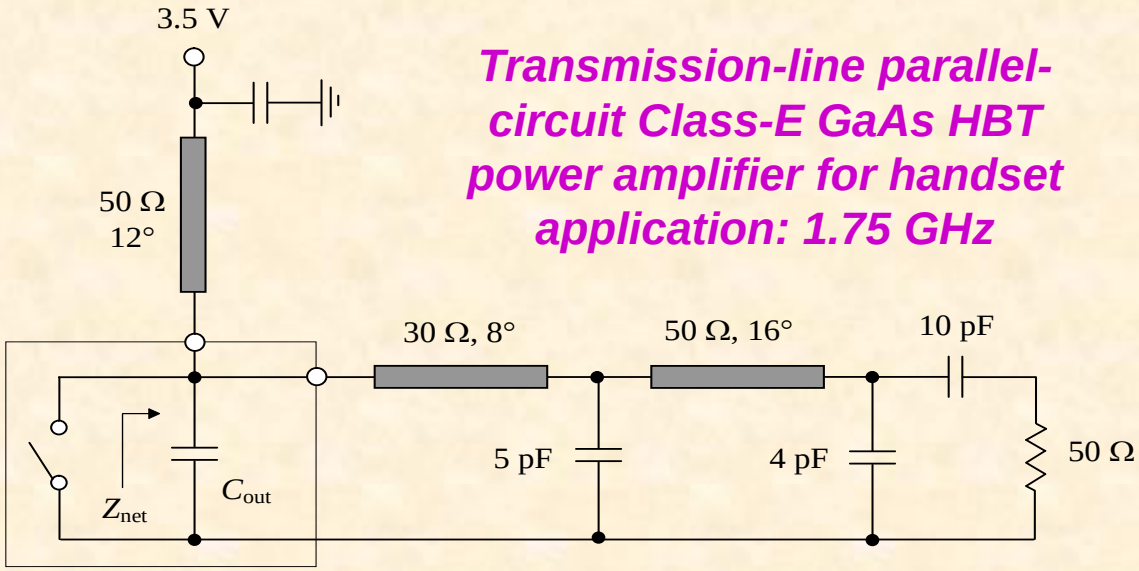
$$R = 1.365\frac{V_{cc}^2}{P_{out}}$$ ***- load resistance: highest value in Class E***

Optimum parameters for series resonant circuit in broadband Class-E mode:

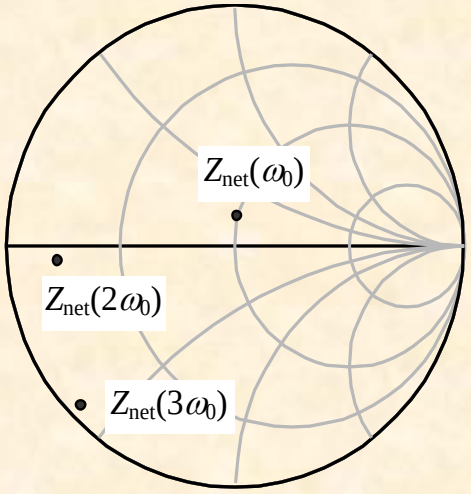
$$L_0 = 1.026\frac{R}{\omega_0}$$

$$C_0 = 1/\omega^2 L_0$$

2. Broadband parallel-circuit Class E power amplifier



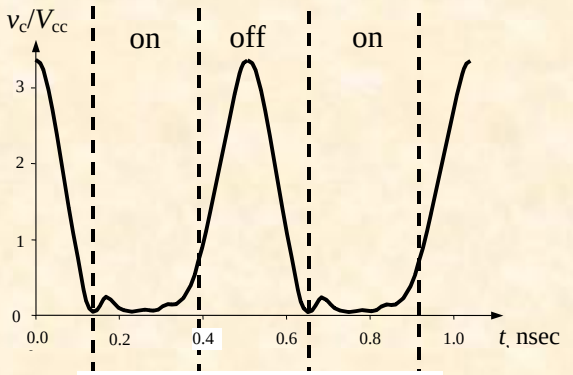
Transmission-line parallel-circuit Class-E GaAs HBT power amplifier for handset application: 1.75 GHz



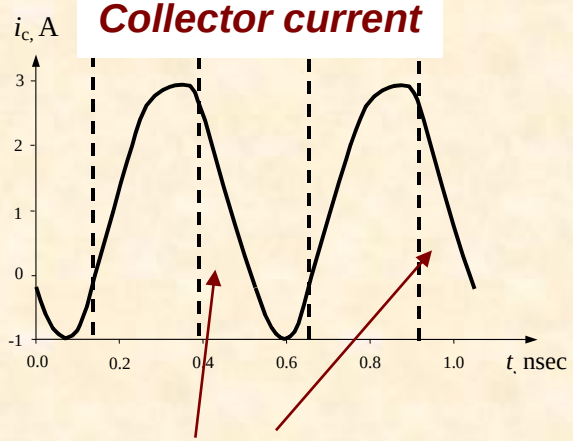
- ***parameters of parallel transmission line is chosen to realize optimum inductive impedance at fundamental***

- ***output matching circuit consisting of series microstrip line with two shunt capacitors should provide capacitive reactances at second and third harmonics***

Collector voltage



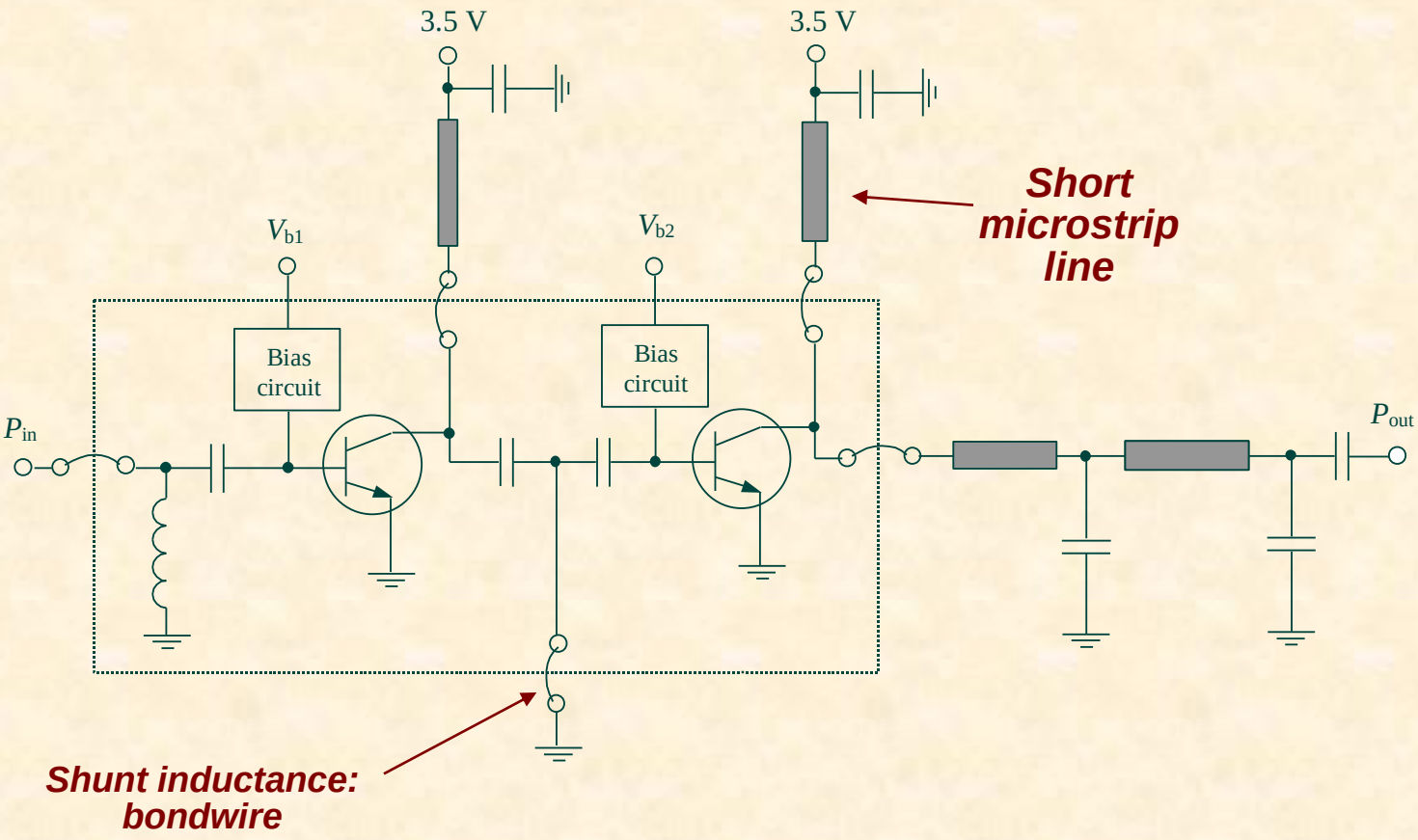
Collector current



Current flowing through collector capacitor

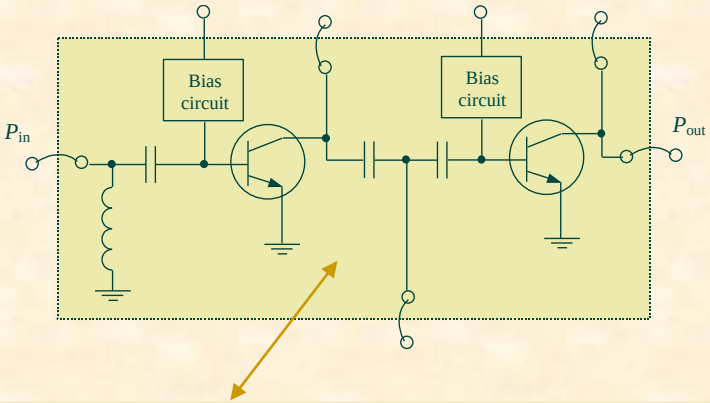
2. Broadband parallel-circuit Class E power amplifier

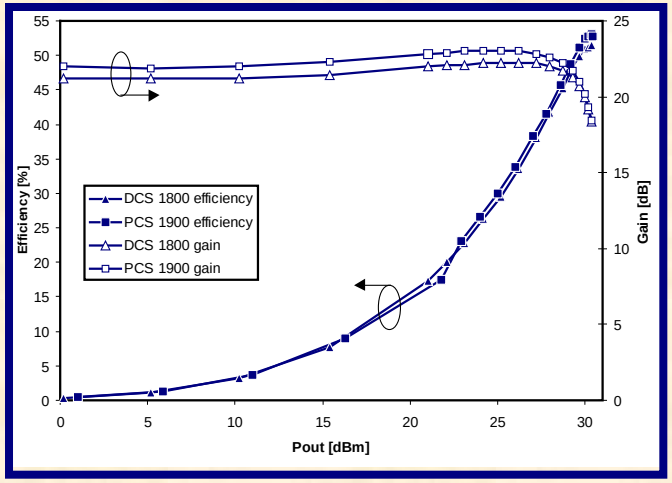
1.71-1.98 GHz handset Class-E InGaP/GaAs HBT power amplifier: two-stage MMIC designed in 2001



2. Broadband parallel-circuit Class E power amplifier

1.71-1.98 GHz handset Class-E InGaP/GaAs HBT power amplifier: two-stage MMIC designed in 2001

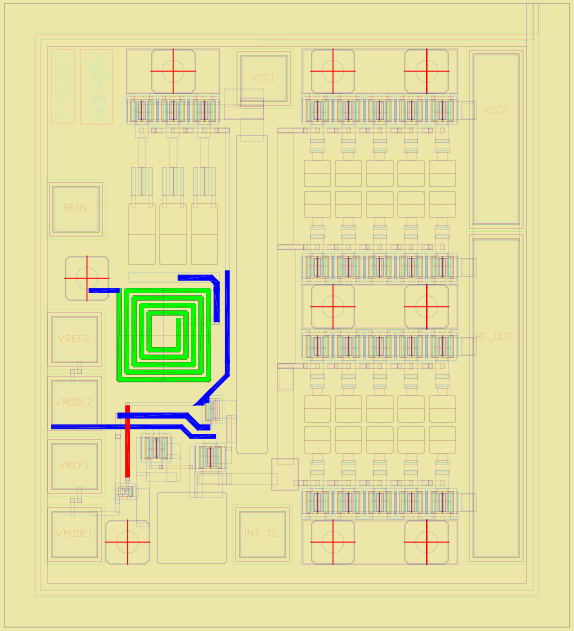




First device: 540 um²

Second device: 3600 um²

Die size: 0.9 x 1.0 mm²



DCS1800/PCS1900:

Pout ≥ 30 dBm

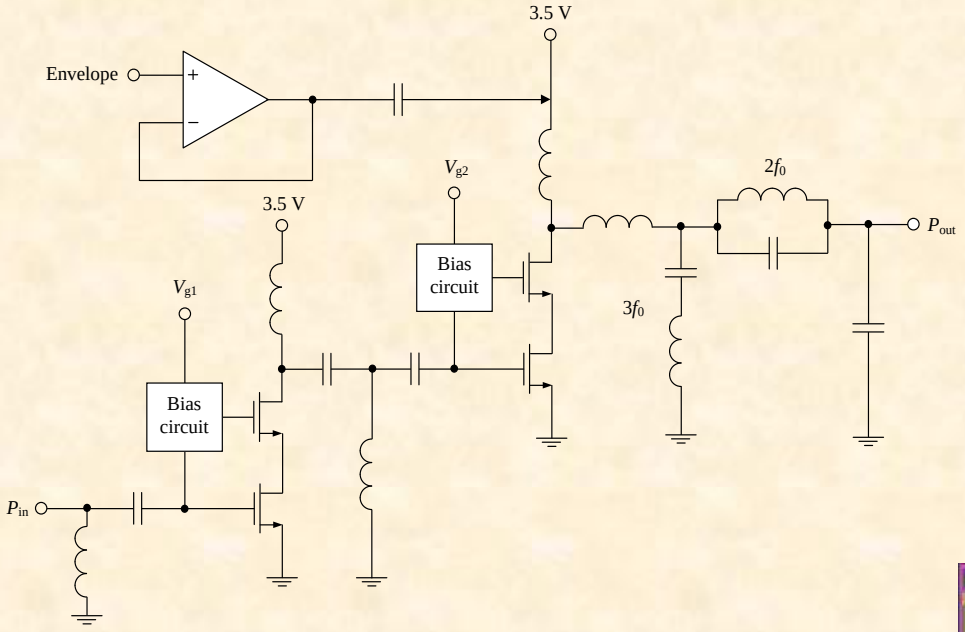
PAE ≥ 51 %

WCDMA at 27 dBm output power:

ACPR ≤ -37 dBc

PAE ≥ 38 %

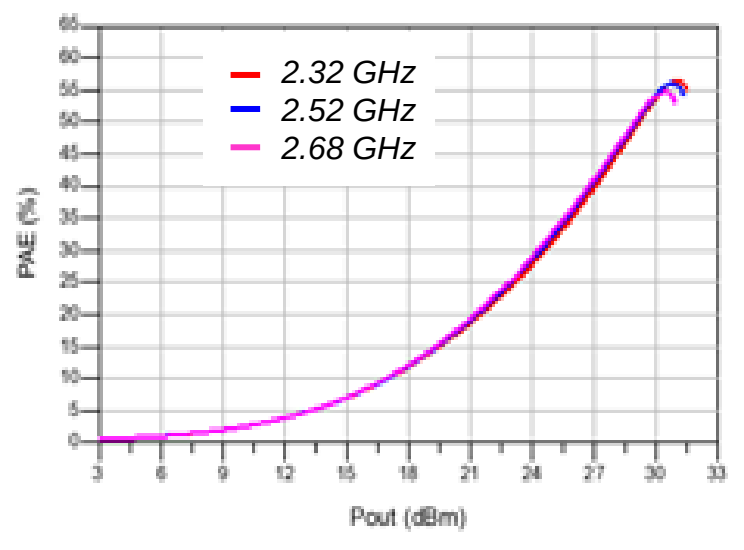
3. Fully integrated broadband CMOS Class-E power amplifier



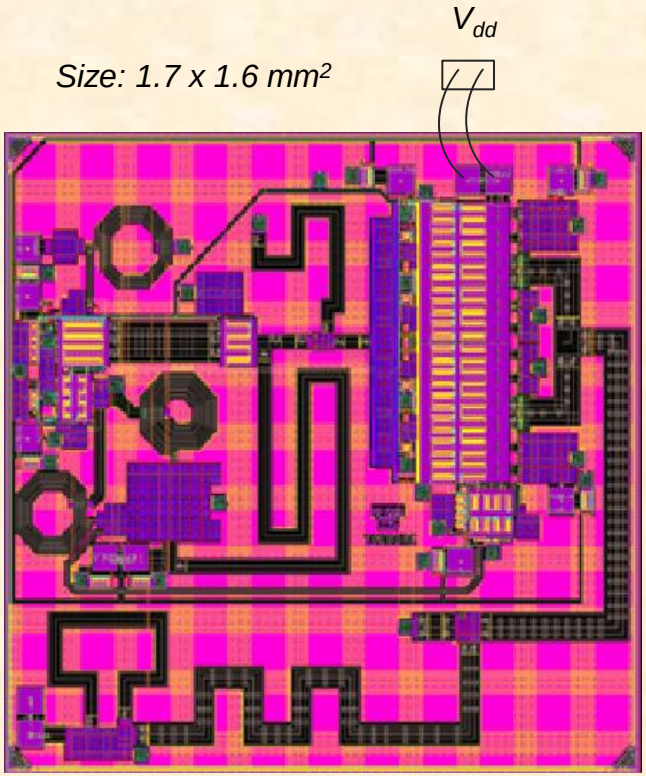
For LTE applications:
2.3-2.7 GHz

High resistivity substrate for high efficiency

Simulations:

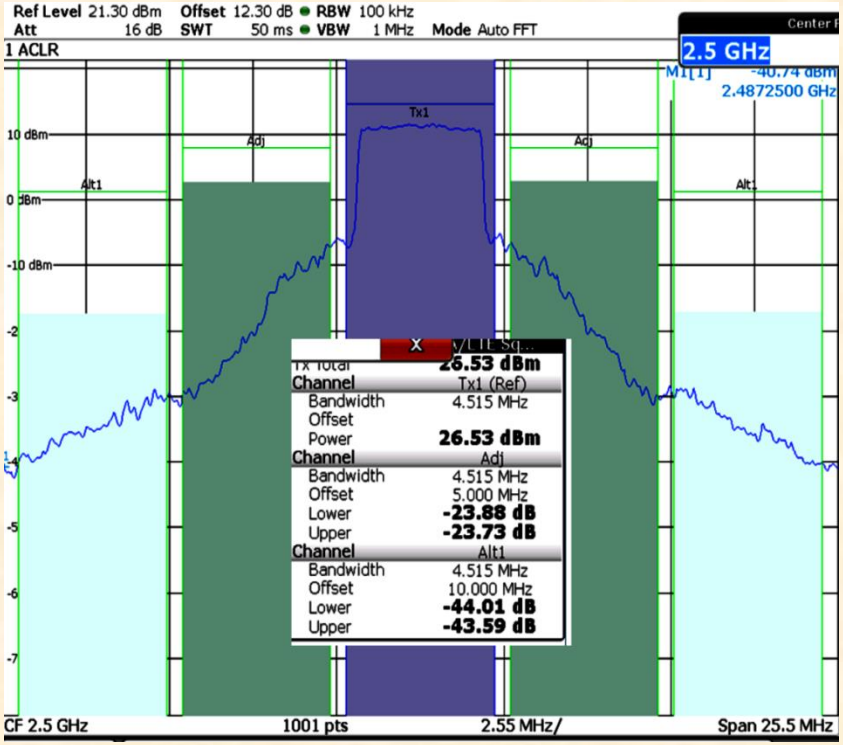


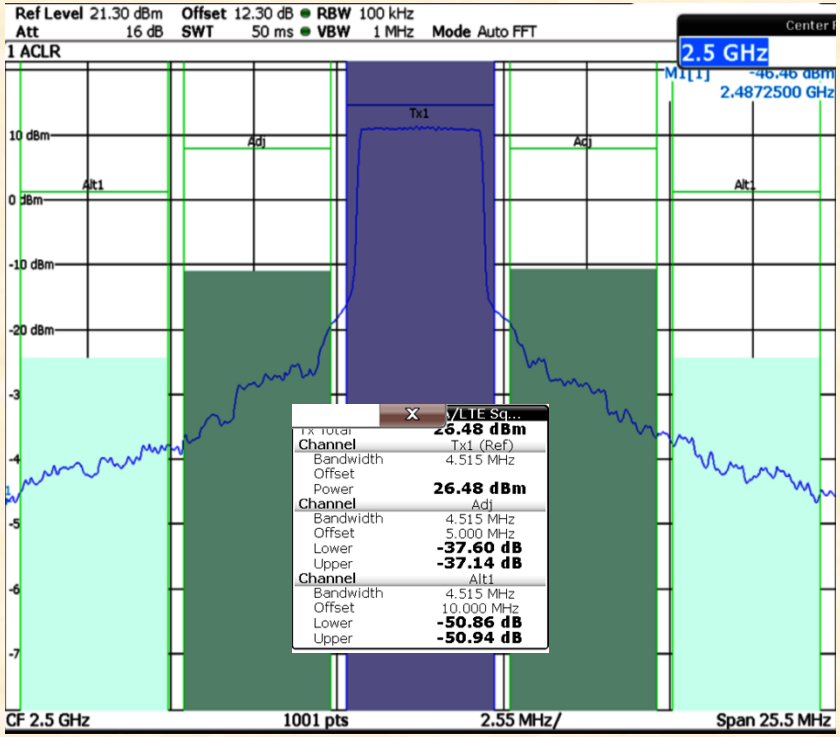
Size: 1.7 x 1.6 mm²



3. Fully integrated broadband CMOS Class-E power amplifier

LTE test data: 16 QAM, 26.5 dBm, 2.5 GHz, V_{dd} = 2.7 V





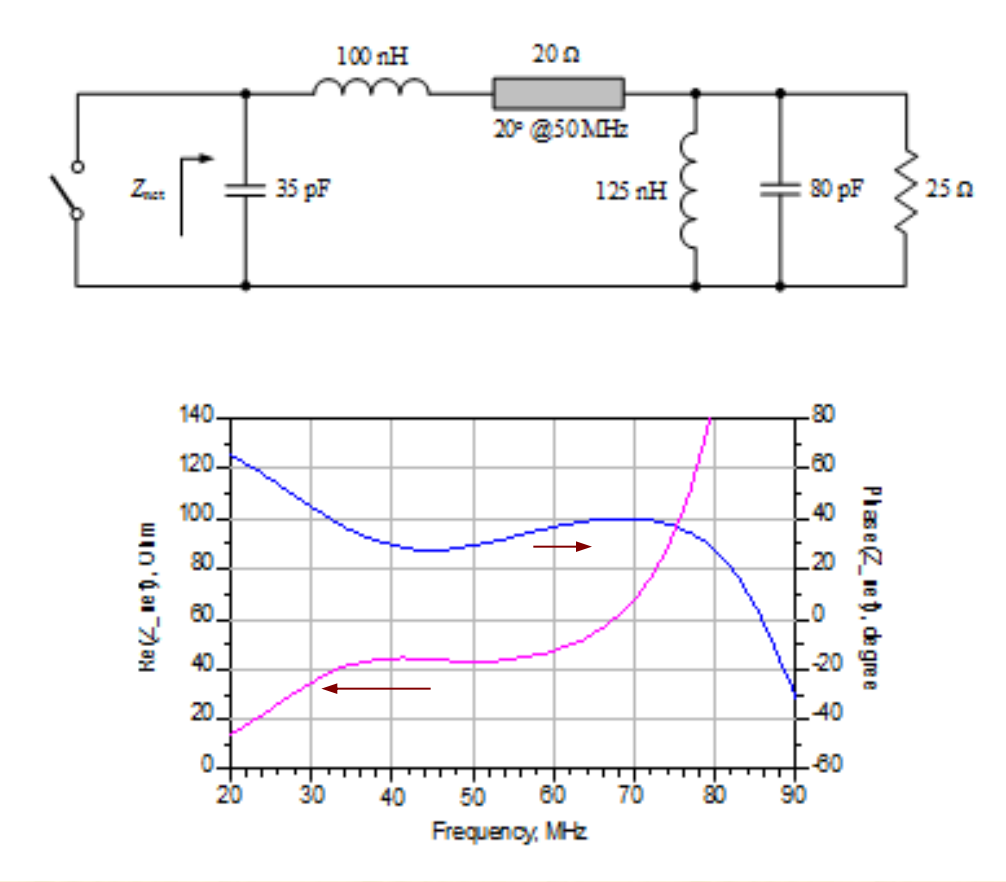
ET disabled

ET enabled

35% overall efficiency
41.5% PA efficiency
ACLR1: 13-dB improvement
ACLR2: 7-dB improvement

4. Broadband Class-E power amplifier with series inductance

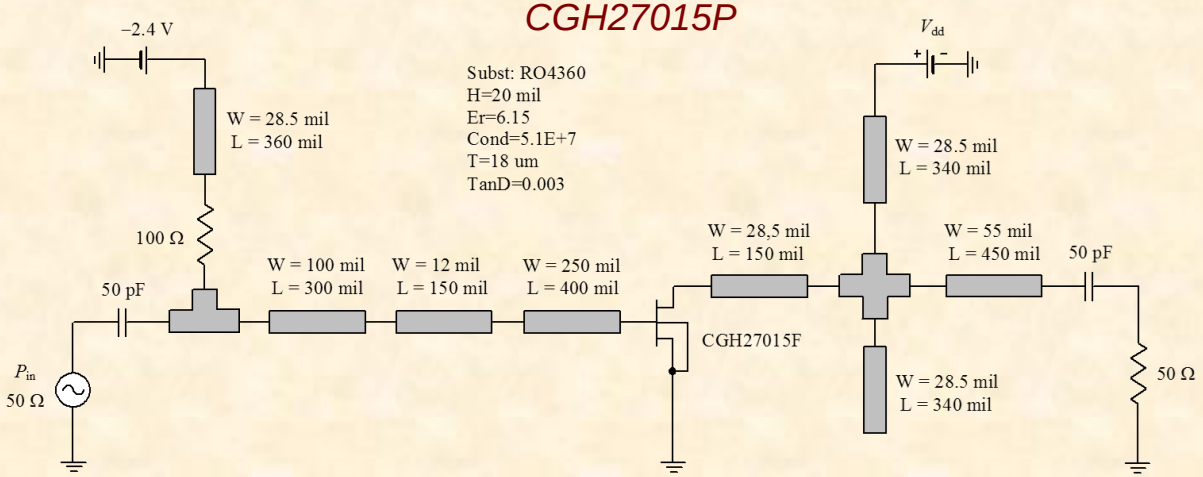
Reactance compensation load network with series inductance

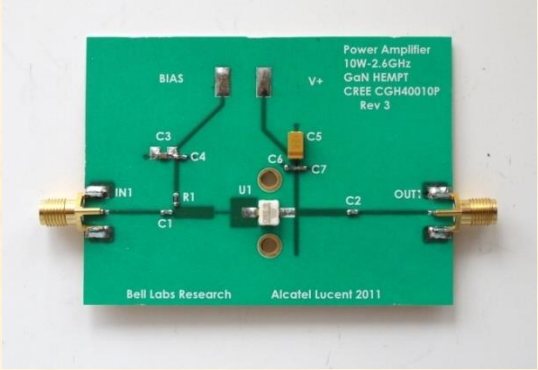


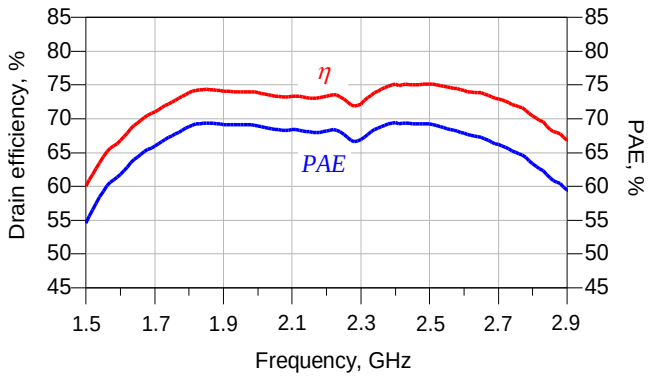
- *useful for packaged devices with series lead inductance*
- *shunt inductance and capacitance can be replaced by short-circuit and open-circuit stubs at microwaves*

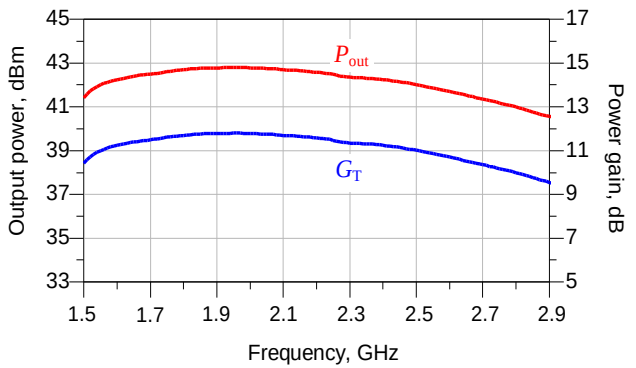
4. Broadband Class-E power amplifier with series inductance

Cree GaN HEMT
CGH27015P





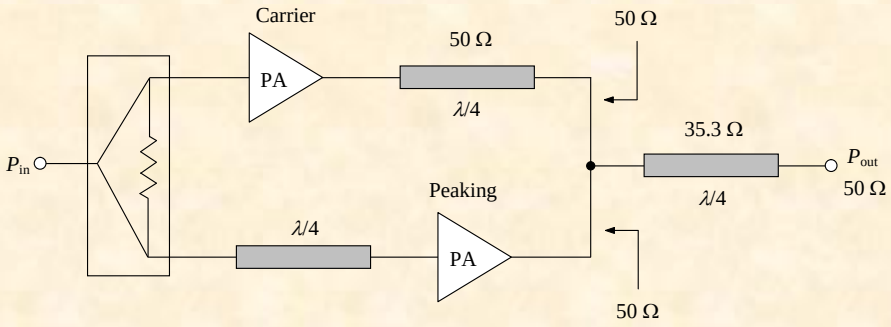




- *Bandwidth: 1.7–2.7 GHz*
- *Drain efficiency = 73±2%*
- *Power gain = 11±0.8 dB*
- *Output power = 42±0.8 dBm*

5. Broadband parallel Doherty amplifier

Classical Doherty architecture



Impedance transformation

high-power region

(carrier and peaking PAs are ON):

50 Ω ⇒ 25 Ω ⇒ 50 Ω

low-power region

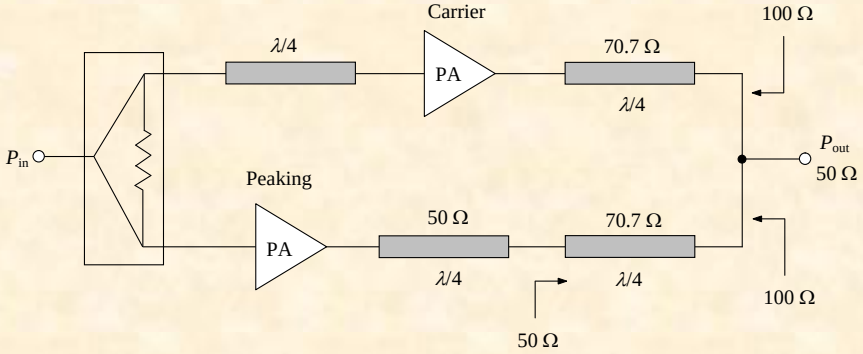
(carrier PA is ON and peaking PA is OFF):

100 Ω ⇒ 25 Ω ⇒ 50 Ω

Impedance transformation ratio = 4

Loaded quality factor $Q_L = \sqrt{4-1} = 1.73$

Parallel Doherty architecture



Impedance transformation

high-power region

(carrier and peaking PAs are ON):

50 Ω ⇒ 100 Ω ⇒ 50 Ω

low-power region

(carrier PA is ON and peaking PA is OFF):

100 Ω ⇒ 50 Ω

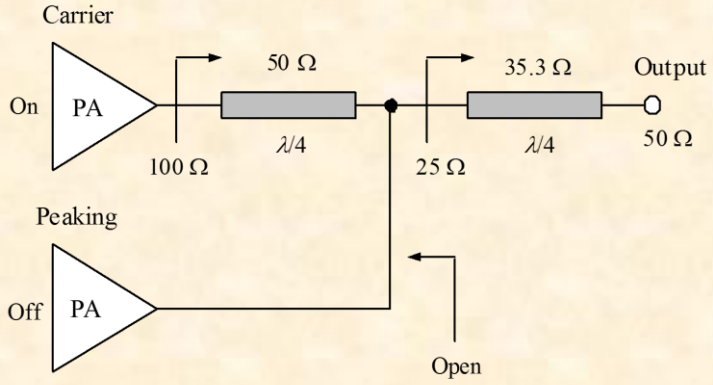
Impedance transformation ratio = 2

Loaded quality factor $Q_L = \sqrt{2-1} = 1$

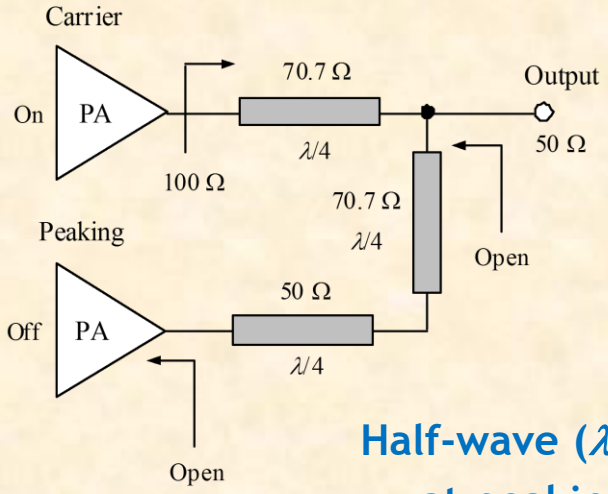
5. Broadband parallel Doherty amplifier

Low-power region (peaking amplifier is OFF)

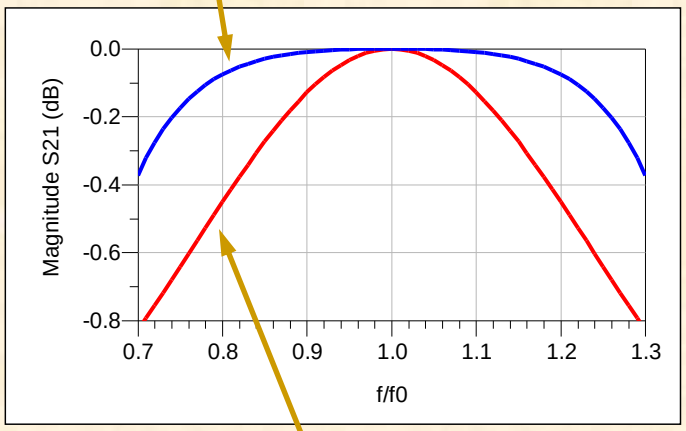
Classical



Parallel



Parallel Doherty PA

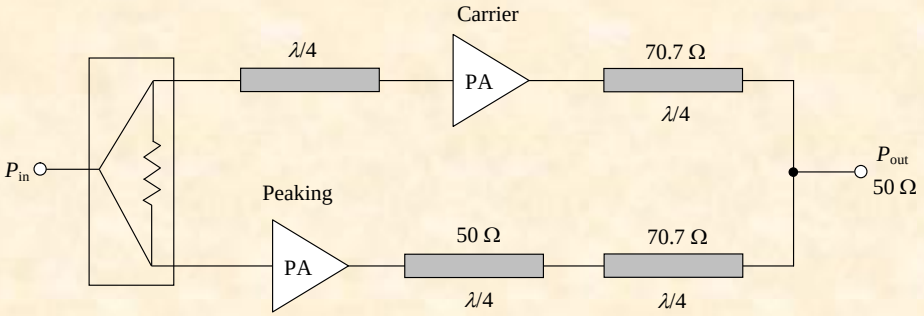


Classical Doherty PA

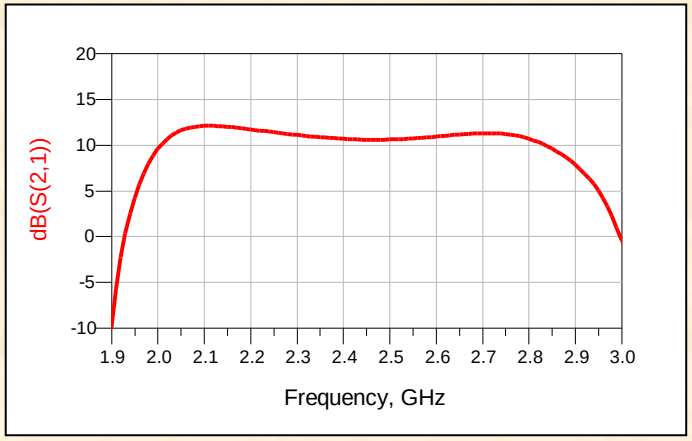
Half-wave ($\lambda/4 + \lambda/4$) line translates open circuit at peaking amplifier output to carrier path

5. Broadband parallel Doherty amplifier

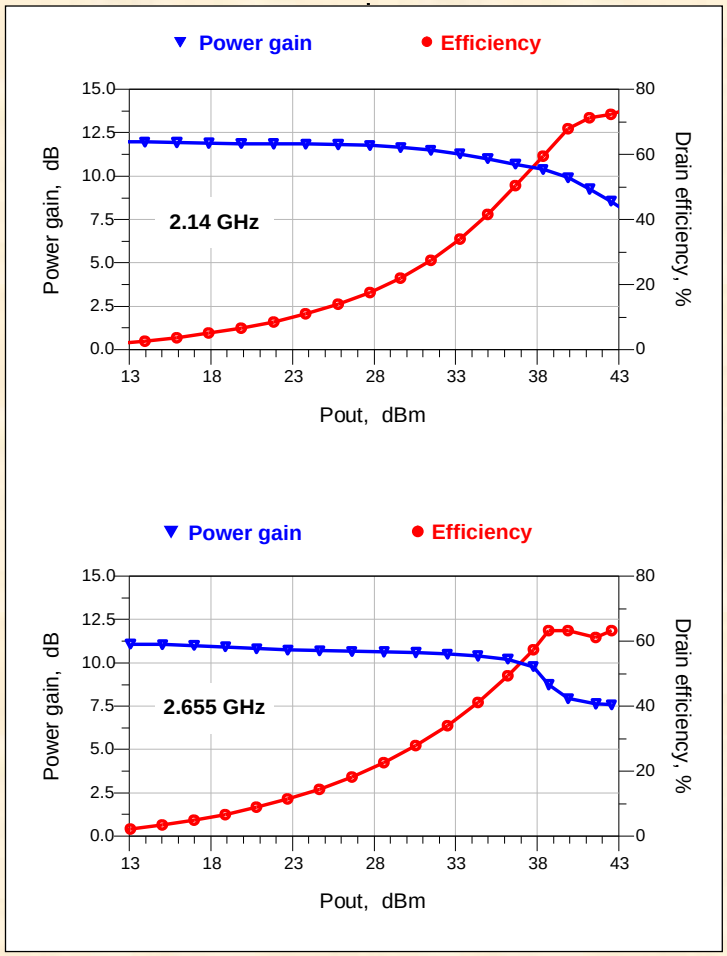
Parallel Doherty architecture based on broadband Class-E amplifiers with 15-W Cree CGH27015P devices: simulation



Small-signal S_{21}



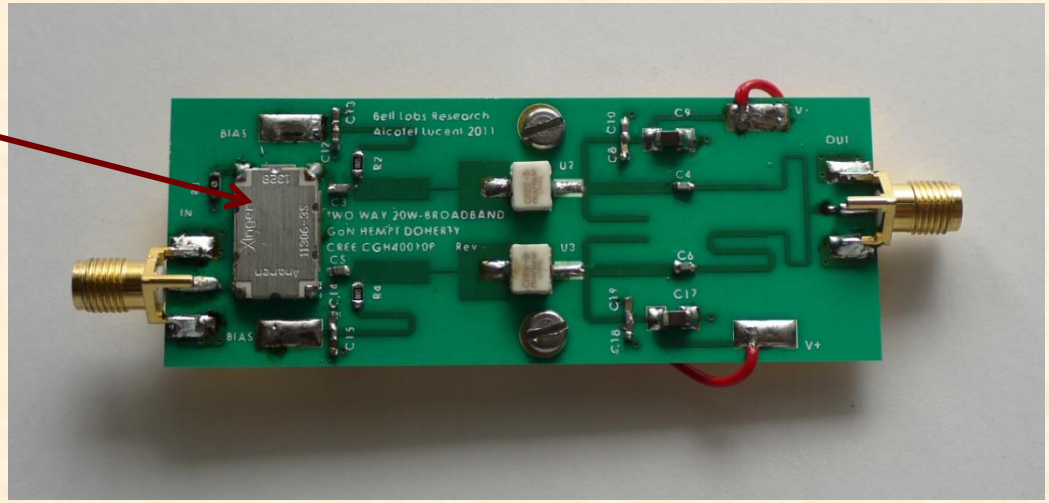
2.0-2.8 GHz

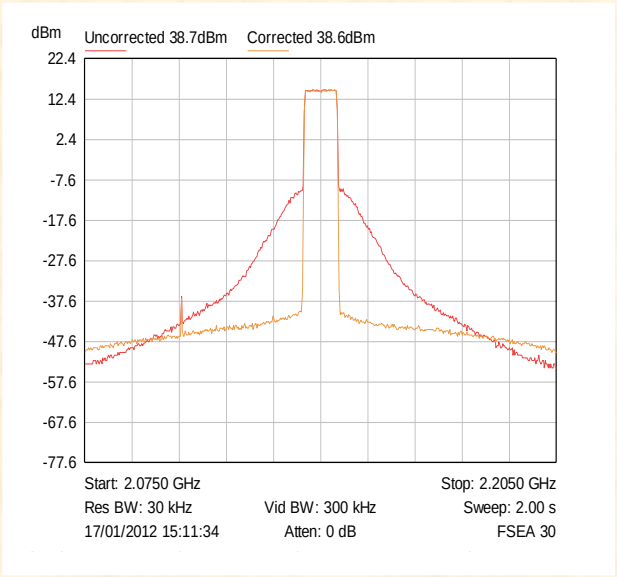


5. Broadband parallel Doherty amplifier

Parallel Doherty architecture based on broadband Class-E amplifiers with 15-W Cree CGH27015P devices: test board

Broadband (2-4 GHz)
Anaren 3-dB coupler



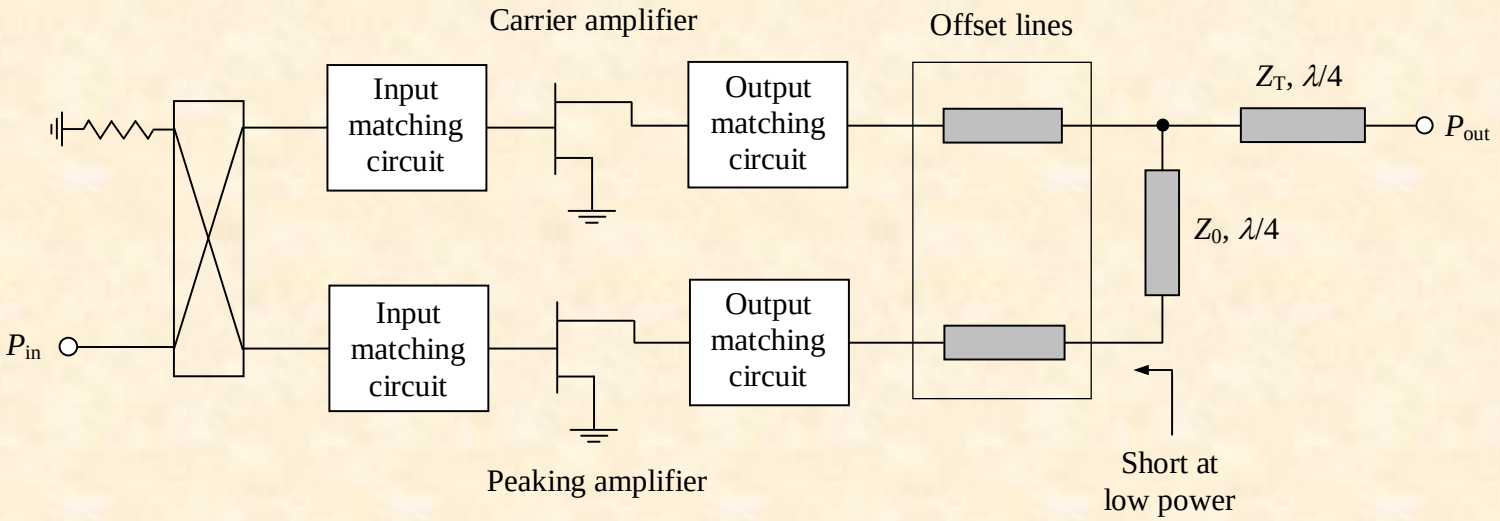


2.14 GHz
10-MHz LTE signal

Single-carrier 5-MHz WCDMA signal, PAR = 6.5 dB:

- V_{dd} = 28 V
- P_{out} = 39 dBm
- Gain = 10 dB
- Drain efficiency = 45% (2.14 GHz) 40% (2.655 GHz)
- ACLR = -32 dBc -29 dBc

6. Inverted Doherty amplifier architecture

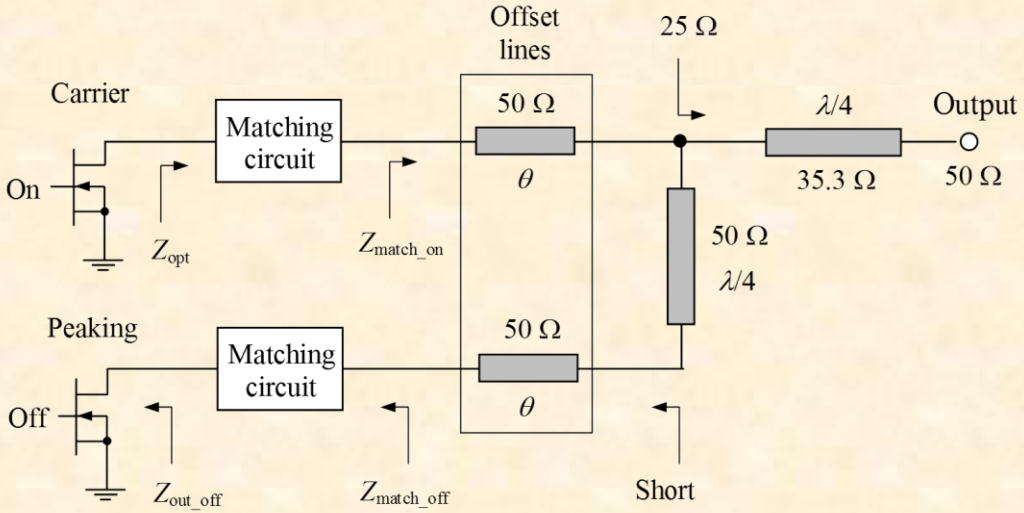


- ***quarterwave transmission line is connected to output of peaking amplifier if it is easier to provide short-circuit condition instead of open circuit for peaking amplifier in low-power region***

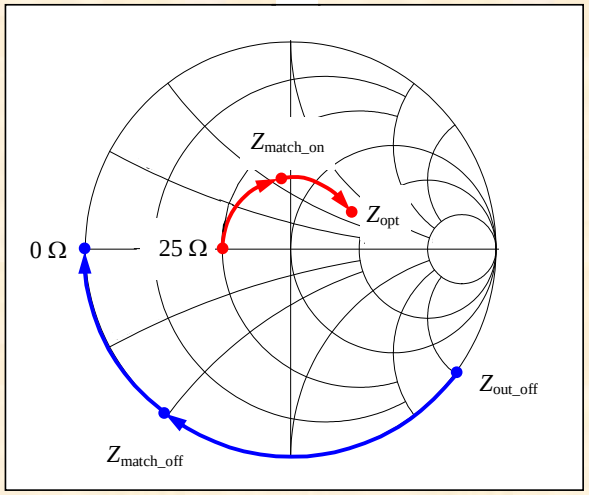
- ***offset lines are necessary to compensate for peaking device parasitics and provide open-circuit condition seen by carrier amplifying path in low-power region***

- ***required 90° phase shift is provided in input circuit of carrier amplifier***

6. Inverted Doherty amplifier architecture



✓ *carrier device should see high impedance in low-power region providing by output matching circuit*



✓ *offset line is necessary to compensate for peaking device parasitics and provide short-circuit condition at its output in low-power region*

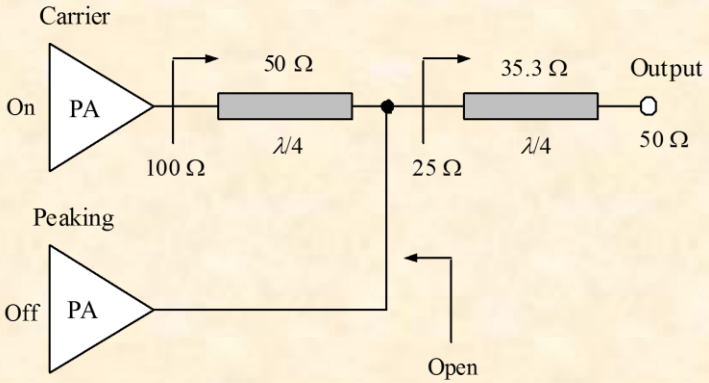
✓ *for three-stage inverted Doherty amplifier, drain efficiency of 40% with power gain of 9 dB achieved at 42 dBm (8.5 dB backoff) at 2.14 GHz*

M.-W. Lee, S.-H. Kam, Y.-S. Lee, and Y.-H. Jeong, "Design of Highly Efficient Three-Stage Inverted Doherty Power Amplifier," IEEE Microwave Wireless Components Lett., vol. 21, pp. 383-385, July 2011

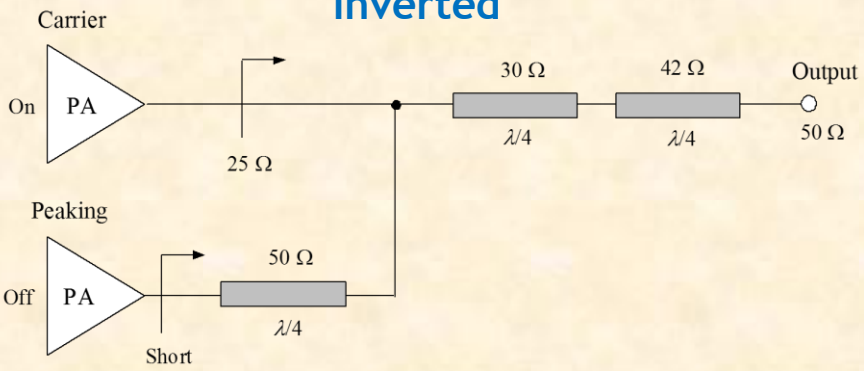
7. Broadband inverted GaN HEMT Doherty amplifier

Low-power region (peaking amplifier is OFF)

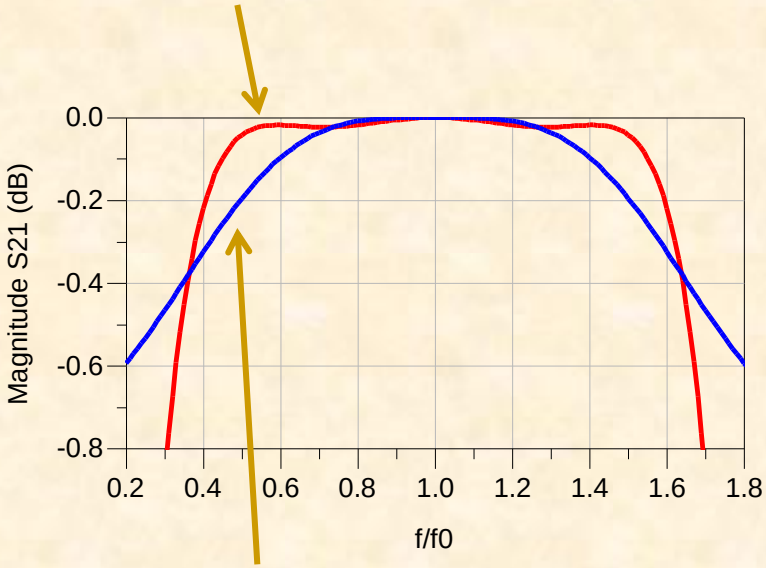
Classical



Inverted



Inverted Doherty PA

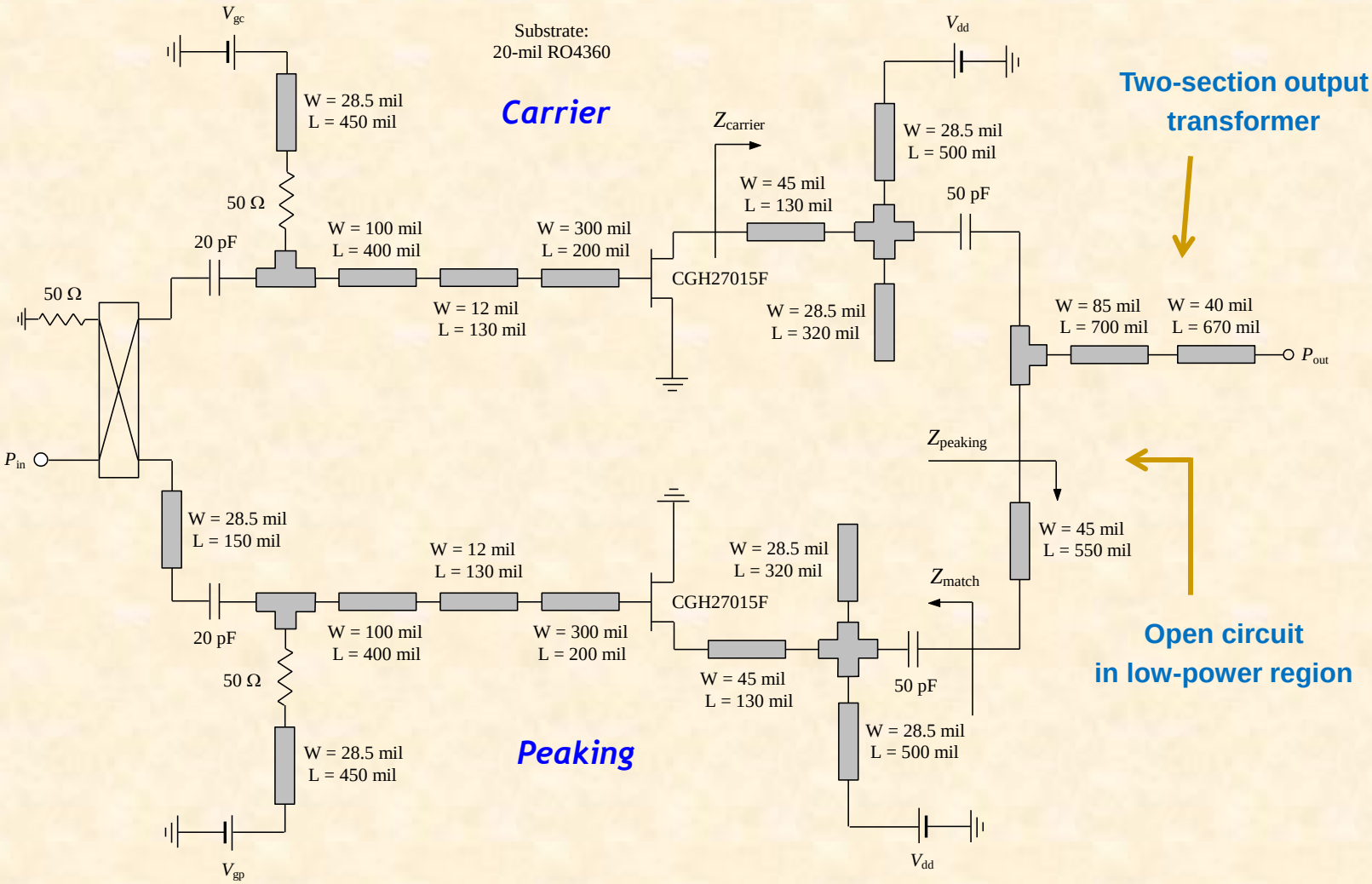


Two-section output transformer
(25 Ω → 50 Ω)

Quarterwave line translates short circuit at peaking amplifier output to open circuit seen by carrier path and extends bandwidth

7. Broadband inverted GaN HEMT Doherty amplifier

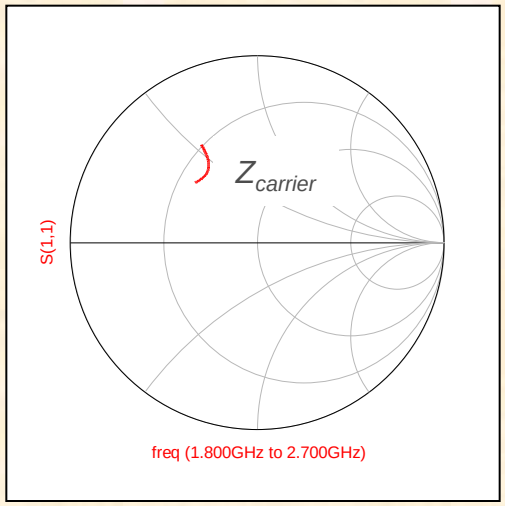
Circuit schematic using two broadband Class-E power amplifiers for carrier and peaking amplifying paths

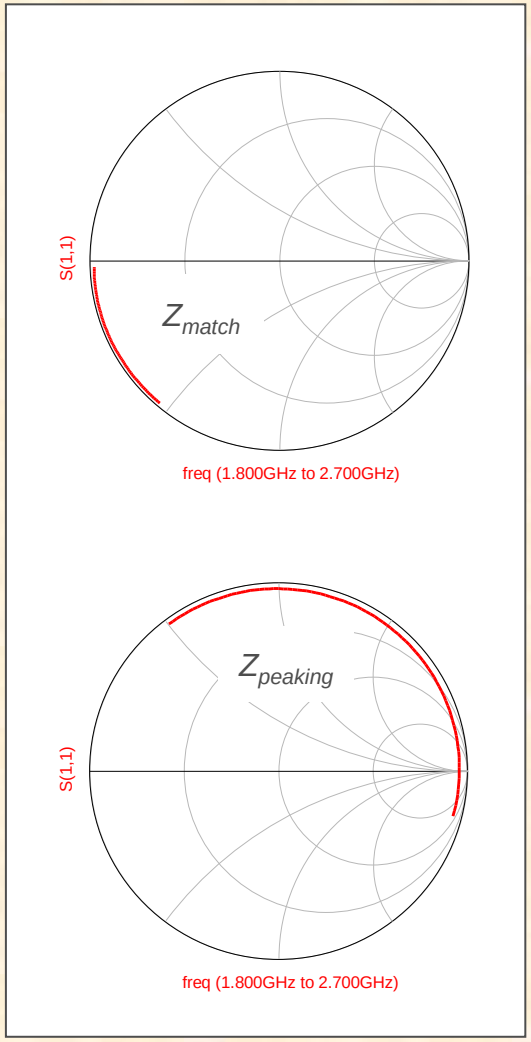


7. Broadband inverted GaN HEMT Doherty amplifier

Inverted Doherty architecture based on broadband Class-E amplifiers with 15-W Cree CGH27015P devices: simulation

Inductive impedance at fundamental seen by carrier device in low-power region





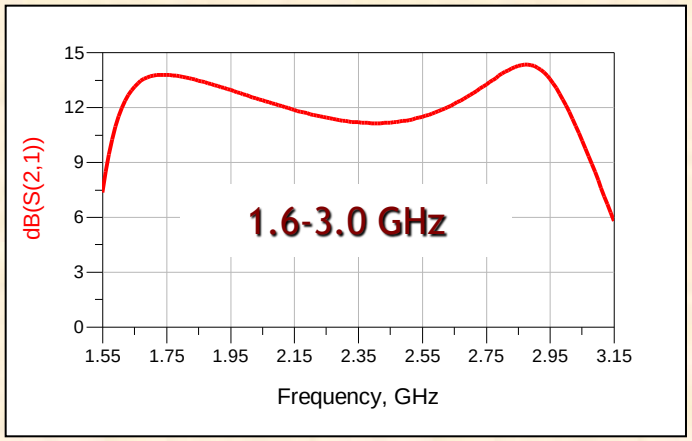
Low reactance seen at peaking amplifier output in low-power region

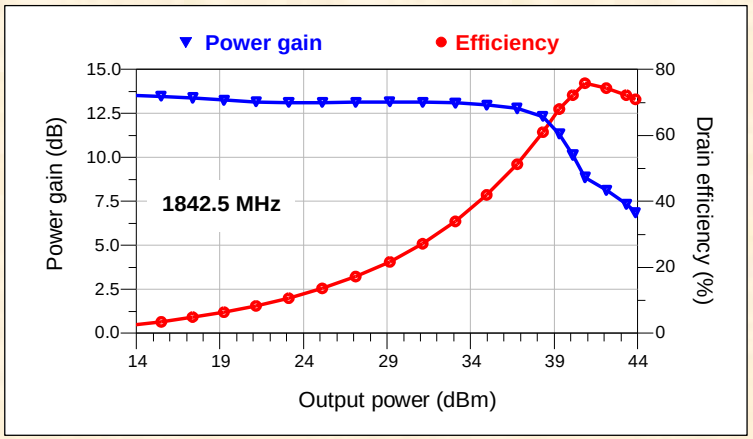
High reactance presented by peaking amplifying path in low-power region

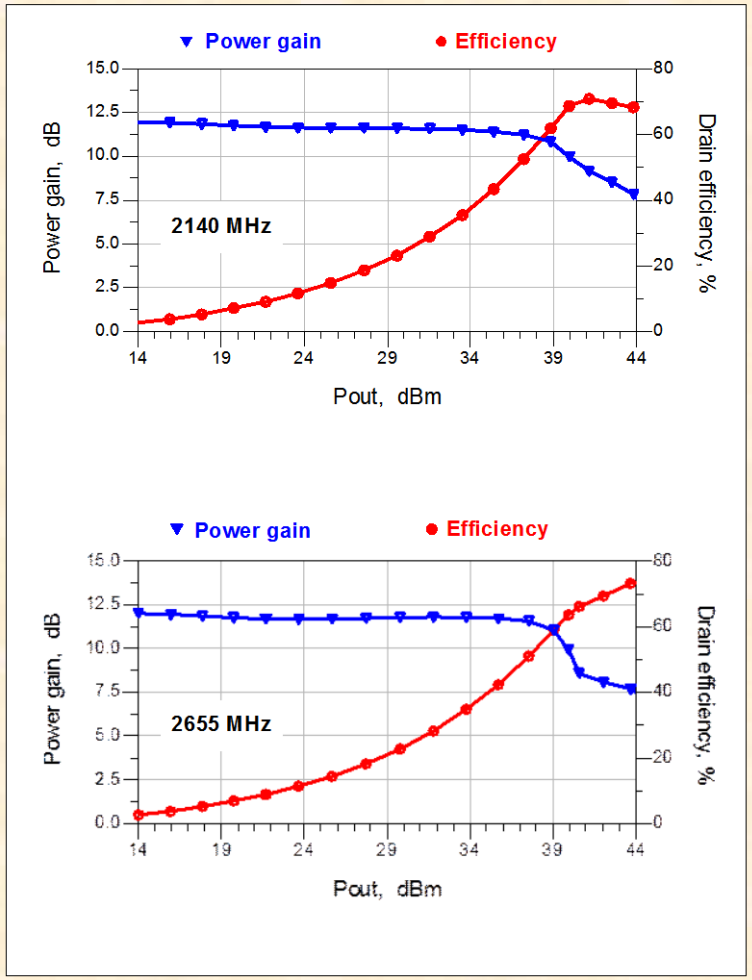
7. Broadband inverted GaN HEMT Doherty amplifier

Inverted Doherty architecture based on broadband Class-E amplifiers with 15-W Cree CGH27015P devices: simulation

Small-signal S_{21}



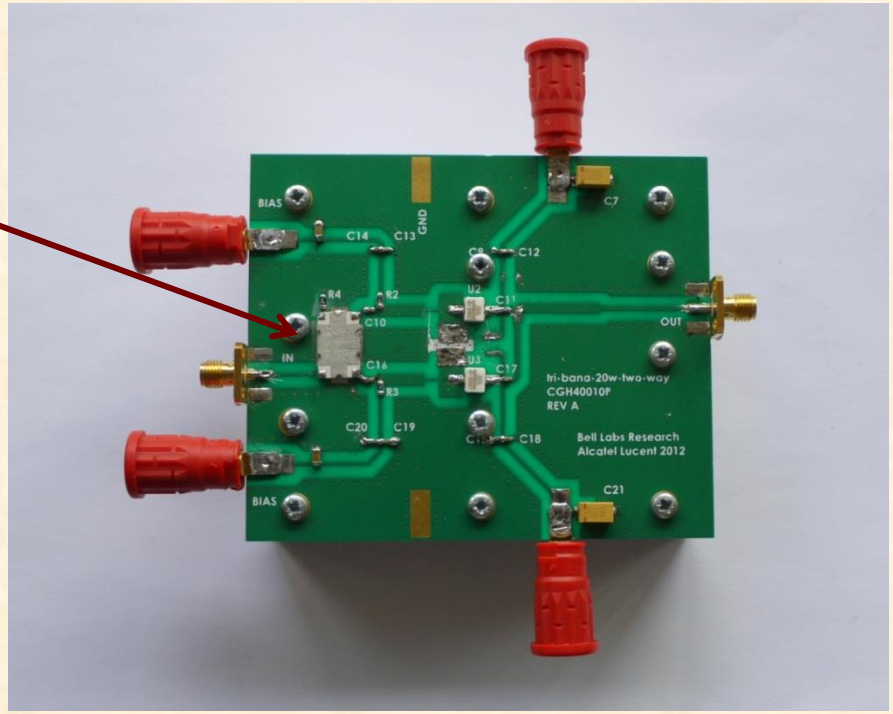




7. Broadband inverted GaN HEMT Doherty amplifier

Inverted Doherty architecture based on broadband Class-E amplifiers with 15-W Cree CGH27015P devices: test board

Broadband
(690-2700 MHz)
Anaren 3-dB coupler



Single-carrier
5-MHz WCDMA signal
PAR = 6.5 dB:

V_{dd} = 28 V
P_{out} = 38 dBm
Gain = 11 dB

Drain efficiency =	***52% (1.85 GHz)***	***50% (2.15 GHz)***	***42% (2.65 GHz)***
ACLR =	***-32 dBc***	***-34 dBc***	***-37 dBc***