<u>Session</u>: Millimeter-Wave PAs for 5G and Beyond

Large-Signal Performance of AlInN/GaN-on-Silicon HEMTs at 94 GHz

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Considerations / Outline

- AllnN/GaN Materials
 - Lattice-Matching to GaN
 - Reduced Surface Depletion vs. AlGaN/GaN

Requirements for mm-Wave HEMTs

- Gate-Channel Spacing / Source-Drain Separation
- Short-Channel Effects (SCEs)
- Series Resistances / Ohmic Contacts (Annealed vs. Regrown)
- Large-Signal on Silicon (W-Band)
- PDK and W-Band Prototype on Silicon

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Lattice Matching (Al_{0.83}In_{0.17}N:GaN)



Materials

Lattice Matching: A Reliability Enhancer (?)



G. Meneghesso et al.



Park et al. (TRIQUINT)

Cumulative Strain (Mismatch + Piezo) Correlated to Device Degradation

Materials AllnN/GaN High Temperature Stability (1000°C)



F. Medjdoub et al., IEDM 2006

AllnN/GaN HEMTs Survive 1000°C Temperatures

(Potential for High-T Electronics)

Materials

Substrate Choices



Silicon:

1,030 cm²/Vs @ 2×10^{13} /cm² 300 Ω / \Box (–17% mismatch)

SiC: 1,300 cm²/Vs @ 2.4×10¹³ /cm² 205 Ω/□ (-3.5% mismatch)

Excellent Mobility in 2DEG: Dislocations are screened by the high carrier density

Appl. Phys. Lett. 89, 062106 (2006)

Materials

Surface Depletion: InP vs. GaAs HEMT Analogy



Ultra-High-Speed Modulation-Doped Field-Effect Transistors: A Tutorial Review

LOI D. NGUYEN, MEMBER, IEEE, LAWRENCE E. LARSON, SENIOR MEMBER, IEEE, AND UMESH K. MISHRA, SENIOR MEMBER, IEEE

Proc. IEEE, p.494 (1992)

Reduced Gate-to-Channel Distance

Theoretical Advantages:

- Higher G_M
- Higher Current Drive, I_{DMAX}
- Improved Aspect Ratio L_G/d
- Weaker Short-Channel Effects
- Textbook Approach to High-Speed

All Recent Record GaN HEMTs:

- Thin Barriers (AlInN or AlN)
- Higher Channel Sheet Density

Requirements: Reduced S/D Spacing



The Original Studies of R_s and R_D Effects on GaN HEMT Bandwidth...

(Essentially, re-work Hughes/Tasker pHEMT analysis)

Transistor Delay Analysis and Effective Channel Velocity Extraction in AlGaN/GaN HFETs

^{1,2)}C.R. Bolognesi, ¹⁾A.C. Kwan, ²⁾D.W. DiSanto

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 53, NO. 12, DECEMBER 200

At-Bias Extraction of Access Parasitic Resistances in AlGaN/GaN HEMTs: Impact on Device Linearity and Channel Electron Velocity

David W. DiSanto, Member, IEEE, and C. R. Bolognesi, Senior Member, IEEE

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Ohmic Contacts (1)

annealed contact **Metallization:** metal alloy Ti / Al / Mo / Au **Yields** epilayer $R_{\rm C} \approx 0.3$ to 1 Ω ·mm 200 nm (strong variability) annealed spikes Cross-sectional SEM image 1 µm Molybdenum FIB cut Oxygen Titanium Top-view SEM image

Aluminum

Requirements:

- Good Morphology
- Low Contact Resistance

Rapid Thermal Annealing T ~ 850°C

Gold

EDX

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Regrown: Ti/Au R_{REG} R^{INT} Barrier n⁺⁺-GaN 2DEG GaN buffer

Regrown Contacts ⁽²⁾





Beneficial for Short L_{SD} Spacings ($R_{SD} < R_{C}$) Better Reproducibility with Respect to Annealed Ohmics

(Best Example: Shinohara et al., HRL)



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Regrown Contacts ⁽³⁾



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 - Large-Signal on Silicon (94 GHz / W-Band)

Large-Signal Operation



Large-Signal Operation

(On Silicon)

d = 7.5 nm, $L_{G} = 50$ nm, $L_{SD} = 2 \mu m$ on HR-Silicon.

Improved Buffer / Channel Design. Regrown Contacts.



+ G_M > 650 mS/mm + Adequate Pinch-Off

+ Good Transport: μ = 1200 cm²/Vs (300 Ω /sq) + Back-Barrier not Implemented

Large-Signal Operation

 $d = 7.5 \text{ nm}, L_G = 50 \text{ nm}, L_{SD} = 2 \mu \text{m}$ on HR-Silicon. Improved Back-Buffer / Channel Design. Regrown Contacts Power gain (Gp), output power (Pout), power added efficiency (PAE) at VGS = -1.2 V and VDS = 9V at 94 GHz for a 50 nm gatelength device, with source-drain spacing of 2 µm, source-gate spacing 0.5 µm and a total gate width of 100 µm



94 GHz Initial Results

1 W/mm / PAE = 12% / G_P = 4 dB @ $P_{IN,Del}$ = 16 dBm (Better than 1 W/mm Result on SiC)

Large-Signal Operation

@ 94 GHz on SiC

 $d = 6 \text{ nm}, L_{\text{G}} = 100 \text{ nm}, L_{\text{SD}} = 1 \text{ }\mu\text{m} \text{ on SiC}.$

No Back-Barrier. Regrown Contacts.



Best results at 94 GHz for AlInN-based HEMTs on SiC

PDK and PA Prototype Development ⁽¹⁾



Large-Signal Model (Angelov) Harmonic Balance Simulation in ADS) vs. Load Pull Measurement at 94 GHz for a 2x50um AlInN/GaN on Si device.

Process Design Kit PDK

Scalable Large-Signal Model (Gate Width & Fingers)

PDK and PA Prototype Development ⁽²⁾

MMIC Process based on Grounded Coplanar Waveguides



PDK and PA Prototype Development ⁽³⁾



Input, Inter-Stage and Output Networks Simulated with Lumped Elements (Full Characterization and Modeling of Passives Elements are Underway)

PDK and PA Prototype Development ⁽⁴⁾

• 3 Stage PA Simulation Results



• Additional Losses of 1 to 3 dB Expected with Lossy Interconnects in Implementation.

Conclusions

- Excellent Progress with mm-Wave AlInN/GaN HEMTs
 - Process Integration Developments (Back-Barrier / Regrown Ohmics)
- GaN-on-Silicon is mm-Wave Ready
- Impressive P_{OUT} at 94 GHz on Silicon (1.3 W/mm)
- Improved Large-Signal Stability
- PDK and PA Prototype Development on Silicon
 - W-Band Gain Block Feasible: 15 dB at W-Band
 - Refinements Required