

A 1.1-Gbit/s, 23-dBm, 10-GHz Outphasing Modulator with 60-dB Dynamic Range

Mohammad Mehrjoo, Samet Zehir

Gabriel Rebeiz, James Buckwalter

Department of Electrical and Computer Engineering

University of California, San Diego



Outline

- **Introduction**
- **System level of the proposed modulator**
- **Circuit design of the key building blocks**
- **Measurement results**
- **Conclusion**

Introduction

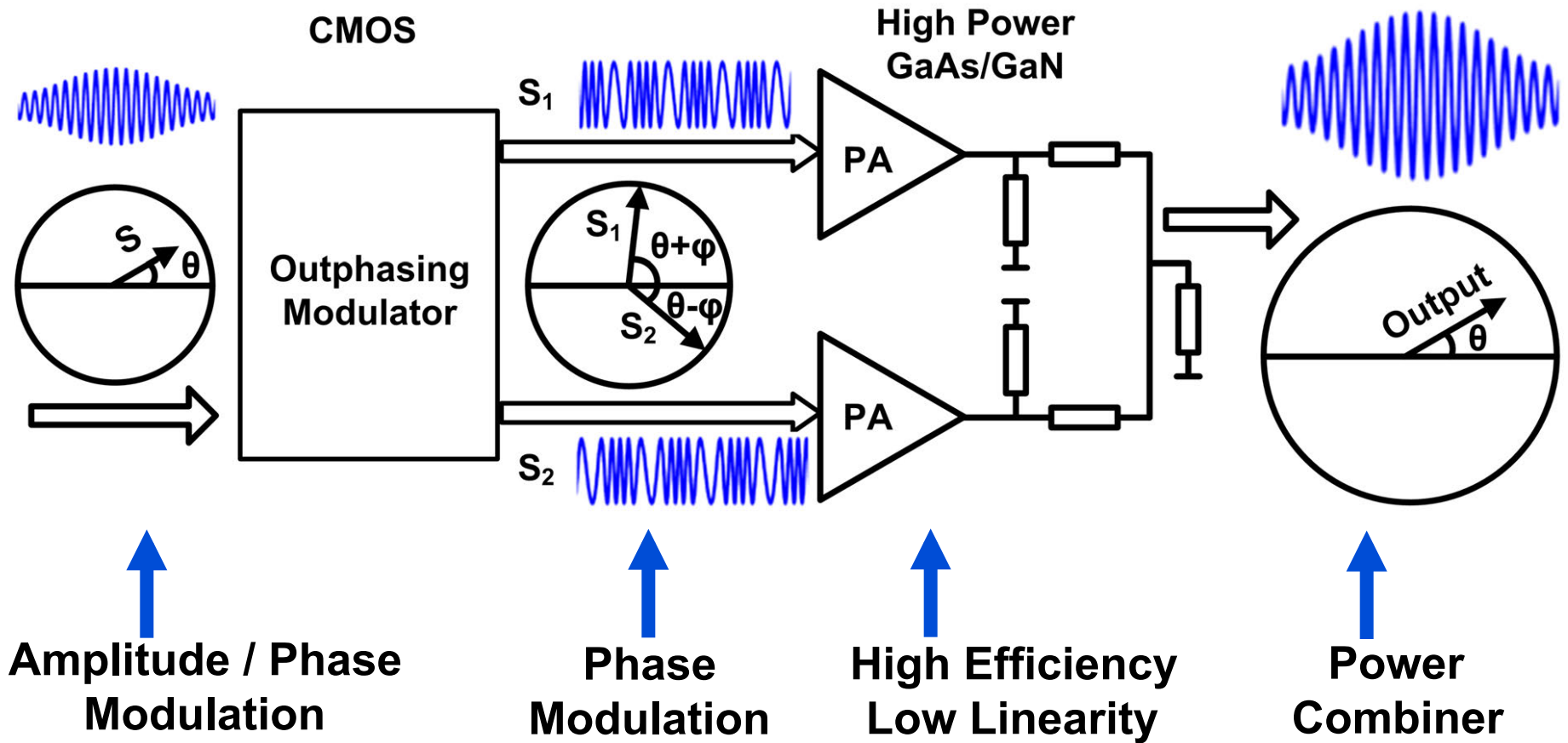
- Tradeoff between linearity and efficiency in PAs.

	Linearity	Efficiency	Modulation
PA class A, AB	high	low	Amplitude
PA class D, E	low	high	Phase

OFDM, multi-channels of QAM, high PAPR → High linear PAs

- Two low linearity high efficiency PAs, rather than one high linearity low efficiency PA.
- Outphasing, Linear Amplification with Nonlinear Components (LINC)

Outphasing Concept

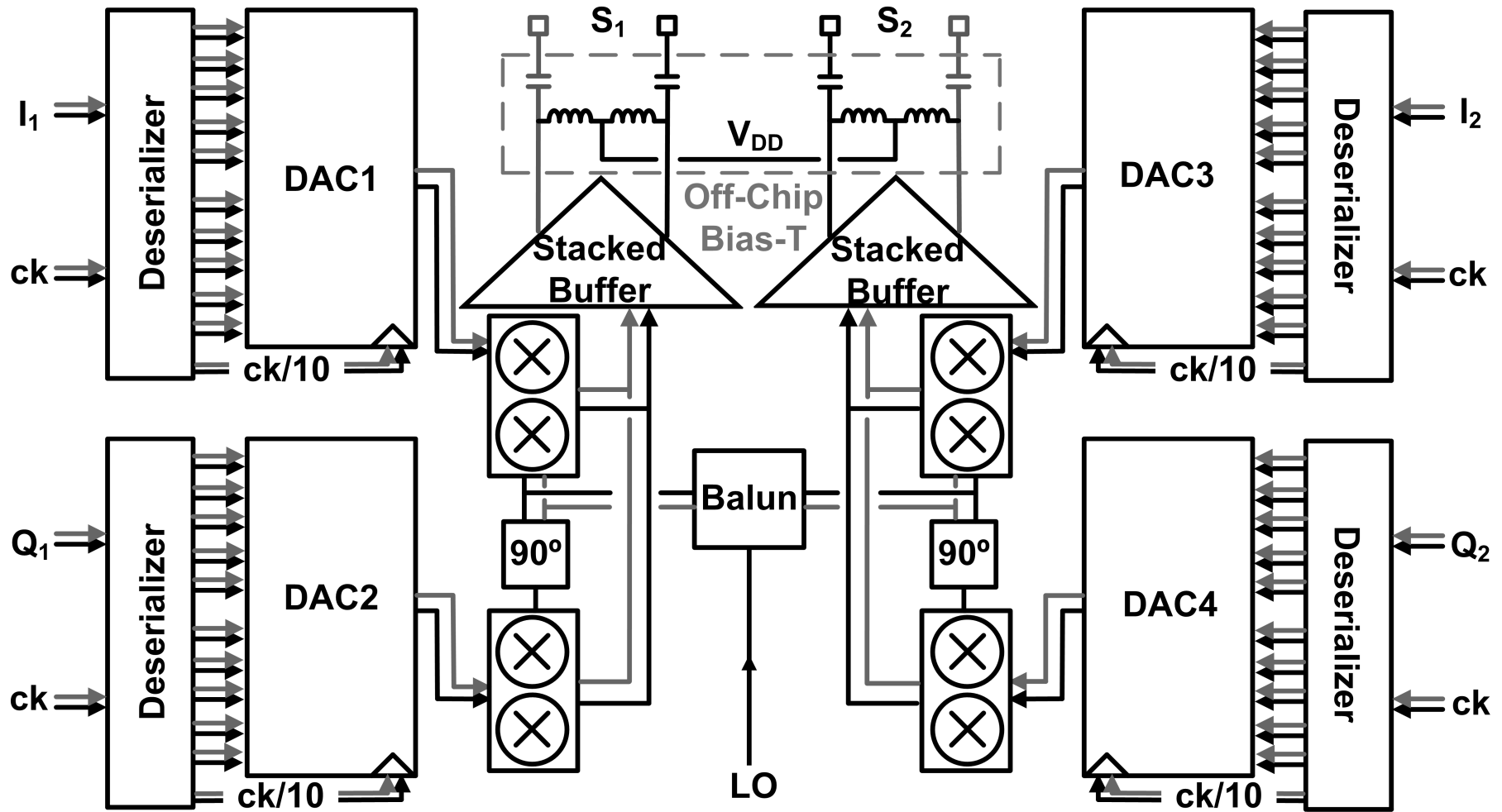


$$S_1(t) = \frac{A_{max}}{2} \cos(\omega t + \theta(t) + \phi(t))$$

$$S_2(t) = \frac{A_{max}}{2} \cos(\omega t + \theta(t) - \phi(t))$$



$$\phi(t) = \arccos(A(t)/A_{max})$$

Block Diagram



Submitted, JSSC

Key Building Blocks (Baseband)

- **Digital-to-analog-converter (DAC)**
- **How many bits are needed?**
- **DR  Phase Error**
- **Phase Resolution  DAC number of bits**
- **DAC floor plan.**

DR as a Function of the Phase Error

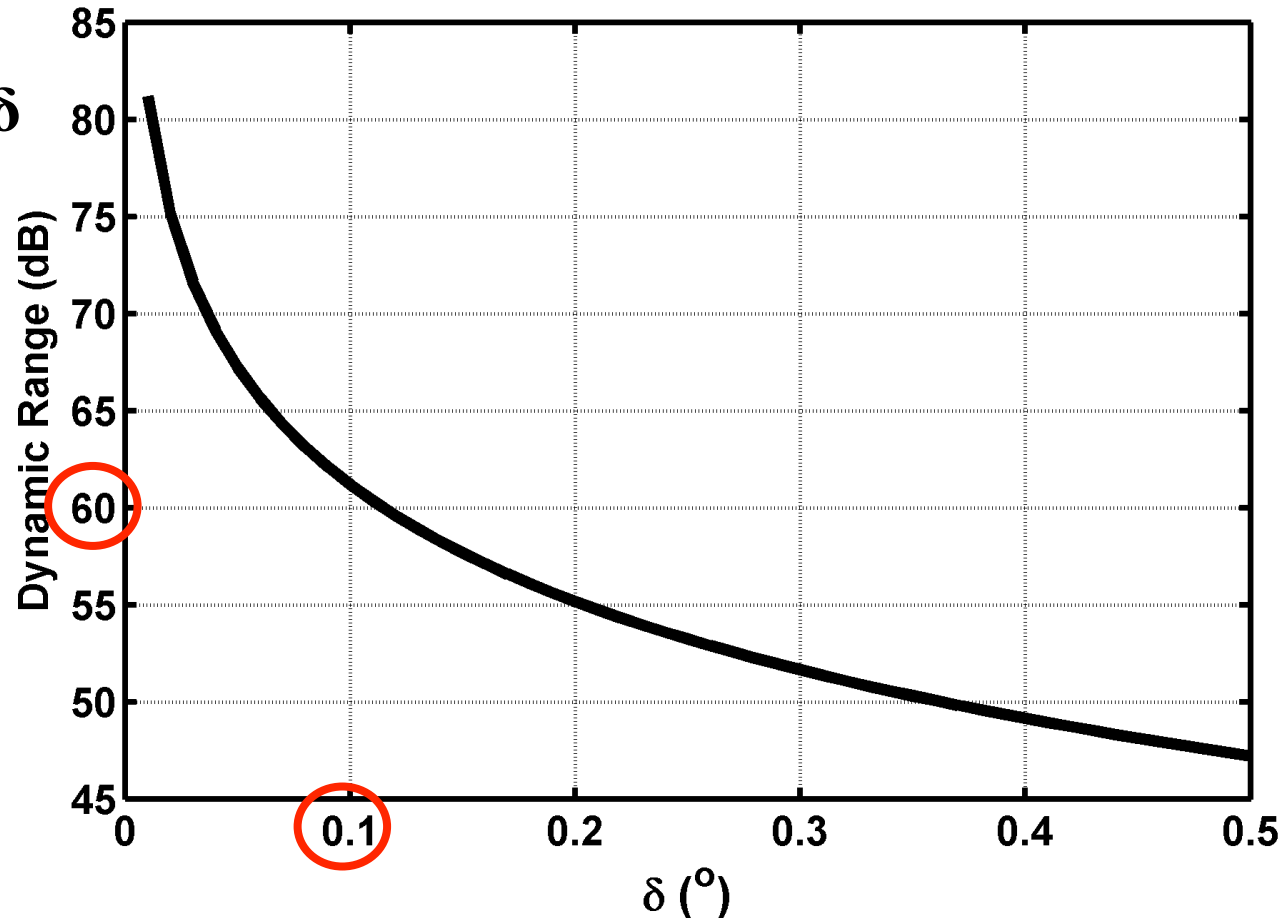
Outphased signals in the presence of phase error:

$$S_1(t) = \frac{A_{max}}{2} \cos(\omega t + \theta(t) + \phi(t))$$

$$S_2(t) = \frac{A_{max}}{2} \cos(\omega t + \theta(t) - \phi(t) + \delta)$$

DR as a function of δ

$$DR = 10 \log_{10} \frac{4}{\delta^2}$$

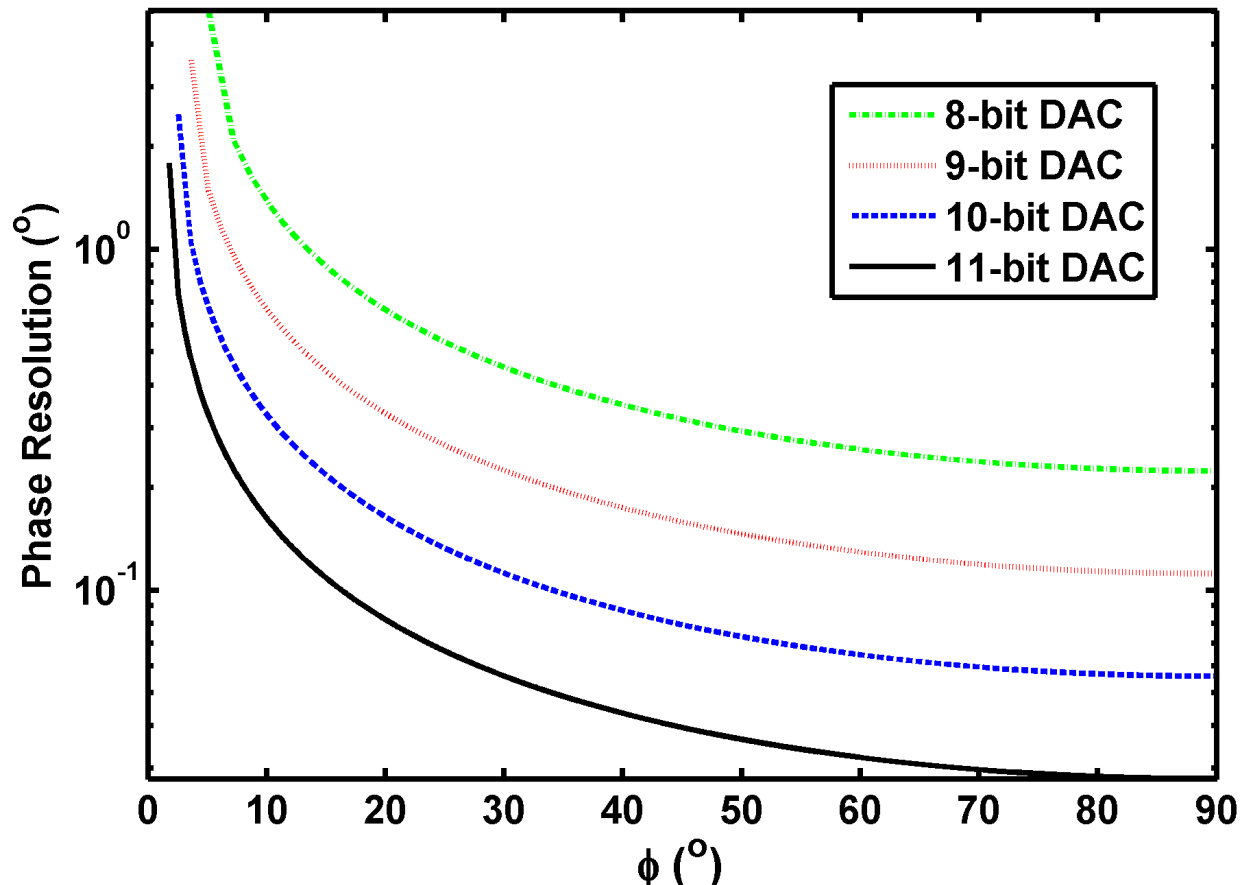


Phase Res. vs Outphasing Angle

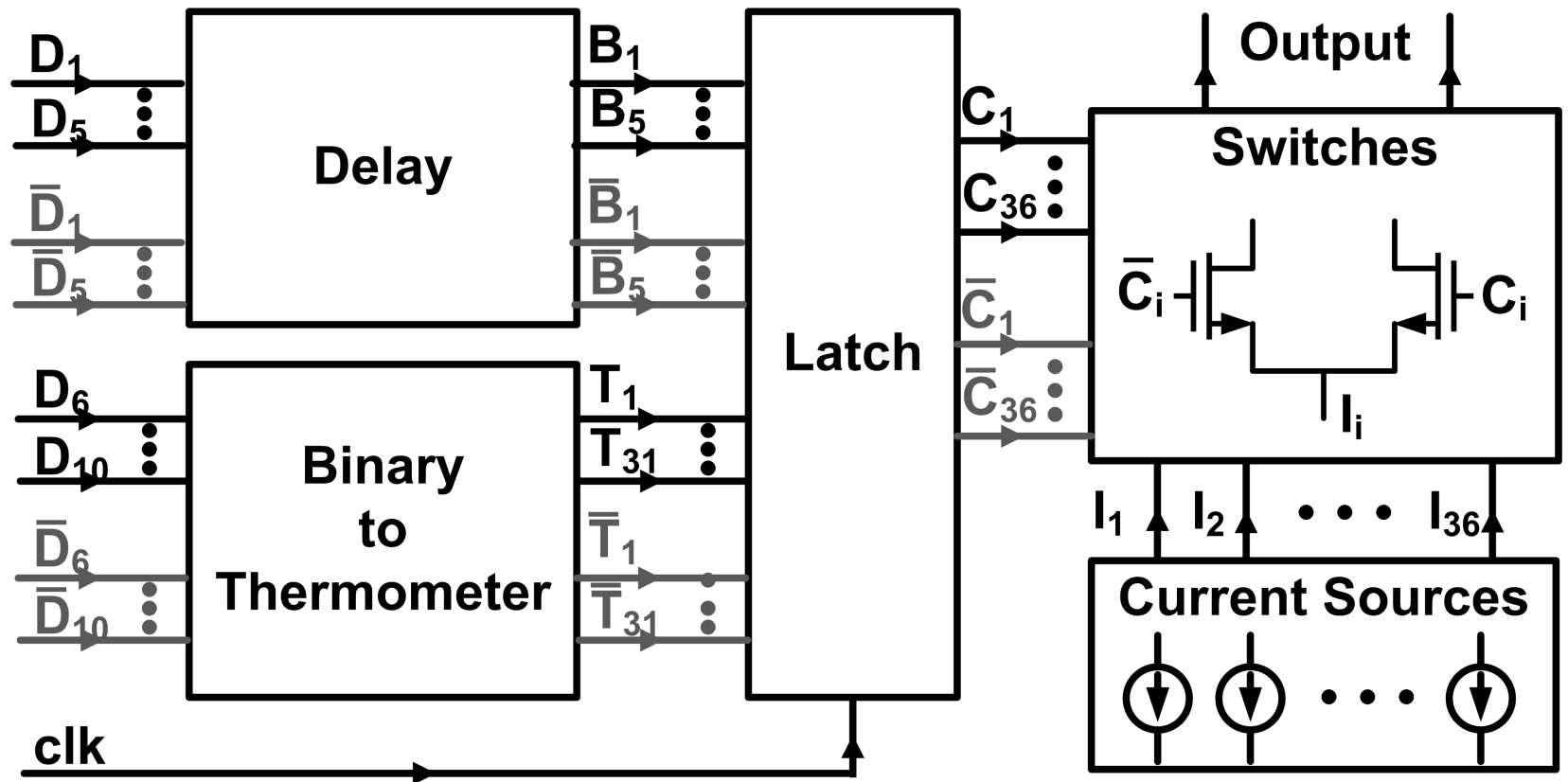
The phase resolution provided by a DAC is higher as Φ increases.

Phase resolution at Φ close to 90° determines the DR.

Minimum 10 bits are needed for a phase resolution better than 0.1° .



DAC Floor Plan



5 thermometer MSB and 5 binary LSB bits.

Key Building Blocks (RF)

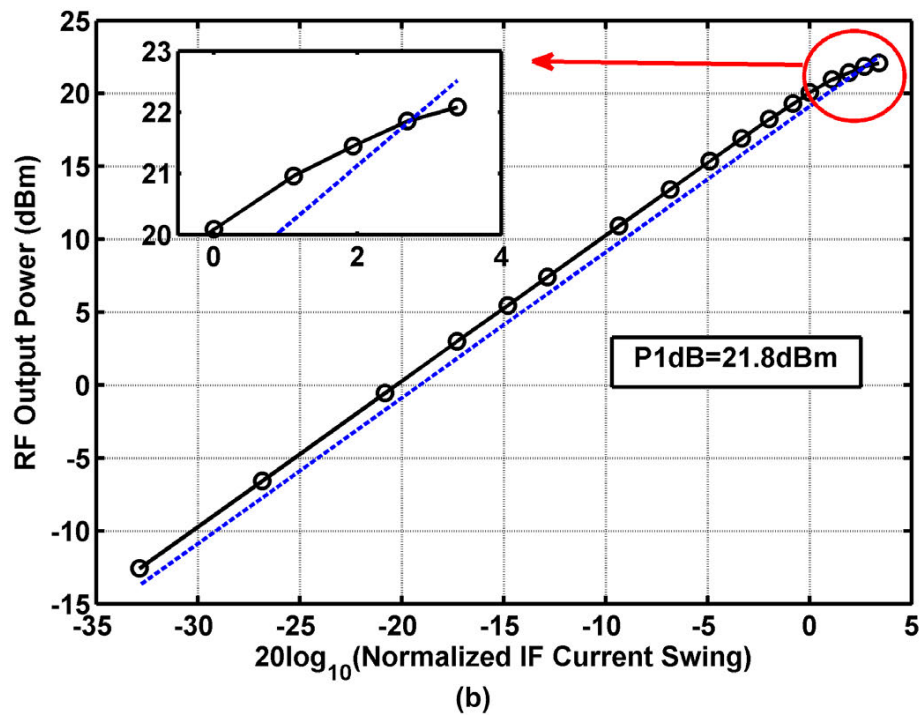
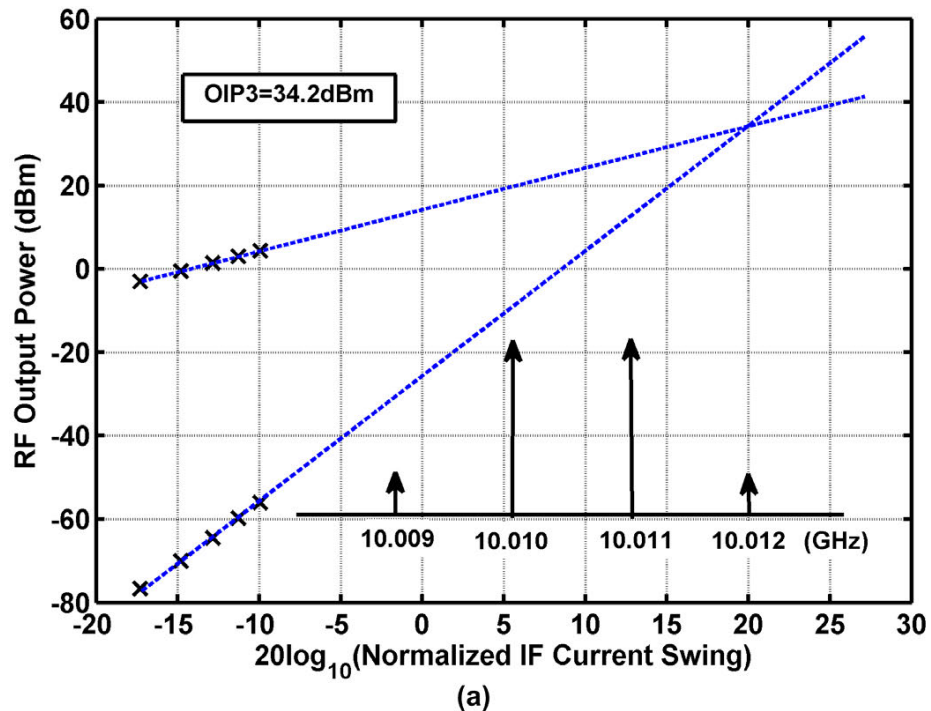
- **Quadrature double-balanced mixer**
- **How linear is the mixer?**
- **LO routing on the chip**

Mixer Linearity

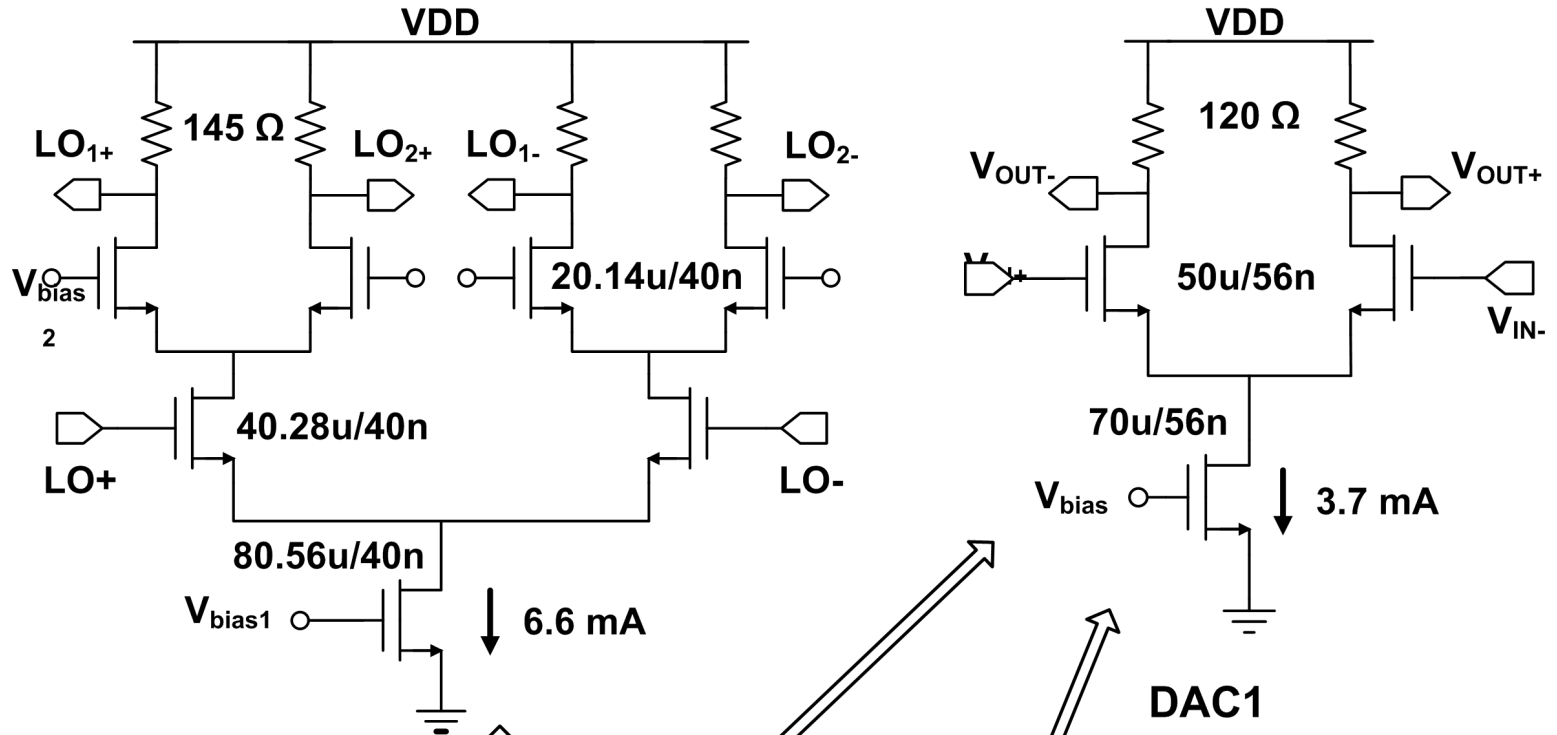
Simulated OIP3 and P1dB.

Two-tone test with LO at 10 GHz and IF at 10 and 11 MHz.

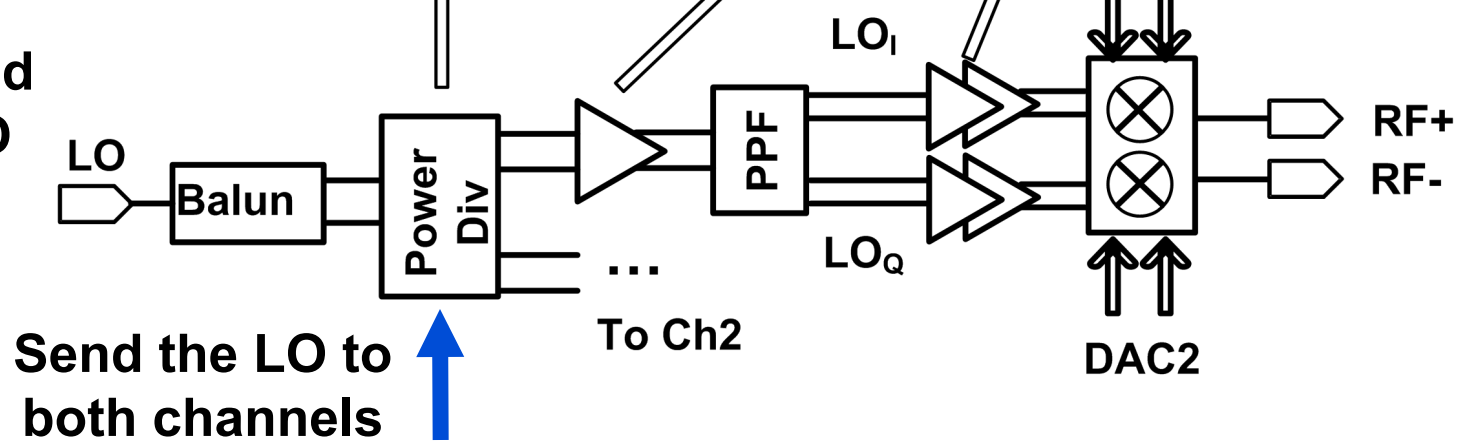
One-tone test with LO at 10 GHz and IF at 10 MHz.



LO Chain



Single-ended external LO



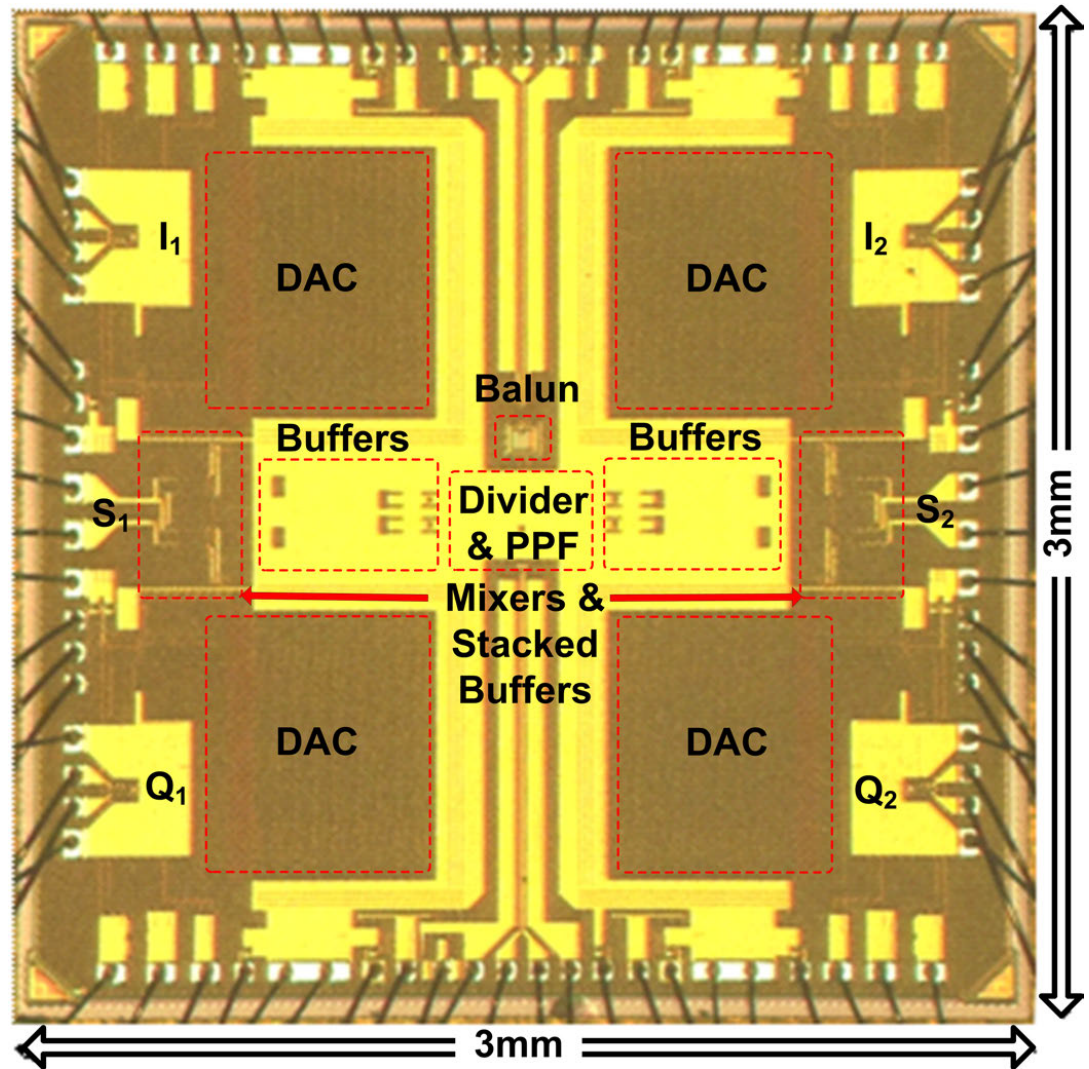
Send the LO to both channels



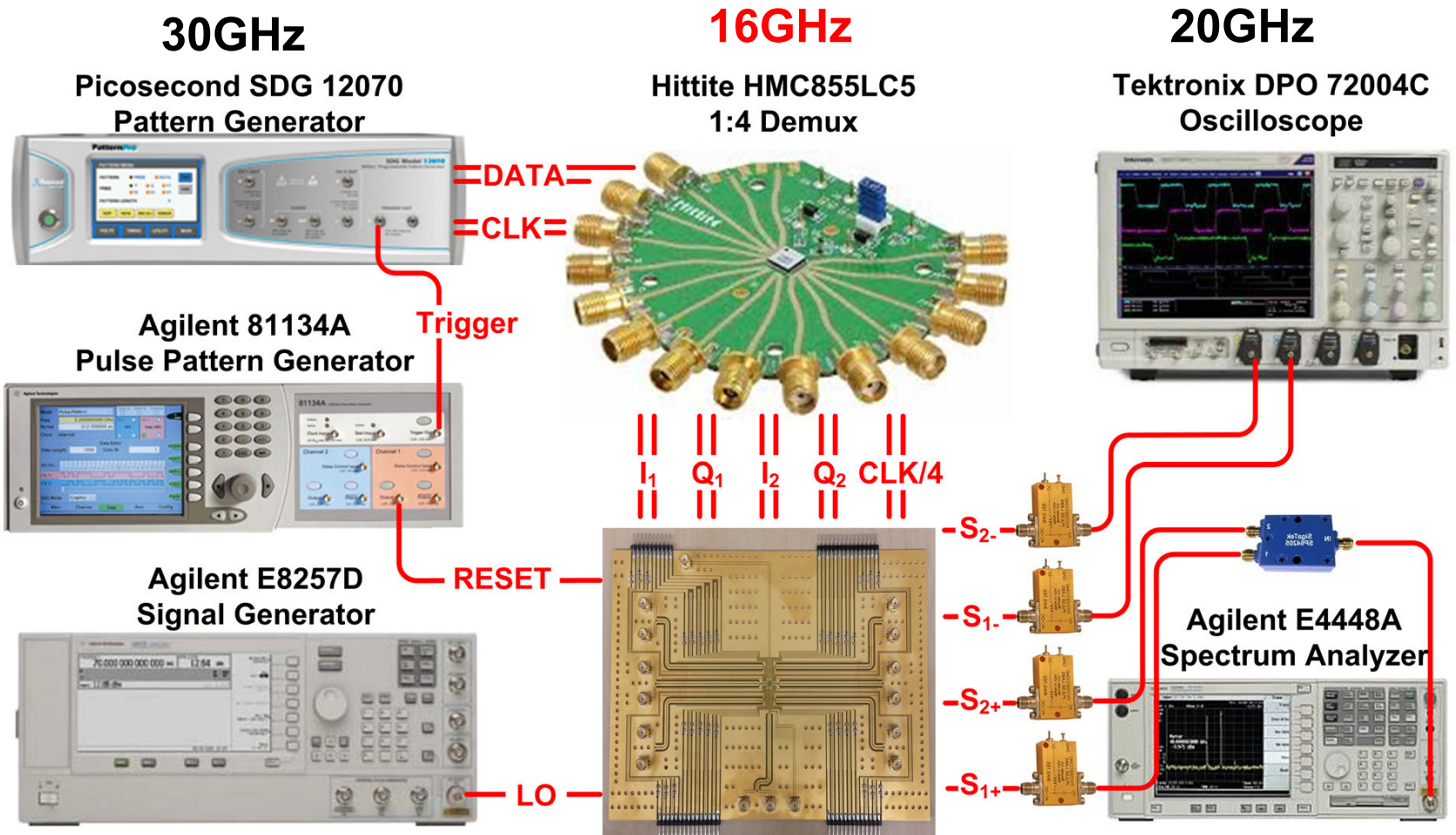
Chip Photo

Block	Power Consumption
Staked-FET + Mixer + DAC	280mA From 4V
DAC	235mA from 1.5V
LO Chain	78mA from 1.5V
Digital	135mA from 1V
Total	1.72W

- 45nm SOI technology
- Area = 9 mm²
- Testing on board



Measurement Setup



16GHz DEMUX limits the bandwidth to 400MHz.

Calibration

Calibrating both I/Q channels.

LO at 10GHz and IF at 10MHz.

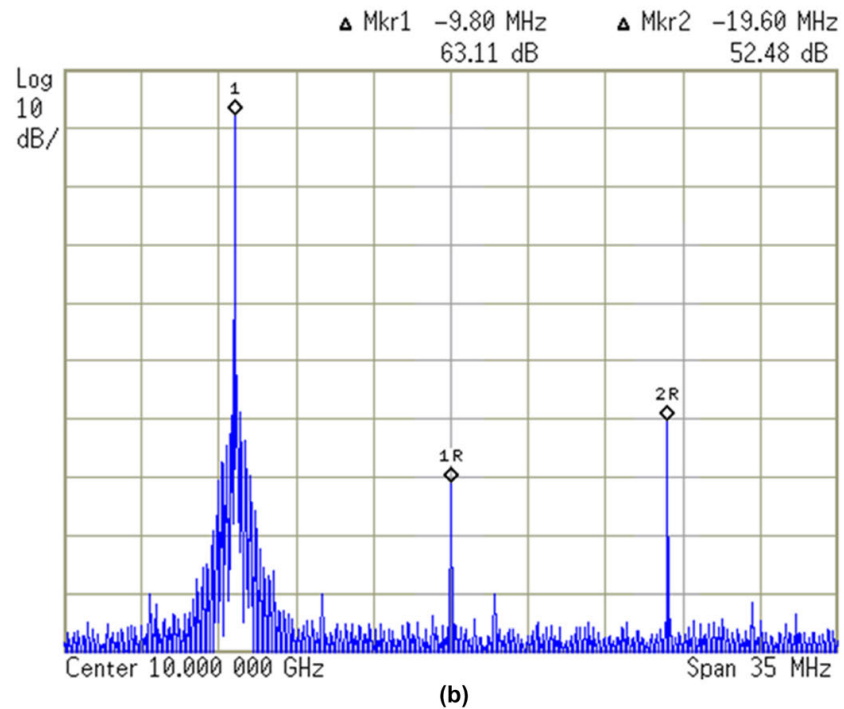
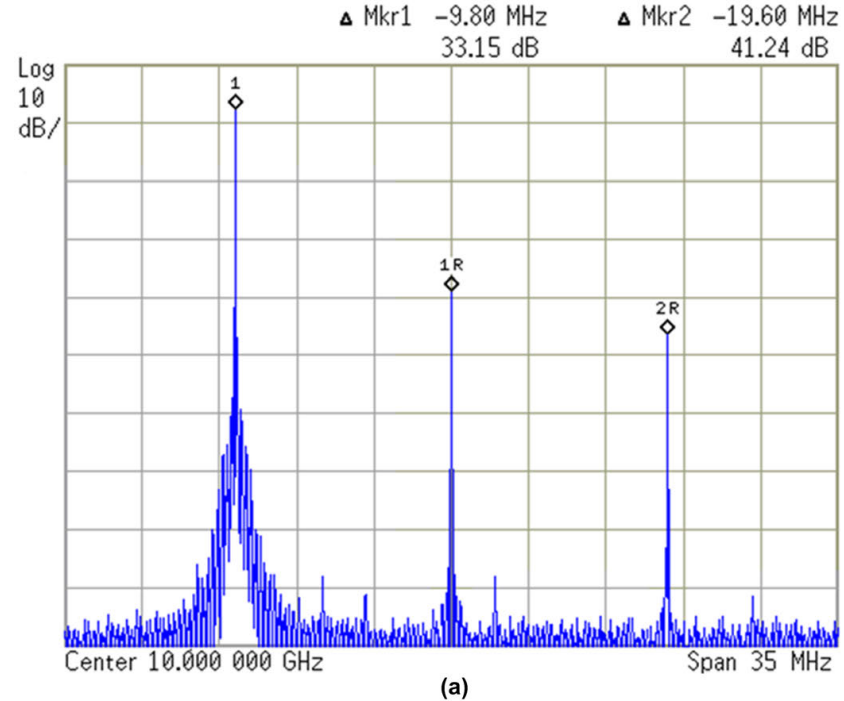
High resolution DACs can

adjust the dc level and swing

amplitude to improve the

measured LO leakage and

sideband suppression.

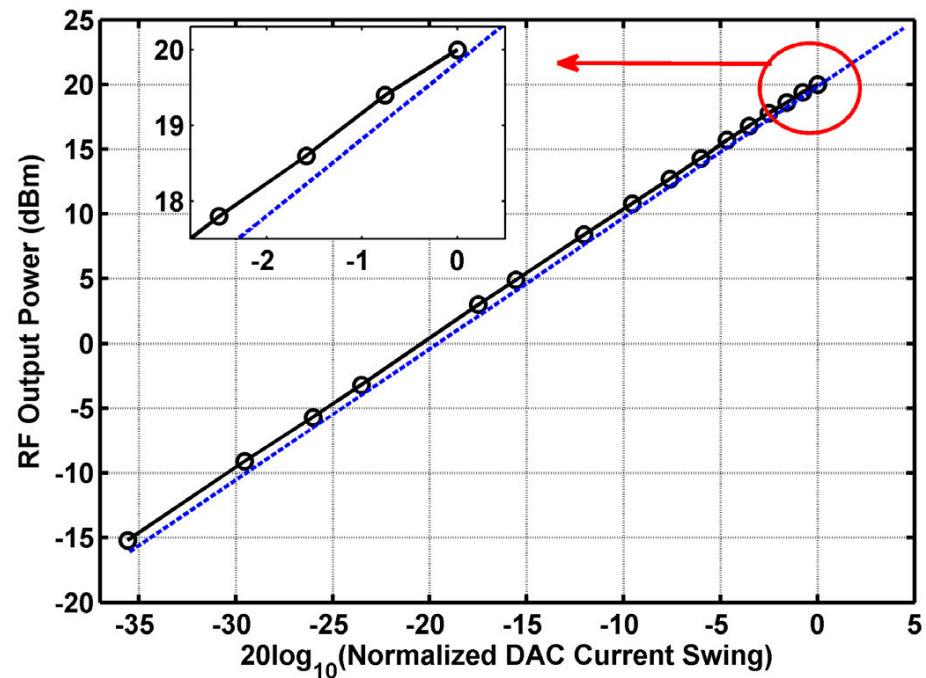


Measured P1dB and OIP3

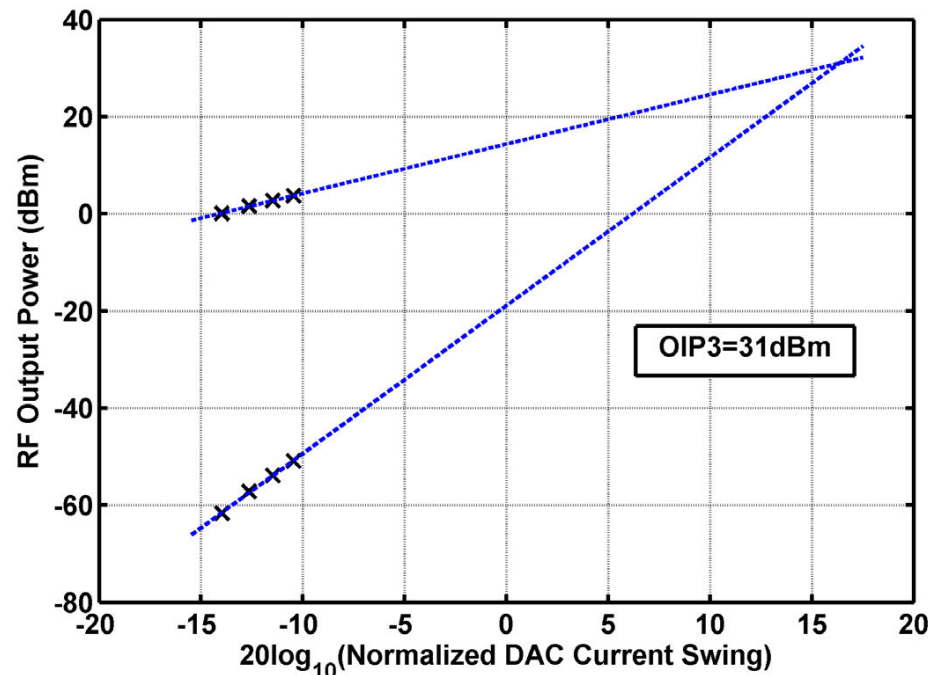
Current Swing is limited by DAC current. P1dB is slightly larger than 20dBm.

(Simulated P1dB=21.8dBm)

(Simulated OIP3=34.2dBm)

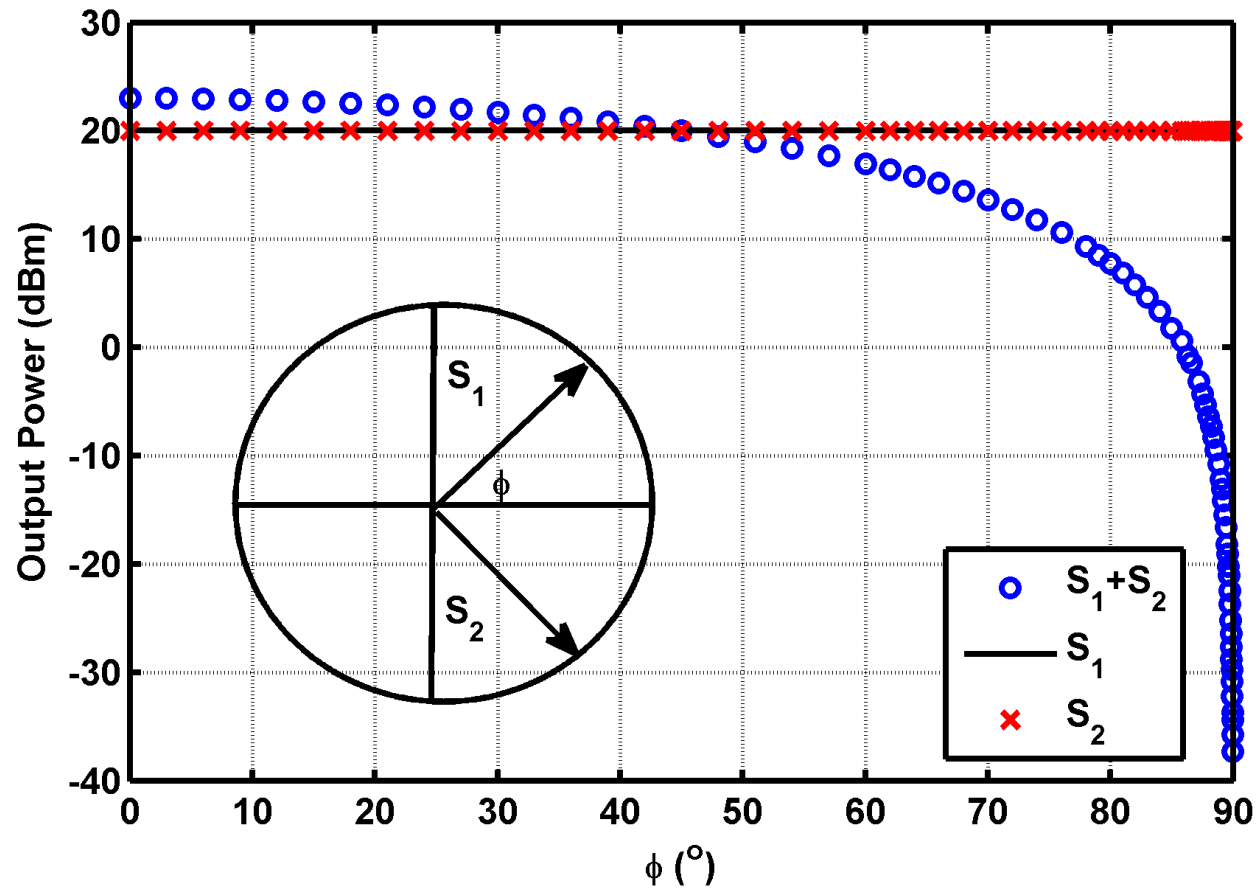


(a)



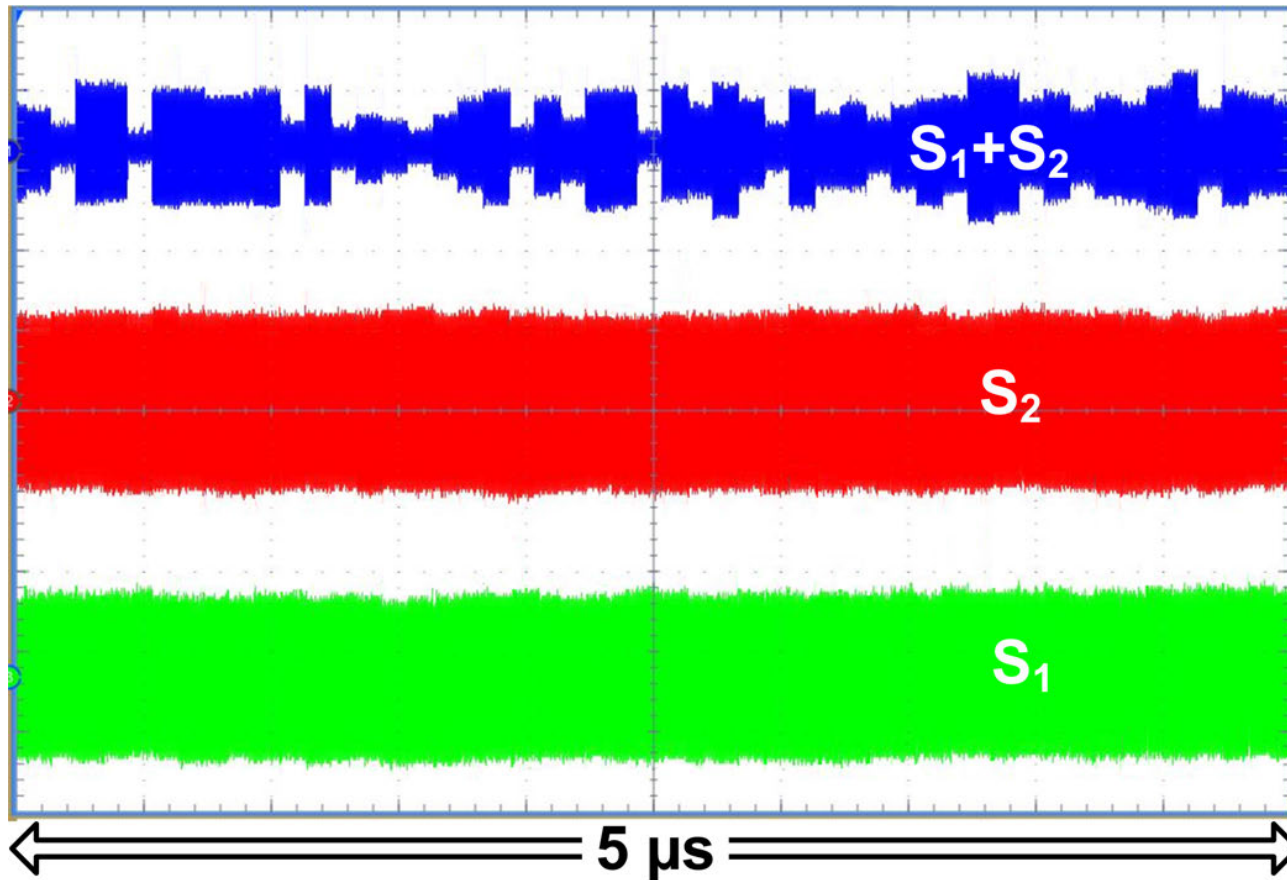
(b)

Measured Dynamic Range



60.3 dB DR with less than 1-dB steps.

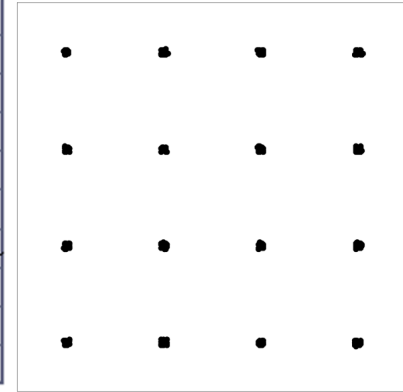
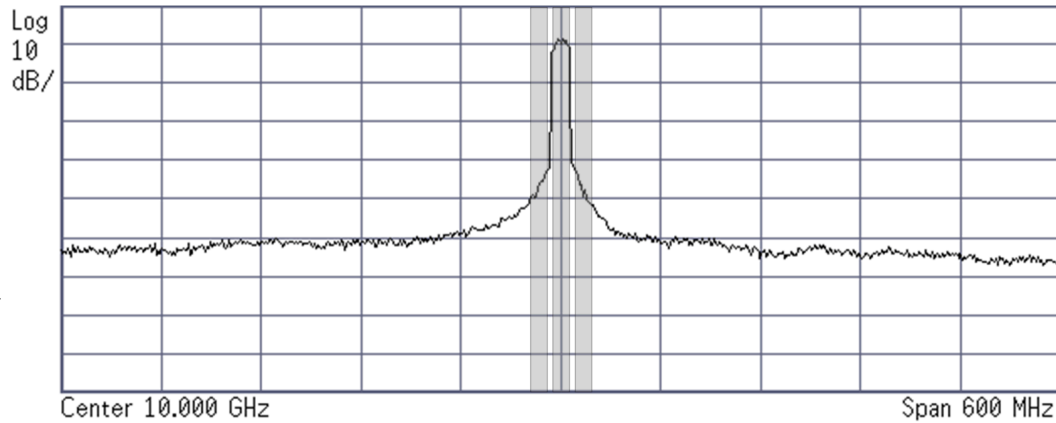
Constant Envelop Outphased Signals



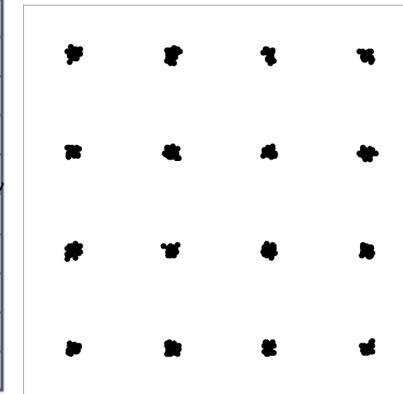
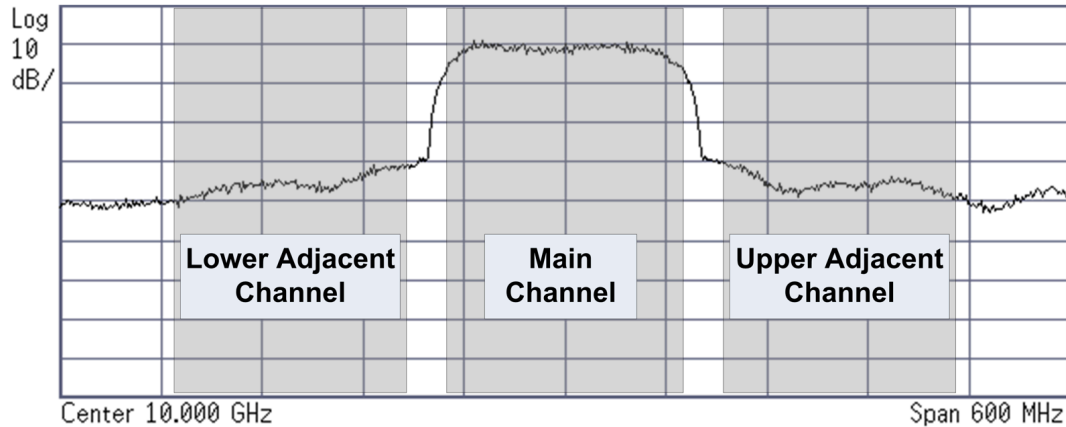
10MHz 256QAM waveform at 10GHz.

Measured 16QAM

10MHz
6.1dB PAPR
2.1% EVM
-37.0dBc ACLR

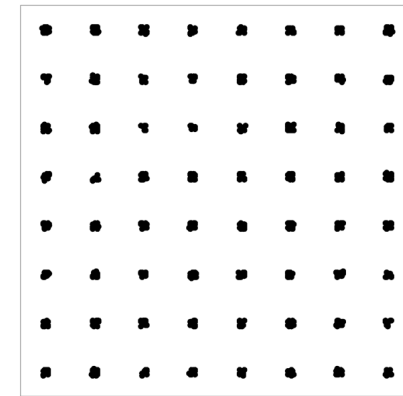
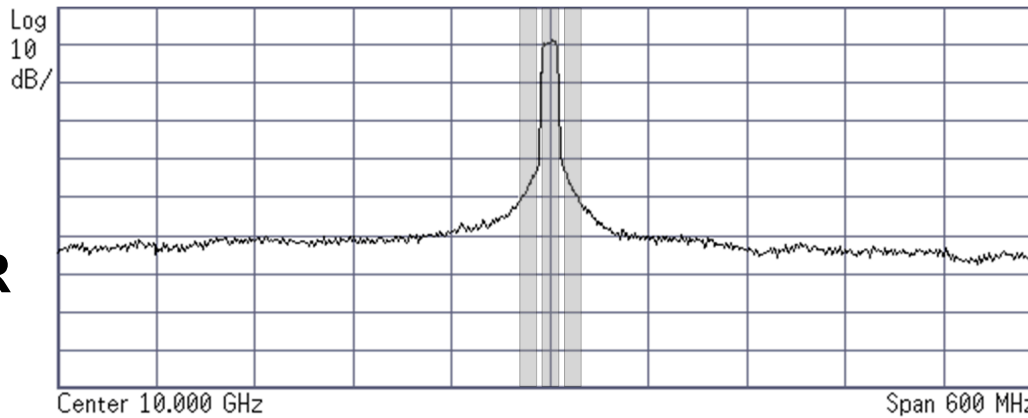


133MHz
6.6dB PAPR
3.4% EVM
-35.1dBc ACLR

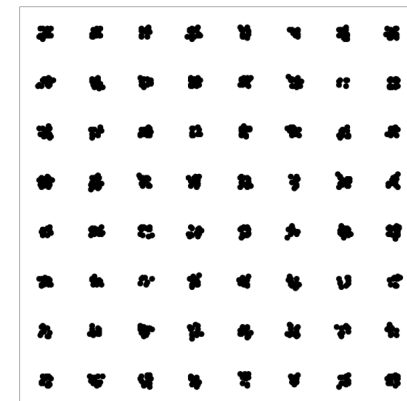
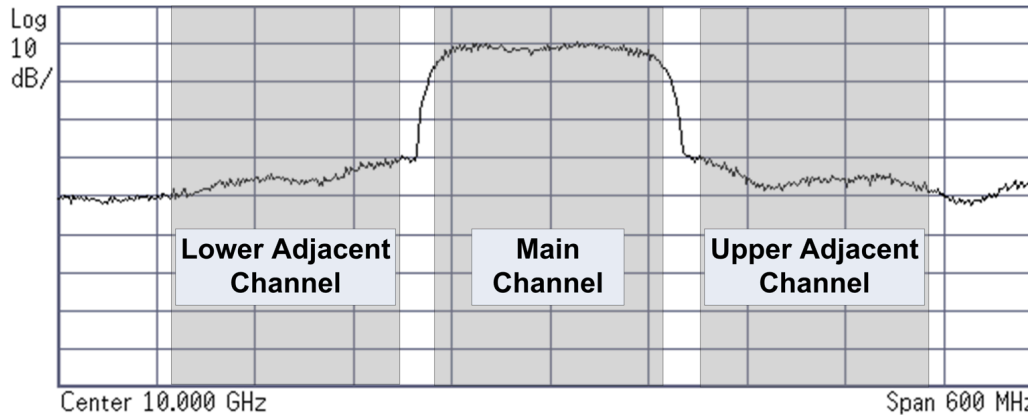


Measured 64QAM

10MHz
6.6dB PAPR
2.2% EVM
-36.9dBc ACLR

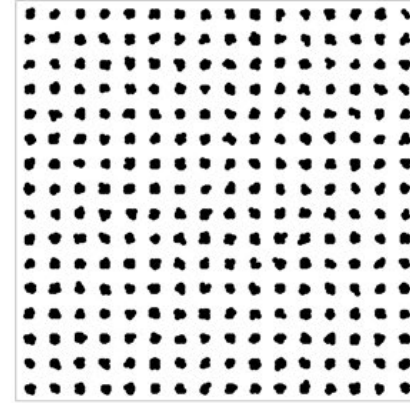
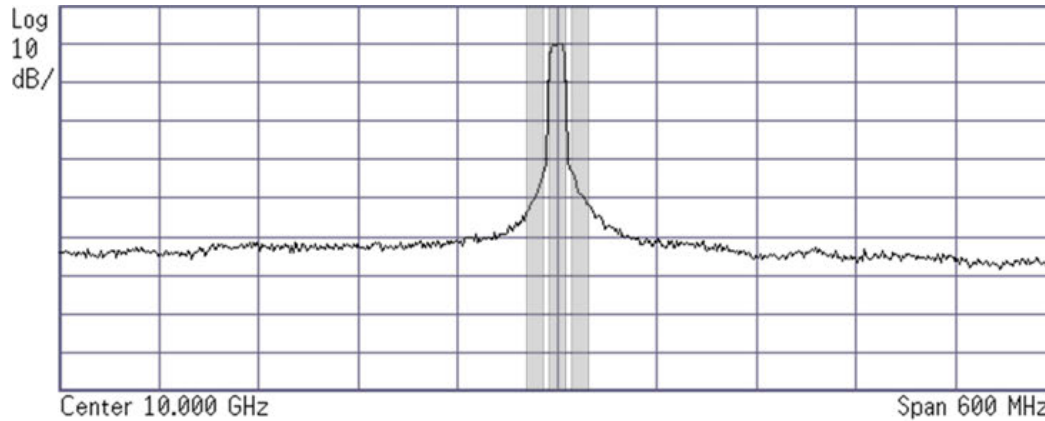


133MHz
7.1dB PAPR
3.5% EVM
-35.2dBc ACLR

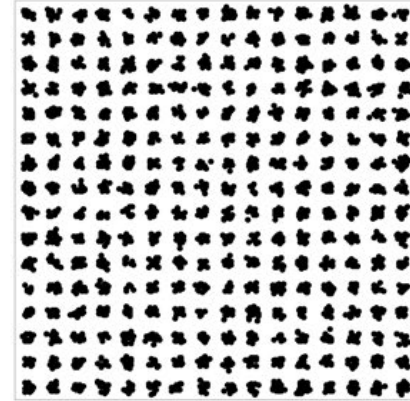
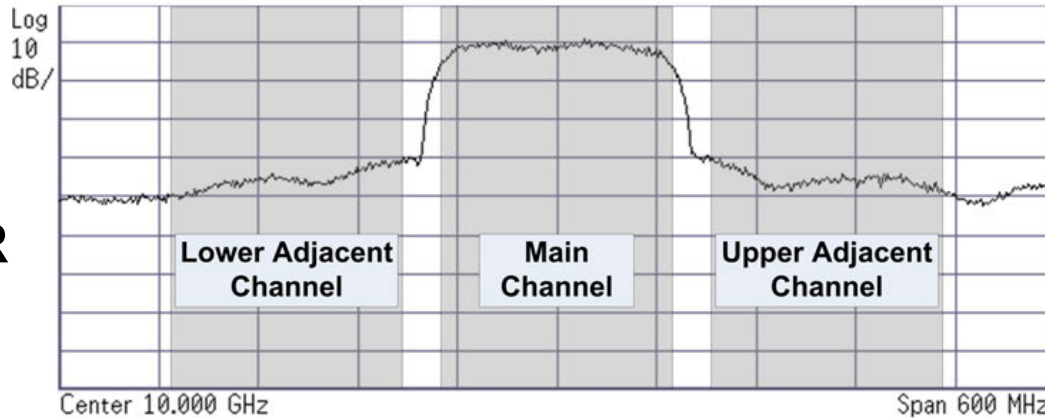


Measured 256QAM

10MHz
6.3dB PAPR
2.2% EVM
-37dBc ACLR

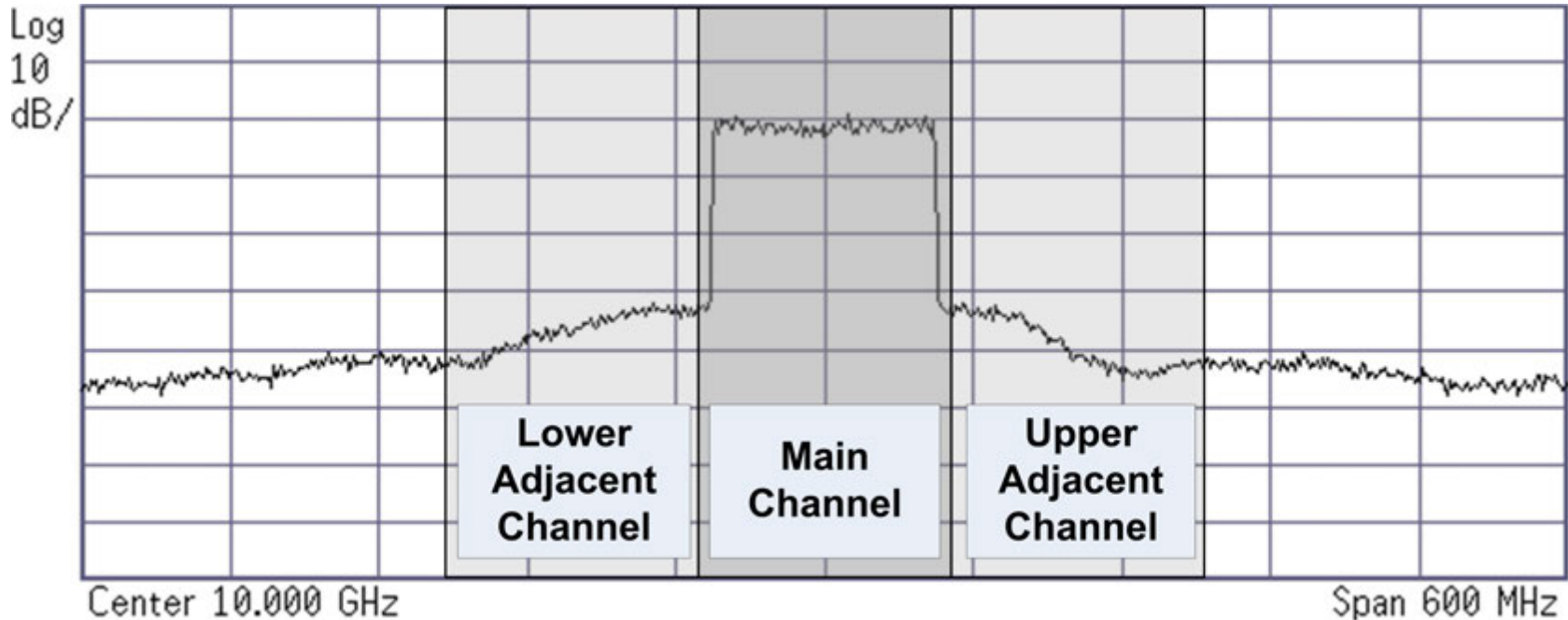


133MHz
7.2dB PAPR
3.5% EVM
-35.2dBc ACLR



Capable of 1.1Gbit/s data transmission.

Measured LTE



100-MHz LTE carrier aggregation.

8.3dB PAPR.

-35.9dBc ACLR.

Conclusion

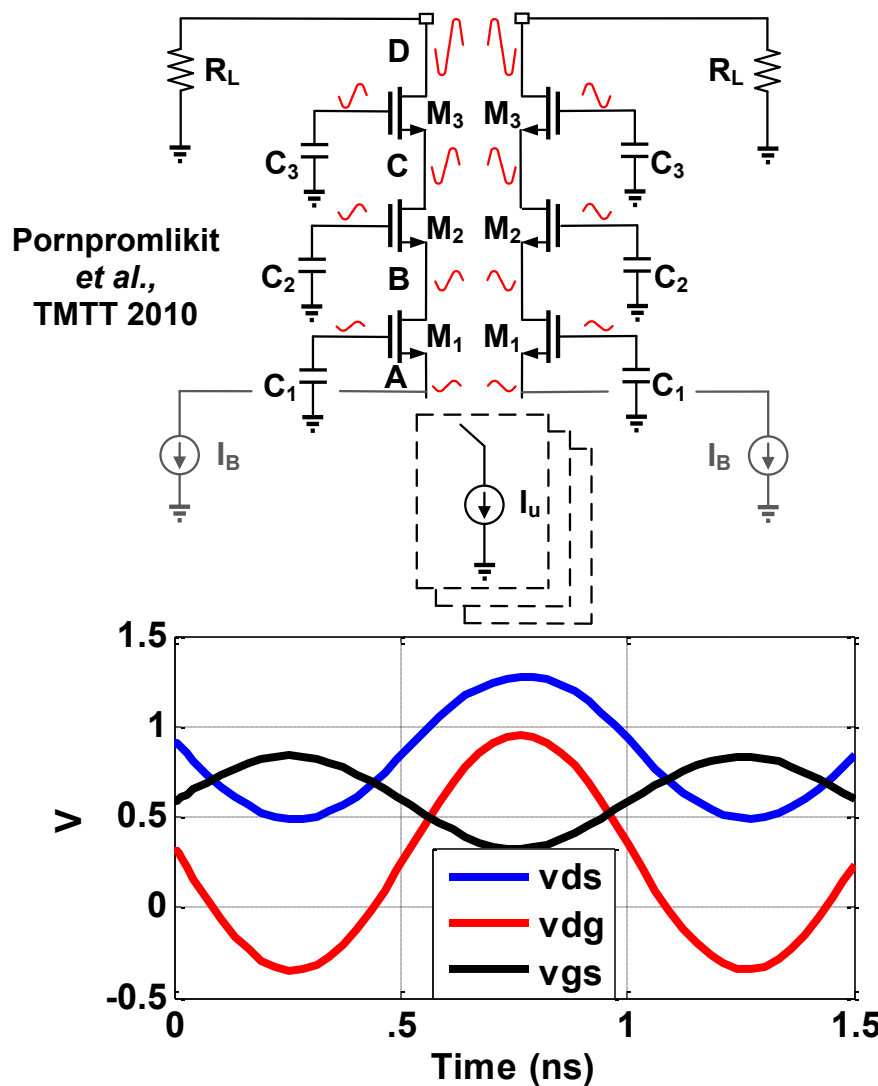
- **Microwave outphasing modulator including all the system blocks from digital to RF on-chip.**
- **Using 10-bit DACs, modulator provides a 60dB dynamic range.**
- **Modulator is capable of transmitting 100-MHz LTE and 1.1Gbit/s 256QAM waveforms.**
- **Each channel delivers 20dBm which is sufficient to drive high-power off-chip PAs without need for any pre-amplification.**

Back up Slides

- **Stacked-FET Structure**
- **SOI vs Bulk CMOS**
- **How does current bleeder improve the linearity?**

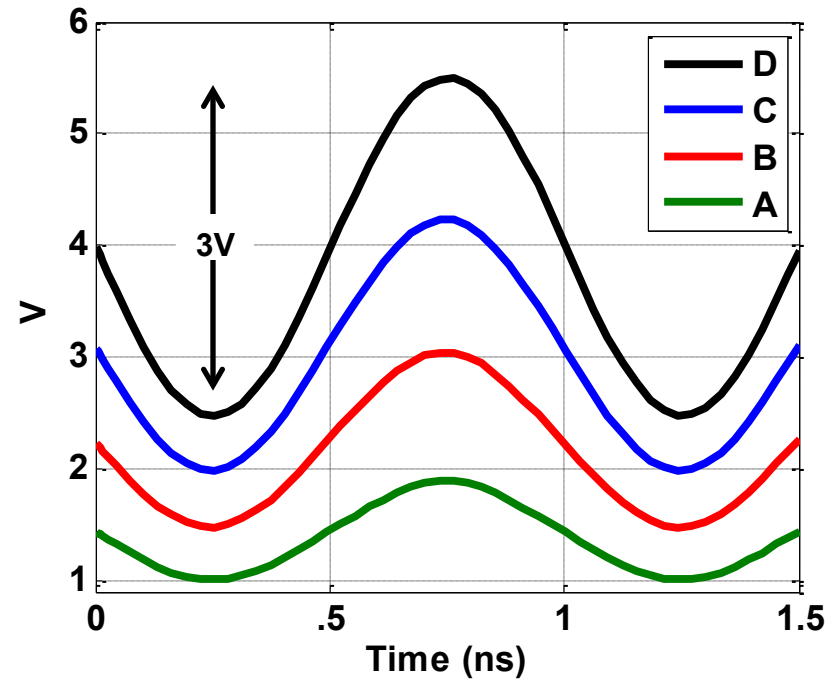
Stacked-FET Current Buffer

Keeping the voltage across the individual transistors below the breakdown.

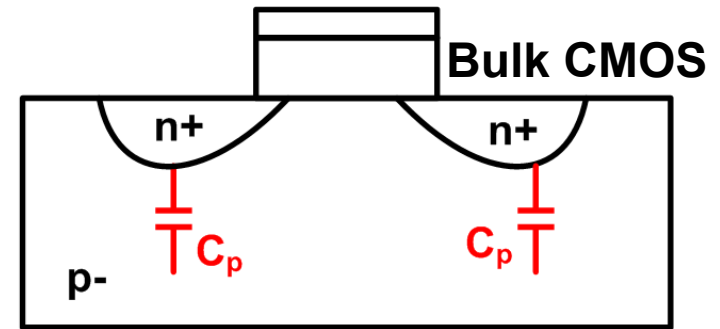
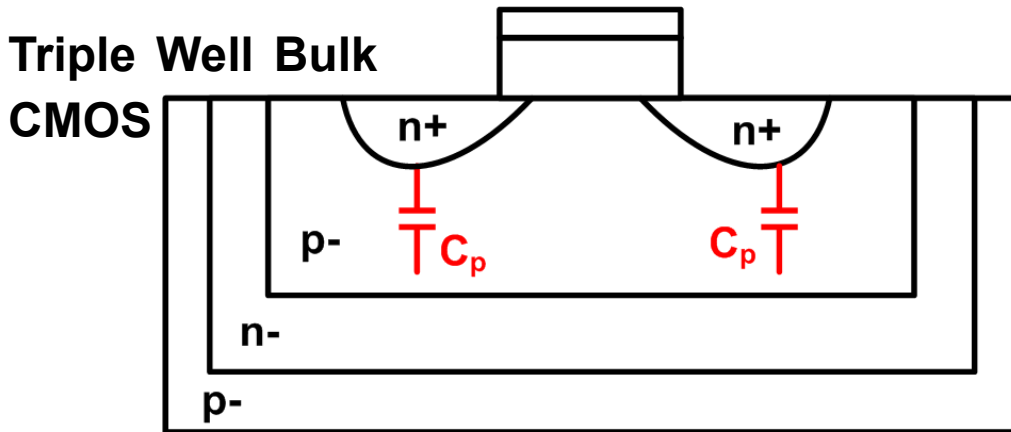


$$Z_i = \left(1 + \frac{C_{gsi}}{C_i} \right) \cdot \left(\frac{1}{g_{mi}} \parallel \frac{1}{sC_{gsi}} \right)$$

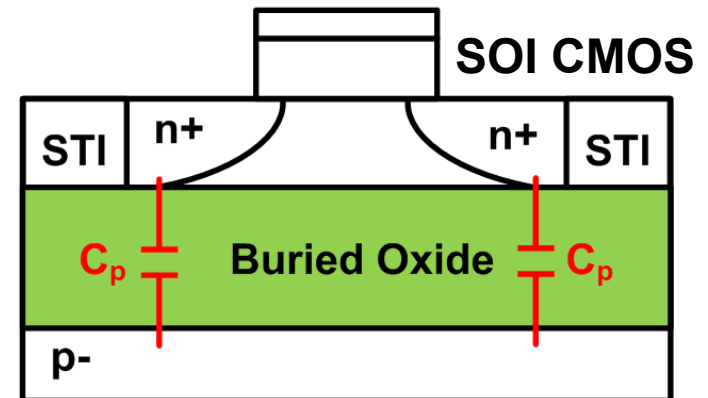
$$Z_3 > Z_2 > Z_1 \rightarrow v_3 > v_2 > v_1$$



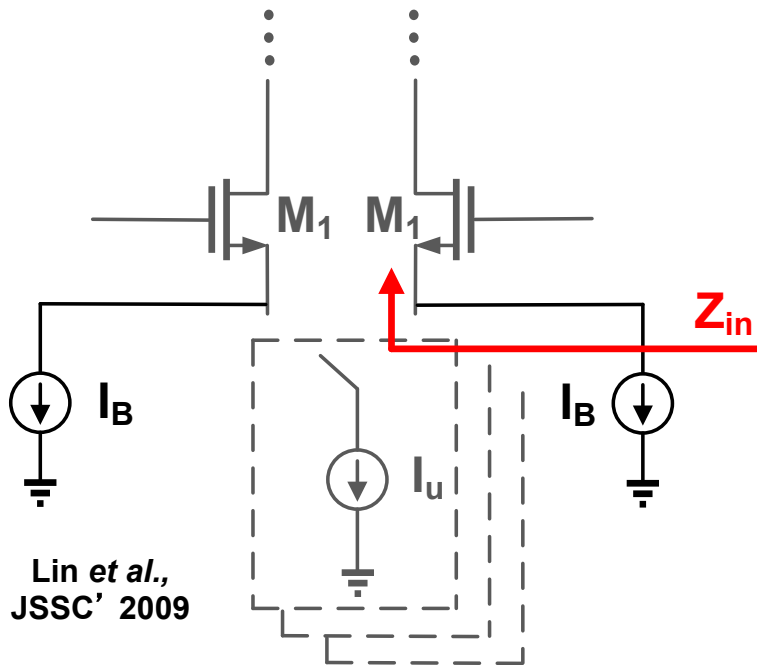
CMOS SOI for Stacking



- **No shared body.**
 - Necessary for stacking
 - Triple well in bulk CMOS or CMOS SOI
- **Buried oxide is much thicker than depletion region.**
 - Lower parasitic capacitances for SOI

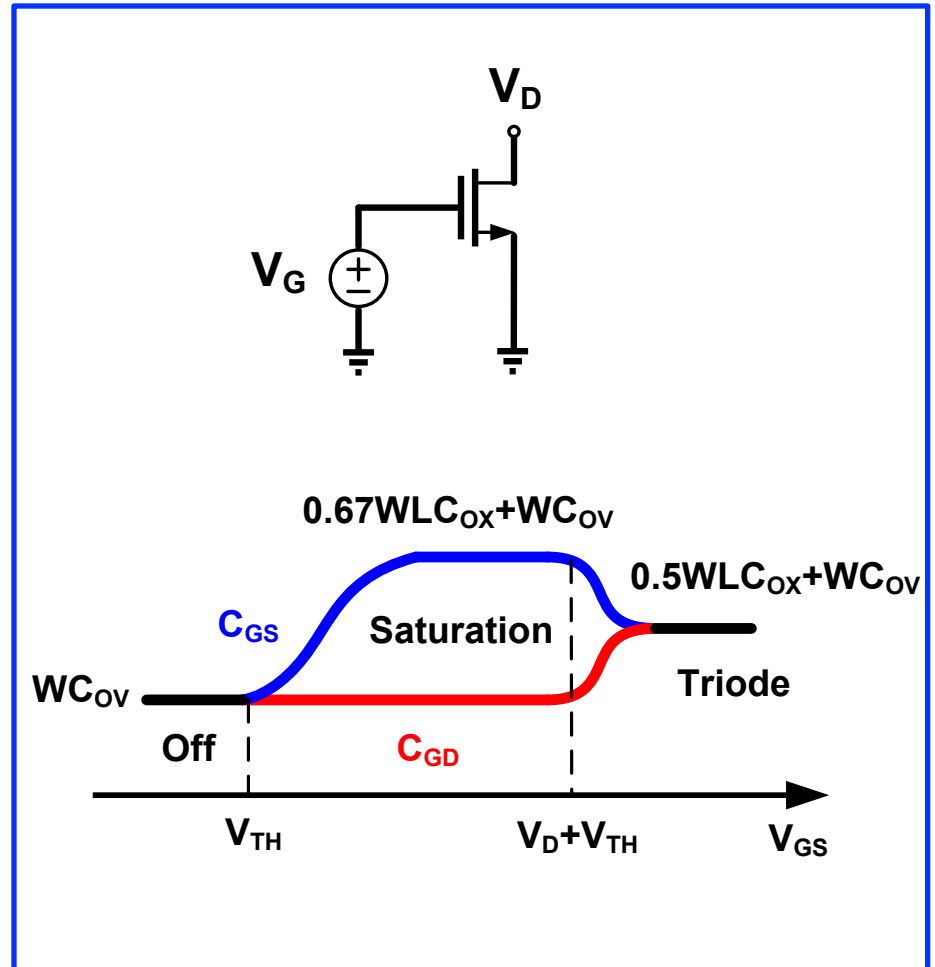


Current Bleeder

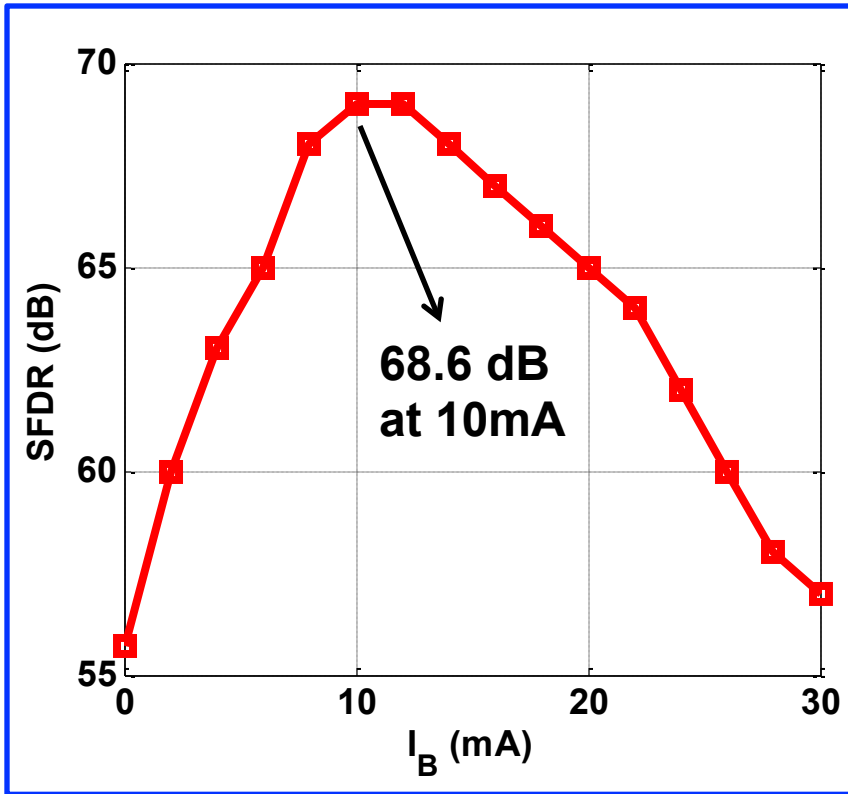


Current bleeder improves the linearity:

- M_1 always on, constant parasitic capacitance
- Z_{in}



Current Bleeder



Current bleeder improves the linearity:

- Less variation in Z_{in}

